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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5sgxma5n2f45i2n">https://www.e-xfl.com/product-detail/intel/5sgxma5n2f45i2n</a>

**Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering <sup>(1), (2), (3)</sup> (Part 2 of 2)**

Transceiver Speed Grade	Core Speed Grade							
	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L	I3YY	I4
3 GX channel—8.5 Gbps	—	Yes	Yes	Yes	—	Yes	Yes <sup>(4)</sup>	Yes

**Notes to Table 1:**

- (1) C = Commercial temperature grade; I = Industrial temperature grade.  
 (2) Lower number refers to faster speed grade.  
 (3) C2L, I2L, and I3L speed grades are for low-power devices.  
 (4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices.

**Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering <sup>(1), (2)</sup>**

Transceiver Speed Grade	Core Speed Grade			
	C1	C2	I2	I3
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	—	—
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes

**Notes to Table 2:**

- (1) C = Commercial temperature grade; I = Industrial temperature grade.  
 (2) Lower number refers to faster speed grade.

**Absolute Maximum Ratings**

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

**Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 1 of 2)**

Symbol	Description	Minimum	Maximum	Unit
V <sub>CC</sub>	Power supply for core voltage and periphery circuitry	−0.5	1.35	V
V <sub>CCPT</sub>	Power supply for programmable power technology	−0.5	1.8	V
V <sub>CCPGM</sub>	Power supply for configuration pins	−0.5	3.9	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	−0.5	3.4	V
V <sub>CCBAT</sub>	Battery back-up power supply for design security volatile key register	−0.5	3.9	V
V <sub>CCPD</sub>	I/O pre-driver power supply	−0.5	3.9	V
V <sub>CCIO</sub>	I/O power supply	−0.5	3.9	V

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

**Table 5. Maximum Allowed Overshoot During Transitions**

Symbol	Description	Condition (V)	Overshoot Duration as % @ $T_J = 100^{\circ}\text{C}$	Unit
$V_i$ (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

**Figure 1. Stratix V Device Overshoot Duration**



**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)**

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	$V_{OL}$ (V)	$V_{OH}$ (V)	$I_{ol}$ (mA)	$I_{oh}$ (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-18 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-15 Class I	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	8	-8
HSTL-15 Class II	—	$V_{REF} - 0.1$	$V_{REF} + 0.1$	—	$V_{REF} - 0.2$	$V_{REF} + 0.2$	0.4	$V_{CCIO} - 0.4$	16	-16
HSTL-12 Class I	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	8	-8
HSTL-12 Class II	-0.15	$V_{REF} - 0.08$	$V_{REF} + 0.08$	$V_{CCIO} + 0.15$	$V_{REF} - 0.15$	$V_{REF} + 0.15$	$0.25^* V_{CCIO}$	$0.75^* V_{CCIO}$	16	-16
HSUL-12	—	$V_{REF} - 0.13$	$V_{REF} + 0.13$	—	$V_{REF} - 0.22$	$V_{REF} + 0.22$	$0.1^* V_{CCIO}$	$0.9^* V_{CCIO}$	—	—

**Table 20. Differential SSTL I/O Standards for Stratix V Devices**

I/O Standard	$V_{CCIO}$ (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.2$	—	$V_{CCIO}/2 + 0.2$	0.62	$V_{CCIO} + 0.6$
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	$V_{CCIO} + 0.6$	$V_{CCIO}/2 - 0.175$	—	$V_{CCIO}/2 + 0.175$	0.5	$V_{CCIO} + 0.6$
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	$V_{CCIO}/2 - 0.15$	—	$V_{CCIO}/2 + 0.15$	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	$2(V_{IL(AC)} - V_{REF})$
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	$V_{CCIO}/2 - 0.15$	$V_{CCIO}/2$	$V_{CCIO}/2 + 0.15$	$2(V_{IH(AC)} - V_{REF})$	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	$V_{REF} - 0.15$	$V_{CCIO}/2$	$V_{REF} + 0.15$	-0.30	0.30

**Note to Table 20:**

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits ( $V_{IH(DC)}$  and  $V_{IL(DC)}$ ).

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)**

I/O Standard	$V_{CCIO}$ (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

## Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

### Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 1 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	—	40	—	710	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>	—	100	—	710	100	—	710	100	—	710	MHz
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>	—	—	400	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	—	0 to -0.5	—	—	0 to -0.5	—	%
On-chip termination resistors <sup>(21)</sup>	—	—	100	—	—	100	—	—	100	—	$\Omega$
Absolute $V_{MAX}$ <sup>(5)</sup>	Dedicated reference clock pin	—	—	1.6	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	—	—	1.2	
Absolute $V_{MIN}$	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
$V_{ICM}$ (AC coupled) <sup>(3)</sup>	Dedicated reference clock pin	1050/1000/900/850 <sup>(2)</sup>			1050/1000/900/850 <sup>(2)</sup>			1050/1000/900/850 <sup>(2)</sup>			mV
	RX reference clock pin	1.0/0.9/0.85 <sup>(4)</sup>			1.0/0.9/0.85 <sup>(4)</sup>			1.0/0.9/0.85 <sup>(4)</sup>			V
$V_{ICM}$ (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) <sup>(20)</sup>	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	$\geq 1$ MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) <sup>(17)</sup>	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)
$R_{REF}$ <sup>(19)</sup>	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	—	180 0 $\pm 1\%$	—	$\Omega$
<b>Transceiver Clocks</b>											
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	—	100 or 125	—	MHz

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock ( <code>mgmt_clk_clk</code> ) frequency	—	100	—	125	100	—	125	100	—	125	MHz
<b>Receiver</b>											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute $V_{MAX}$ for a receiver pin <sup>(5)</sup>	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) before device configuration <sup>(22)</sup>	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> , (22)	$V_{CCR\_GXB} =$ 1.0 V/1.05 V ( $V_{ICM} =$ 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	$V_{CCR\_GXB} =$ 0.90 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	$V_{CCR\_GXB} =$ 0.85 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6)</sup> , (22), (27)	—	85	—	—	85	—	—	85	—	—	mV

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	—	—	500	—	—	500	—	—	500	ps
<b>CMU PLL</b>											
Supported Data Range	—	600	—	12500	600	—	12500	600	—	8500/ 10312.5 <sup>(24)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	—	1	—	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(16)</sup>	—	—	—	10	—	—	10	—	—	10	μs
<b>ATX PLL</b>											
Supported Data Rate Range	VCO post-divider L=2	8000	—	14100	8000	—	12500	8000	—	8500/ 10312.5 <sup>(24)</sup>	Mbps
	L=4	4000	—	7050	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3525	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	1000	—	1762.5	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	—	1	—	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(16)</sup>	—	—	—	10	—	—	10	—	—	10	μs
<b>fPLL</b>											
Supported Data Range	—	600	—	3250/ 3125 <sup>(25)</sup>	600	—	3250/ 3125 <sup>(25)</sup>	600	—	3250/ 3125 <sup>(25)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	—	1	—	—	1	—	—	1	—	—	μs



Figure 2 shows the differential transmitter output waveform.

**Figure 2. Differential Transmitter Output Waveform**



Figure 3 shows the Stratix V AC gain curves for GX channels.

**Figure 3. AC Gain Curves for GX Channels (full bandwidth)**



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Figure 6 shows the Stratix V DC gain curves for GT channels.

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**Figure 6. DC Gain Curves for GT Channels**

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**Transceiver Characterization**

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

Symbol	Parameter	Min	Typ	Max	Unit
$f_{RES}$	Resolution of VCO frequency ( $f_{INPFD} = 100$ MHz)	390625	5.96	0.023	Hz

**Notes to Table 31:**

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (5) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$  MHz
  - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 - 0.95 must be  $\geq 1000$  MHz, while  $f_{VCO}$  for fractional value range 0.20 - 0.80 must be  $\geq 1200$  MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05-0.95 must be  $\geq 1000$  MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.20-0.80 must be  $\geq 1200$  MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

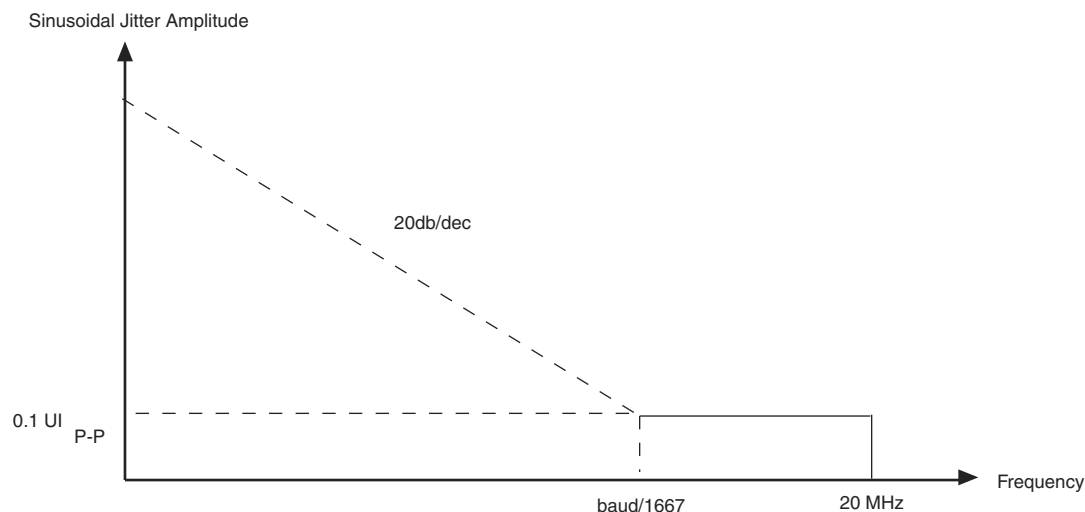
**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

Mode	Peformance							Unit
	C1	C2, C2L	I2, I2L	C3	I3, I3L, I3YY	C4	I4	
Modes using one DSP								
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
Modes using two DSPs								
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

**Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate  $\geq 1.25$  Gbps**

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $< 1.25$  Gbps.

**Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate  $< 1.25$  Gbps**

### DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

**Table 39. DLL Range Specifications for Stratix V Devices <sup>(1)</sup>**

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

**Note to Table 39:**

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices <sup>(1)</sup>, (Part 2 of 2) <sup>(2)</sup>, <sup>(3)</sup>**

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

**Notes to Table 42:**

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

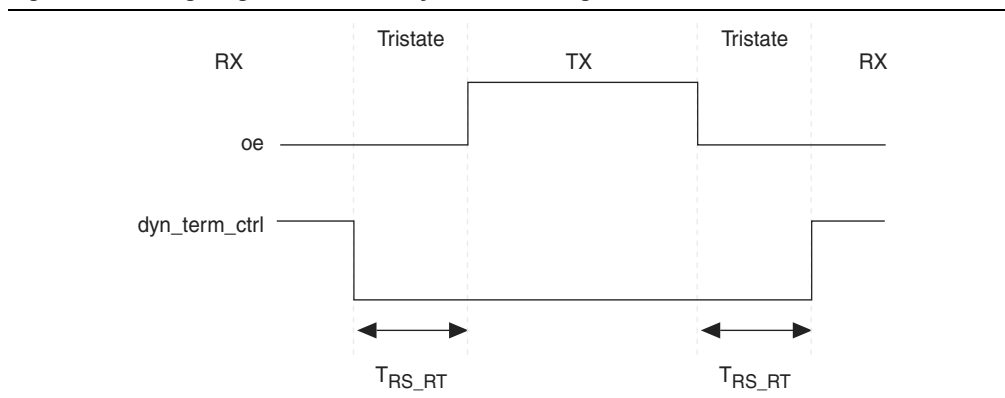
**OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

**Table 43. OCT Calibration Block Specifications for Stratix V Devices**

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
$T_{OCTCAL}$	Number of OCTUSRCLK clock cycles required for OCT $R_S/R_T$ calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
$T_{RS\_RT}$	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

**Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals**

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

Variant	Member Code	Active Serial <sup>(1)</sup>			Fast Passive Parallel <sup>(2)</sup>		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GS	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
E	E9	4	100	0.857	32	100	0.107
	EB	4	100	0.857	32	100	0.107

**Notes to Table 48:**

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

## Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

### DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA [] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA [] ratio for each combination.

**Table 49. DCLK-to-DATA[] Ratio <sup>(1)</sup> (Part 1 of 2)**

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

**Table 50. FPP Timing Parameters for Stratix V Devices <sup>(1)</sup>**

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μs
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μs
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(3)</sup>	μs
t <sub>CF2CK</sub> <sup>(6)</sup>	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t <sub>ST2CK</sub> <sup>(6)</sup>	nSTATUS high to first rising edge of DCLK	2	—	μs
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CL</sub>	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CLK</sub>	DCLK period	$1/f_{\text{MAX}}$	—	s
f <sub>MAX</sub>	DCLK frequency (FPP $\times 8/\times 16$ )	—	125	MHz
	DCLK frequency (FPP $\times 32$ )	—	100	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(4)</sup>	175	437	μs
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(5)</sup>	—	—

**Notes to Table 50:**

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

## Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

**Table 52. DCLK Frequency Specification in the AS Configuration Scheme <sup>(1), (2)</sup>**

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

**Notes to Table 52:**

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

**Figure 14. AS Configuration Timing**



**Notes to Figure 14:**

- (1) If you are using AS ×4 mode, this signal represents the AS\_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

**Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices <sup>(1), (2)</sup> (Part 1 of 2)**

Symbol	Parameter	Minimum	Maximum	Units
$t_{CO}$	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
$t_{SU}$	Data setup time before falling edge on DCLK	1.5	—	ns
$t_H$	Data hold time after falling edge on DCLK	0	—	ns



Table 54 lists the PS configuration timing parameters for Stratix V devices.

**Table 54. PS Timing Parameters for Stratix V Devices**

Symbol	Parameter	Minimum	Maximum	Units
$t_{CF2CD}$	nCONFIG low to CONF_DONE low	—	600	ns
$t_{CF2ST0}$	nCONFIG low to nSTATUS low	—	600	ns
$t_{CFG}$	nCONFIG low pulse width	2	—	$\mu$ s
$t_{STATUS}$	nSTATUS low pulse width	268	1,506 <sup>(1)</sup>	$\mu$ s
$t_{CF2ST1}$	nCONFIG high to nSTATUS high	—	1,506 <sup>(2)</sup>	$\mu$ s
$t_{CF2CK}$ <sup>(5)</sup>	nCONFIG high to first rising edge on DCLK	1,506	—	$\mu$ s
$t_{ST2CK}$ <sup>(5)</sup>	nSTATUS high to first rising edge of DCLK	2	—	$\mu$ s
$t_{DSU}$	DATA [] setup time before rising edge on DCLK	5.5	—	ns
$t_{DH}$	DATA [] hold time after rising edge on DCLK	0	—	ns
$t_{CH}$	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CL}$	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
$t_{CLK}$	DCLK period	$1/f_{MAX}$	—	s
$f_{MAX}$	DCLK frequency	—	125	MHz
$t_{CD2UM}$	CONF_DONE high to user mode <sup>(3)</sup>	175	437	$\mu$ s
$t_{CD2CU}$	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
$t_{CD2UMC}$	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup>	—	—

**Notes to Table 54:**

- (1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section.
- (5) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

## Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

**Table 55. Initialization Clock Source Option and the Maximum Frequency**

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles <sup>(1)</sup>
Internal Oscillator	AS, PS, FPP	12.5 MHz	8576
CLKUSR	AS, PS, FPP <sup>(2)</sup>	125 MHz	
DCLK	PS, FPP	125 MHz	

**Notes to Table 55:**

- (1) The minimum number of clock cycles required for device initialization.
- (2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

## Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

**Table 56. Remote System Upgrade Circuitry Timing Specifications**

Parameter	Minimum	Maximum	Unit
$t_{RU\_nCONFIG}^{(1)}$	250	—	ns
$t_{RU\_nRSTIMER}^{(2)}$	250	—	ns

**Notes to Table 56:**

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

## User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

**Table 57. 12.5-MHz Internal Oscillator Specifications**

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

## I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.



You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)**

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Table 60. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	SW (sampling window)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p> 
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p> 
T	$t_c$	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).
	$t_{DUTY}$	<p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p><b>Timing Unit Interval (TUI)</b></p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = <math>1/(\text{receiver input clock frequency multiplication factor}) = t_c/w</math>)</p>
	$t_{FALL}$	Signal high-to-low transition time (80-20%)
	$t_{INCCJ}$	Cycle-to-cycle jitter tolerance on the PLL clock input.
	$t_{OUTPJ\_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	$t_{OUTPJ\_DC}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{RISE}$	Signal low-to-high transition time (20-80%)
U	—	—

## Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

Date	Version	Changes
June 2018	3.9	<ul style="list-style-type: none"> <li>■ Added the “Stratix V Device Overshoot Duration” figure.</li> </ul>
April 2017	3.8	<ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “PS Timing Parameters for Stratix V Devices” table.</li> <li>■ Changed the condition for <math>100\text{-}\Omega</math> <math>R_D</math> in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table.</li> </ul>
June 2016	3.7	<ul style="list-style-type: none"> <li>■ Added the <math>V_{ID}</math> minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table</li> <li>■ Added the <math>I_{OUT}</math> specification to the “Absolute Maximum Ratings for Stratix V Devices” table.</li> </ul>
December 2015	3.6	<ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> </ul>
December 2015	3.5	<ul style="list-style-type: none"> <li>■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table.</li> </ul>
July 2015	3.4	<ul style="list-style-type: none"> <li>■ Changed the data rate specification for transceiver speed grade 3 in the following tables: <ul style="list-style-type: none"> <li>■ “Transceiver Specifications for Stratix V GX and GS Devices”</li> <li>■ “Stratix V Standard PCS Approximate Maximum Date Rate”</li> <li>■ “Stratix V 10G PCS Approximate Maximum Data Rate”</li> </ul> </li> <li>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the <math>t_{CO}</math> maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table.</li> <li>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> </ul>

**Table 61. Document Revision History (Part 2 of 3)**

Date	Version	Changes
November 2014	3.3	<ul style="list-style-type: none"> <li>■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> <li>■ Added the I3YY speed grade to the <math>V_{CC}</math> description in Table 6.</li> <li>■ Added the I3YY speed grade to <math>V_{CCHIP\_L}</math>, <math>V_{CCHIP\_R}</math>, <math>V_{CCHSSI\_L}</math>, and <math>V_{CCHSSI\_R}</math> descriptions in Table 7.</li> <li>■ Added 240-Ω to Table 11.</li> <li>■ Changed CDR PPM tolerance in Table 23.</li> <li>■ Added additional max data rate for fPLL in Table 23.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> <li>■ Changed CDR PPM tolerance in Table 28.</li> <li>■ Added additional max data rate for fPLL in Table 28.</li> <li>■ Changed the mode descriptions for MLAB and M20K in Table 33.</li> <li>■ Changed the Max value of <math>f_{HCLK\_OUT}</math> for the C2, C2L, I2, I2L speed grades in Table 36.</li> <li>■ Changed the frequency ranges for C1 and C2 in Table 39.</li> <li>■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> <li>■ Added note about nSTATUS to Table 50, Table 51, Table 54.</li> <li>■ Changed the available settings in Table 58.</li> <li>■ Changed the note in “Periphery Performance”.</li> <li>■ Updated the “I/O Standard Specifications” section.</li> <li>■ Updated the “Raw Binary File Size” section.</li> <li>■ Updated the receiver voltage input range in Table 22.</li> <li>■ Updated the max frequency for the LVDS clock network in Table 36.</li> <li>■ Updated the DCLK note to Figure 11.</li> <li>■ Updated Table 23 <math>VO_{CM}</math> (DC Coupled) condition.</li> <li>■ Updated Table 6 and Table 7.</li> <li>■ Added the DCLK specification to Table 55.</li> <li>■ Updated the notes for Table 47.</li> <li>■ Updated the list of parameters for Table 56.</li> </ul>
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	<ul style="list-style-type: none"> <li>■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> <li>■ Added Figure 1 and Figure 3</li> <li>■ Added the “Transceiver Characterization” section</li> <li>■ Removed all “Preliminary” designations.</li> </ul>