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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	185000
Number of Logic Elements/Cells	490000
Total RAM Bits	46080000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/intel/5sgxma5n3f40i3n">https://www.e-xfl.com/product-detail/intel/5sgxma5n3f40i3n</a>

## Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)**

Symbol	Description	Condition	Min <sup>(4)</sup>	Typ	Max <sup>(4)</sup>	Unit
V <sub>CC</sub>	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	—	0.87	0.9	0.93	V
	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) <sup>(3)</sup>	—	0.82	0.85	0.88	V
V <sub>CCPT</sub>	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V <sub>CC_AUX</sub>	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V <sub>CCPD</sub> <sup>(1)</sup>	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V <sub>CCIO</sub>	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V <sub>CCPGM</sub>	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V <sub>CCA_FPLL</sub>	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V <sub>CCD_FPLL</sub>	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V <sub>CCBAT</sub> <sup>(2)</sup>	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V <sub>I</sub>	DC input voltage	—	−0.5	—	3.6	V
V <sub>O</sub>	Output voltage	—	0	—	V <sub>CCIO</sub>	V
T <sub>J</sub>	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C

**Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)**

Symbol	Description	Condition	Min <sup>(4)</sup>	Typ	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 $\mu$ s	—	100 ms	—
		Fast POR	200 $\mu$ s	—	4 ms	—

**Notes to Table 6:**

- (1) V<sub>CCPD</sub> must be 2.5 V when V<sub>CCIO</sub> is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V<sub>CCPD</sub> must be 3.0 V when V<sub>CCIO</sub> is 3.0 V.
- (2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.
- (3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.
- (4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA_GXBL</sub> (1), (3)	Transceiver channel PLL power supply (left side)	GX, GS, GT	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V <sub>CCA_GXBR</sub> (1), (3)	Transceiver channel PLL power supply (right side)	GX, GS	2.85	3.0	3.15	V
			2.375	2.5	2.625	
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCR_GXBL</sub> (2)	Receiver analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)**

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
$V_{CCR\_GXBR}$ (2)	Receiver analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCR\_GTBR}$	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCT\_GXBL}$ (2)	Transmitter analog power supply (left side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GXBR}$ (2)	Transmitter analog power supply (right side)	GX, GS, GT	0.82	0.85	0.88	V
			0.87	0.90	0.93	
			0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT\_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
$V_{CCH\_GXBL}$	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
$V_{CCH\_GXBR}$	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

**Notes to Table 7:**

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

## Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

### Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 1 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	—	40	—	710	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>	—	100	—	710	100	—	710	100	—	710	MHz
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>	—	—	400	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reconfiguration clock ( <code>mgmt_clk_clk</code> ) frequency	—	100	—	125	100	—	125	100	—	125	MHz
<b>Receiver</b>											
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Data rate (Standard PCS) (9), (23)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 (24)	Mbps
Data rate (10G PCS) (9), (23)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 (24)	Mbps
Absolute $V_{MAX}$ for a receiver pin <sup>(5)</sup>	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute $V_{MIN}$ for a receiver pin	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) before device configuration <sup>(22)</sup>	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak- to-peak differential input voltage $V_{ID}$ (diff p- p) after device configuration <sup>(18)</sup> , (22)	$V_{CCR\_GXB} =$ 1.0 V/1.05 V ( $V_{ICM} =$ 0.70 V)	—	—	2.0	—	—	2.0	—	—	2.0	V
	$V_{CCR\_GXB} =$ 0.90 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
	$V_{CCR\_GXB} =$ 0.85 V ( $V_{ICM} = 0.6$ V)	—	—	2.4	—	—	2.4	—	—	2.4	V
Minimum differential eye opening at receiver serial input pins <sup>(6)</sup> , (22), (27)	—	85	—	—	85	—	—	85	—	—	mV

Table 25 shows the approximate maximum data rate using the standard PCS.

**Table 25. Stratix V Standard PCS Approximate Maximum Date Rate <sup>(1)</sup>, <sup>(3)</sup>**

Mode <sup>(2)</sup>	Transceiver Speed Grade	PMA Width	20	20	16	16	10	10	8	8
		PCS/Core Width	40	20	32	16	20	10	16	8
FIFO	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
		C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
	3	C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
		I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
Register	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	2	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
		C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
	3	C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
		I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
		C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

**Notes to Table 25:**

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Figure 2 shows the differential transmitter output waveform.

**Figure 2. Differential Transmitter Output Waveform**



Figure 3 shows the Stratix V AC gain curves for GX channels.

**Figure 3. AC Gain Curves for GX Channels (full bandwidth)**



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.



**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) <sup>(1)</sup>**

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) <sup>(6)</sup>	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) <sup>(6)</sup>	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to −0.5	—	—	0 to −0.5	—	%
On-chip termination resistors <sup>(19)</sup>	—	—	100	—	—	100	—	Ω
Absolute V <sub>MAX</sub> <sup>(3)</sup>	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V <sub>MIN</sub>	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V <sub>ICM</sub> (AC coupled)	Dedicated reference clock pin	1050/1000 <sup>(2)</sup>			1050/1000 <sup>(2)</sup>			mV
	RX reference clock pin	1.0/0.9/0.85 <sup>(22)</sup>			1.0/0.9/0.85 <sup>(22)</sup>			V
V <sub>ICM</sub> (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) <sup>(1)</sup>**

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors <sup>(7)</sup>	GT channels	—	100	—	—	100	—	$\Omega$
Differential on-chip termination resistors for GX channels <sup>(19)</sup>	85- $\Omega$ setting	—	85 $\pm$ 30%	—	—	85 $\pm$ 30%	—	$\Omega$
	100- $\Omega$ setting	—	100 $\pm$ 30%	—	—	100 $\pm$ 30%	—	$\Omega$
	120- $\Omega$ setting	—	120 $\pm$ 30%	—	—	120 $\pm$ 30%	—	$\Omega$
	150- $\Omega$ setting	—	150 $\pm$ 30%	—	—	150 $\pm$ 30%	—	$\Omega$
V <sub>ICM</sub> (AC coupled)	GT channels	—	650	—	—	650	—	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 0.85 V or 0.9 V	—	600	—	—	600	—	mV
	VCCR_GXB = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	VCCR_GXB = 1.0 V half bandwidth	—	750	—	—	750	—	mV
t <sub>LTR</sub> <sup>(9)</sup>	—	—	—	10	—	—	10	$\mu$ s
t <sub>LTD</sub> <sup>(10)</sup>	—	4	—	—	4	—	—	$\mu$ s
t <sub>LTD_manual</sub> <sup>(11)</sup>	—	4	—	—	4	—	—	$\mu$ s
t <sub>LTR_LTD_manual</sub> <sup>(12)</sup>	—	15	—	—	15	—	—	$\mu$ s
Run Length	GT channels	—	—	72	—	—	72	CID
	GX channels	<sup>(8)</sup>						
CDR PPM	GT channels	—	—	1000	—	—	1000	$\pm$ PPM
	GX channels	<sup>(8)</sup>						
Programmable equalization (AC Gain) <sup>(5)</sup>	GT channels	—	—	14	—	—	14	dB
	GX channels	<sup>(8)</sup>						
Programmable DC gain <sup>(6)</sup>	GT channels	—	—	7.5	—	—	7.5	dB
	GX channels	<sup>(8)</sup>						
Differential on-chip termination resistors <sup>(7)</sup>	GT channels	—	100	—	—	100	—	$\Omega$
<b>Transmitter</b>								
Supported I/O Standards	—	1.4-V and 1.5-V PCML						
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) <sup>(1)</sup>**

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels	(8)						
V <sub>OCM</sub> (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels	(8)						
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels	(8)						
Intra-differential pair skew	GX channels	(8)						
Intra-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)						
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	—	10	—	—	10	μs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post- divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	—	14025	9800	—	12890	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	—	10	—	—	10	μs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 <sup>(23)</sup>	600	—	3250/ 3.125 <sup>(23)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 4 of 4)**

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f <sub>HSDR</sub> (data rate)	SERDES factor J = 3 to 10	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
<b>DPA Mode</b>														
DPA run length	—	—	—	1000 0	—	—	1000 0	—	—	1000 0	—	—	1000 0	UI
<b>Soft CDR mode</b>														
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	—	—	300	± PPM
<b>Non DPA Mode</b>														
Sampling Window	—	—	—	300	—	—	300	—	—	300	—	—	300	ps

**Notes to Table 36:**

- (1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.
- (2) When J = 1 or 2, bypass the SERDES block.
- (3) This only applies to DPA and soft-CDR modes.
- (4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.
- (5) This is achieved by using the **LVDS** clock network.
- (6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (f<sub>OUT</sub>) provided you can close the design timing and the signal integrity simulation is clean.
- (8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.
- (9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
- (10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- (11) The F<sub>MAX</sub> specification is based on the fast clock used for serial data. The interface F<sub>MAX</sub> is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.
- (12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.
- (13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.
- (14) Requires package skew compensation with PCB trace length.
- (15) Do not mix single-ended I/O buffer within LVDS I/O bank.
- (16) Chip-to-chip communication only with a maximum load of 5 pF.
- (17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)**

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

**Notes to Table 40:**

- (1) The typical value equals the average of the minimum and maximum values.
- (2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is  $[625 \text{ ps} + (10 \times 10 \text{ ps}) \pm 20 \text{ ps}] = 725 \text{ ps} \pm 20 \text{ ps}$ .

Table 41 lists the DQS phase shift error for Stratix V devices.

**Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock ( $t_{\text{DQS\_PSERR}}$ ) for Stratix V Devices <sup>(1)</sup>**

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

**Notes to Table 41:**

- (1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is  $\pm 78 \text{ ps}$  or  $\pm 39 \text{ ps}$ .

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices <sup>(1), (Part 1 of 2)</sup> <sup>(2), (3)</sup>**

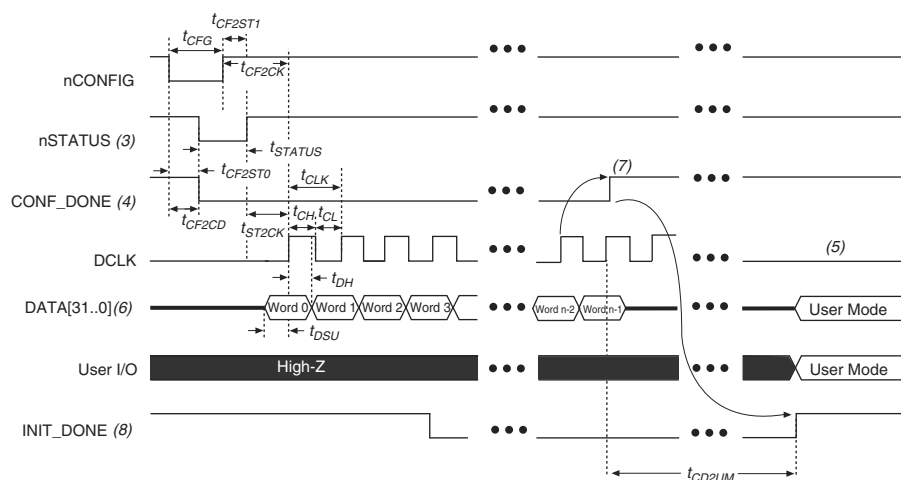
Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Regional	Clock period jitter	$t_{\text{JIT(per)}}$	–50	50	–50	50	–55	55	–55	55	ps
	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	–100	100	–100	100	–110	110	–110	110	ps
	Duty cycle jitter	$t_{\text{JIT(duty)}}$	–50	50	–50	50	–82.5	82.5	–82.5	82.5	ps
Global	Clock period jitter	$t_{\text{JIT(per)}}$	–75	75	–75	75	–82.5	82.5	–82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	–150	150	–150	150	–165	165	–165	165	ps
	Duty cycle jitter	$t_{\text{JIT(duty)}}$	–75	75	–75	75	–90	90	–90	90	ps



## FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

**Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 <sup>(1), (2)</sup>**



### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP x16, use DATA [15..0]. For FPP x8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is 1.

**Table 50. FPP Timing Parameters for Stratix V Devices <sup>(1)</sup>**

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low	—	600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low	—	600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	—	μs
t <sub>STATUS</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μs
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high	—	1,506 <sup>(3)</sup>	μs
t <sub>CF2CK</sub> <sup>(6)</sup>	nCONFIG high to first rising edge on DCLK	1,506	—	μs
t <sub>ST2CK</sub> <sup>(6)</sup>	nSTATUS high to first rising edge of DCLK	2	—	μs
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5	—	ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	—	ns
t <sub>CH</sub>	DCLK high time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CL</sub>	DCLK low time	$0.45 \times 1/f_{\text{MAX}}$	—	s
t <sub>CLK</sub>	DCLK period	$1/f_{\text{MAX}}$	—	s
f <sub>MAX</sub>	DCLK frequency (FPP $\times 8/\times 16$ )	—	125	MHz
	DCLK frequency (FPP $\times 32$ )	—	100	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(4)</sup>	175	437	μs
t <sub>CD2CU</sub>	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t <sub>CD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	t <sub>CD2CU</sub> + (8576 × CLKUSR period) <sup>(5)</sup>	—	—

**Notes to Table 50:**

- (1) Use these timing parameters when the decompression and design security features are disabled.
- (2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.



**Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)**

Parameter (1)	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	I2	I3, I3YY	I4	Unit
D3	8	0	1.587	1.699	2.793	2.793	2.992	3.192	2.811	3.047	3.257	ns
D4	64	0	0.464	0.492	0.838	0.838	0.924	1.011	0.843	0.920	1.006	ns
D5	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D6	32	0	0.229	0.244	0.415	0.415	0.458	0.503	0.418	0.456	0.499	ns

**Notes to Table 58:**

- (1) You can set this value in the Quartus II software by selecting **D1, D2, D3, D5, and D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

## Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

**Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)**

Symbol	Parameter	Typical	Unit
D <sub>OUTBUF</sub>	Rising and/or falling edge delay	0 (default)	ps
		25	ps
		50	ps
		75	ps

**Note to Table 59:**

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

## Glossary

Table 60 lists the glossary for this chapter.

**Table 60. Glossary (Part 1 of 4)**

Letter	Subject	Definitions
A	—	—
B		
C		
D	—	—
E	—	—
F	f <sub>HCLK</sub>	Left and right PLL input clock frequency.
	f <sub>HSDR</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDR</sub> = 1/TUI), non-DPA.
	f <sub>HSDRDPA</sub>	High-speed I/O block—Maximum and minimum <b>LVDS</b> data transfer rate (f <sub>HSDRDPA</sub> = 1/TUI), DPA.

Table 60. Glossary (Part 2 of 4)

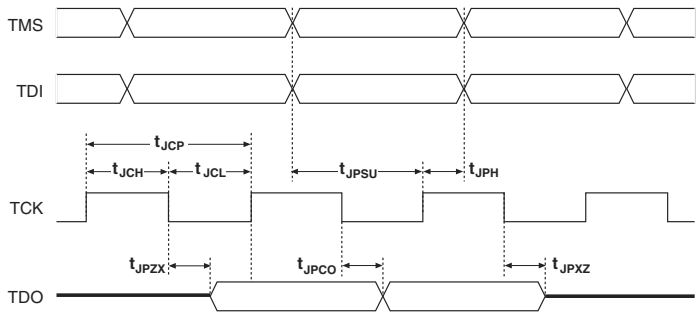
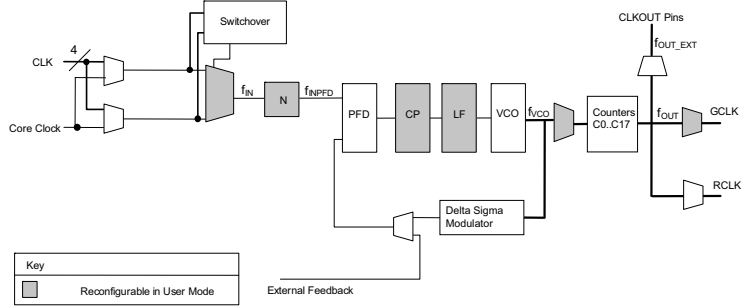
Letter	Subject	Definitions
G H I	—	—
J	JTAG Timing Specifications	<p>High-speed I/O block—Deserialization factor (width of parallel data bus).</p> <p>JTAG Timing Specifications:</p> 
K L M N O	—	—
P	PLL Specifications	<p><b>Diagram of PLL Specifications <sup>(1)</sup></b></p>  <p><b>Note:</b> (1) Core Clock can only be fed by dedicated clock input pins or PLL outputs.</p>
Q	—	—
R	R <sub>L</sub>	Receiver differential input discrete resistor (external to the Stratix V device).

Table 60. Glossary (Part 3 of 4)

Letter	Subject	Definitions
S	SW (sampling window)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p> 
	Single-ended voltage referenced I/O standard	<p>The JEDEC standard for <b>SSTL</b> and <b>HSTL</b> I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p> 
T	$t_c$	High-speed receiver and transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including $t_{CO}$ variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under <b>SW</b> in this table).
	$t_{DUTY}$	<p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p><b>Timing Unit Interval (TUI)</b></p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = <math>1/(\text{receiver input clock frequency multiplication factor}) = t_c/w</math>)</p>
	$t_{FALL}$	Signal high-to-low transition time (80-20%)
	$t_{INCCJ}$	Cycle-to-cycle jitter tolerance on the PLL clock input.
	$t_{OUTPJ\_IO}$	Period jitter on the general purpose I/O driven by a PLL.
	$t_{OUTPJ\_DC}$	Period jitter on the dedicated clock output driven by a PLL.
	$t_{RISE}$	Signal low-to-high transition time (20-80%)
U	—	—

**Table 60. Glossary (Part 4 of 4)**

Letter	Subject	Definitions
<b>V</b>	$V_{CM(DC)}$	DC common mode input voltage.
	$V_{ICM}$	Input common mode voltage—The common mode of the differential signal at the receiver.
	$V_{ID}$	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	$V_{IH}$	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	$V_{IL}$	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	$V_{OCM}$	Output common mode voltage—The common mode of the differential signal at the transmitter.
	$V_{OD}$	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	$V_{SWING}$	Differential input voltage
	$V_X$	Input differential cross point voltage
	$V_{OX}$	Output differential cross point voltage
<b>W</b>	W	High-speed I/O block—clock boost factor
<b>X</b>	—	—
<b>Y</b>		
<b>Z</b>		

**Table 61. Document Revision History (Part 2 of 3)**

Date	Version	Changes
November 2014	3.3	<ul style="list-style-type: none"> <li>■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> <li>■ Added the I3YY speed grade to the <math>V_{CC}</math> description in Table 6.</li> <li>■ Added the I3YY speed grade to <math>V_{CCHIP\_L}</math>, <math>V_{CCHIP\_R}</math>, <math>V_{CCHSSI\_L}</math>, and <math>V_{CCHSSI\_R}</math> descriptions in Table 7.</li> <li>■ Added 240-<math>\Omega</math> to Table 11.</li> <li>■ Changed CDR PPM tolerance in Table 23.</li> <li>■ Added additional max data rate for fPLL in Table 23.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> <li>■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> <li>■ Changed CDR PPM tolerance in Table 28.</li> <li>■ Added additional max data rate for fPLL in Table 28.</li> <li>■ Changed the mode descriptions for MLAB and M20K in Table 33.</li> <li>■ Changed the Max value of <math>f_{HCLK\_OUT}</math> for the C2, C2L, I2, I2L speed grades in Table 36.</li> <li>■ Changed the frequency ranges for C1 and C2 in Table 39.</li> <li>■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> <li>■ Added note about nSTATUS to Table 50, Table 51, Table 54.</li> <li>■ Changed the available settings in Table 58.</li> <li>■ Changed the note in “Periphery Performance”.</li> <li>■ Updated the “I/O Standard Specifications” section.</li> <li>■ Updated the “Raw Binary File Size” section.</li> <li>■ Updated the receiver voltage input range in Table 22.</li> <li>■ Updated the max frequency for the LVDS clock network in Table 36.</li> <li>■ Updated the DCLK note to Figure 11.</li> <li>■ Updated Table 23 <math>VO_{CM}</math> (DC Coupled) condition.</li> <li>■ Updated Table 6 and Table 7.</li> <li>■ Added the DCLK specification to Table 55.</li> <li>■ Updated the notes for Table 47.</li> <li>■ Updated the list of parameters for Table 56.</li> </ul>
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	<ul style="list-style-type: none"> <li>■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> <li>■ Added Figure 1 and Figure 3</li> <li>■ Added the “Transceiver Characterization” section</li> <li>■ Removed all “Preliminary” designations.</li> </ul>