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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	552
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma7h3f35i3

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCD_FPLL}	PLL digital power supply	0.5	1.8	V
V_{CCA_FPLL}	PLL analog power supply	0.5	3.4	V
V_I	DC input voltage	0.5	3.8	V
T_J	Operating junction temperature	55	125	°C
T_{STG}	Storage temperature (No bias)	65	150	°C
I_{OUT}	DC output current per pin	25	40	mA

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	0.5	3.75	V
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	0.5	1.35	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	0.5	1.35	V
V_{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	0.5	1.35	V
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	0.5	1.35	V
V_{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to 2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

Table 5. Maximum Allowed Overshoot During Transitions

Symbol	Description	Condition (V)	Overshoot Duration as % @ T_J = 100°C	Unit
Vi (AC)	AC input voltage	3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
		4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Figure 1. Stratix V Device Overshoot Duration

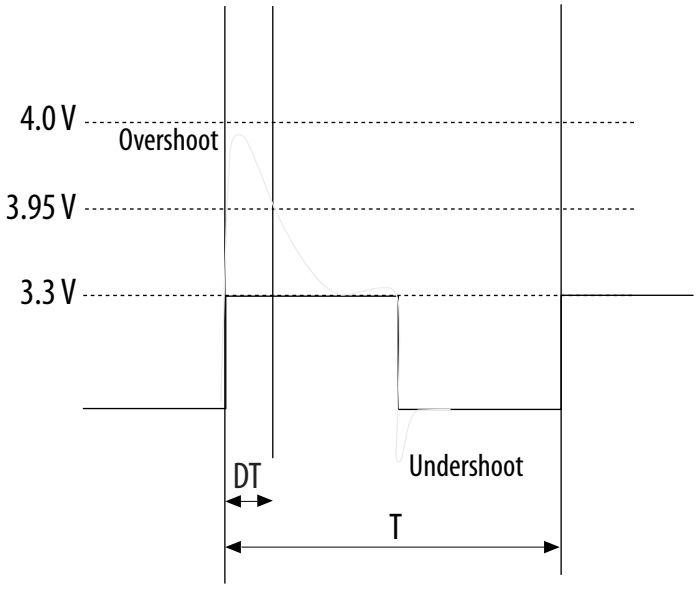

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB (2)	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: Data rate > 10.3 Gbps. DFE is used.	All	1.05	3.0	1.5	V
If ANY of the following conditions are true (1): ATX PLL is used. Data rate > 6.5Gbps. DFE (data rate > 10.3 Gbps), AEQ, or EyeQ feature is used.	All	1.0			
If ALL of the following conditions are true: ATX PLL is not used. Data rate ≤ 6.5Gbps. DFE, AEQ, and EyeQ are not used.	C1, C2, I2, and I3YY	0.90	2.5		
	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		

Notes to Table 8

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

f For more information about power estimation tools, refer to the PowerPlay Early Power Estimator User Guide and the PowerPlay Power Analysis chapter in the Quartus II Handbook.

1 You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

f For more information about power estimation tools, refer to the PowerPlay Early Power Estimator User Guide and the PowerPlay Power Analysis chapter in the Quartus II Handbook.

Table 24 shows the maximum transmitter da ta rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications (1)

Clock Network	ATX PLL			CMU PLL (2)			fPLL		
	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span	Non-bonded Mode (Gbps)	Bonded Mode (Gbps)	Channel Span
x1 (3)	14.1		6	12.5		6	3.125		3
x6 (3)		14.1	6		12.5	6	3.125		6
x6 PLL Feedback (4)		14.1	Side-wide		12.5	Side-wide			
xN (PCIe)		8.0	8		5.0	8			
xN (Native PHY IP)	8.0	8.0	Up to 13 channels above and below PLL	7.99	7.99	Up to 13 channels above and below PLL	3.125	3.125	Up to 13 channels above and below PLL
		8.01 to 9.8304	Up to 7 channels above and below PLL						

Notes to Table 24

(1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.

(2) ATX PLL is recommended at 8 Gbps and below data rates for improved jitter performance.

(3) Channel span is within a transceiver bank.

(4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 26 shows the approximate maximum data rate using the 10G PCS.

Table 26. Stratix V 10G PCS Approximate Maximum Data Rate (1)

Mode (2)	Transceiver Speed Grade	PMA Width	64	40	40	40	32	32
		PCS Width	64	66/67	50	40	64/66/67	32
FIFO or Register	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5
		C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88
	3	C1, C2, C2L, I2, I2L core speed grade	8.5 Gbps					
		C3, I3, I3L core speed grade						
		C4, I4 core speed grade						
		I3YY core speed grade	10.3125 Gbps					

Notes to Table 26

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Figure 4 shows the differential transmitter output waveform.

Figure 4. Differential Transmitter/Receiver Output/Input Waveform

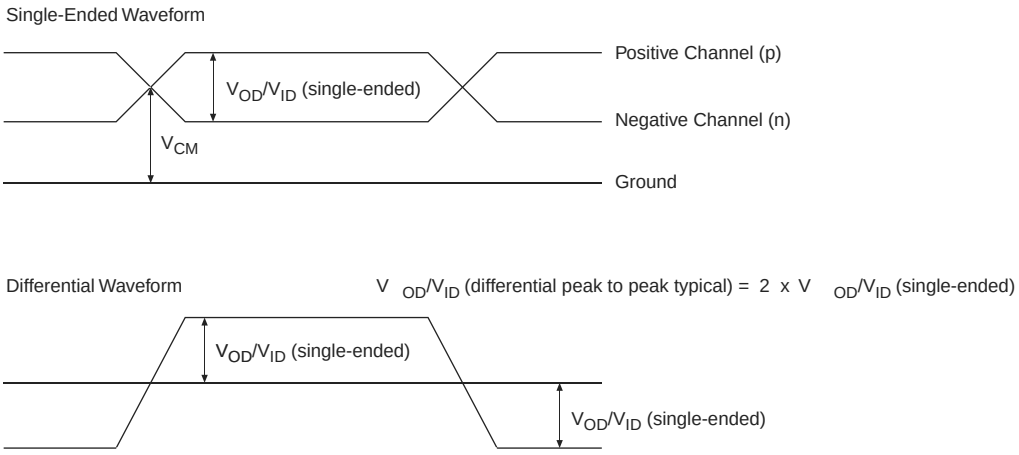

Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-V LVTTL/LVCMOS are capable of a typical 167 MHz and 1.2-V LVCMOS at 100 MHz interfacing frequency with a 10 pF load.

1 The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1) (2) (Part 1 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (4)	5		800	5		800	5		625	5		525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (3)	Clock boost factor W = 1 to 40 (4)	5		800	5		800	5		625	5		525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 (4)	5		520	5		520	5		420	5		420	MHz
f_{HSCLK_OUT} (output clock frequency)		5		800	5		800	5		625 (5)	5		525 (5)	MHz

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f_{HSDR}(data rate)	SERDES factor J = 3 to 10 (9), (11), (12), (13), (14), (15), (16)	(6)		1600	(6)		1434	(6)		1250	(6)		1050	Mbps
	SERDES factor J = 4 LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)		1250	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)		(7)	(6)		(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)		(7)	(6)		(7)	(6)		(7)	(6)		(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR}(data rate) (10)	SERDES factor J = 4 to 10 (17)	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
$t_{x\ Jitter}$- True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps			160		160			160			160		ps
	Total Jitter for Data Rate < 600 Mbps			0.1		0.1			0.1			0.1		UI
$t_{x\ Jitter}$- Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps			300		300			300			325		ps
	Total Jitter for Data Rate < 600 Mbps			0.2		0.2			0.2			0.25		UI

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) (4), (5)
Stratix V GX	5SGXA3	H35, F40, F35 (2)	213,798,880	562,392
		H29, F35 (3)	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528