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Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma7k2f40c2n

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min ⁽⁴⁾	Typ	Max ⁽⁴⁾	Unit
V _{CC}	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	—	0.87	0.9	0.93	V
	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾	—	0.82	0.85	0.88	V
V _{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V _{CCPD} ⁽¹⁾	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V _{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V _{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V _{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V _{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V _{CCBAT} ⁽²⁾	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V _I	DC input voltage	—	−0.5	—	3.6	V
V _O	Output voltage	—	0	—	V _{CCIO}	V
T _J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	−40	—	100	°C

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices ⁽¹⁾

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	$V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$	-30	—	30	μA

Note to Table 9:

(1) If $V_O = V_{CCIO}$ to $V_{CCIO\text{MAX}}$, 100 μA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

Parameter	Symbol	Conditions	V _{CCIO}										Unit
			1.2 V		1.5 V		1.8 V		2.5 V		3.0 V		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	−22.5	—	−25.0	—	−30.0	—	−50.0	—	−70.0	—	μA
Low overdrive current	I _{ODL}	0V < V _{IN} < V _{CCIO}	—	120	—	160	—	200	—	300	—	500	μA
High overdrive current	I _{ODH}	0V < V _{IN} < V _{CCIO}	—	−120	—	−160	—	−200	—	−300	—	−500	μA
Bus-hold trip point	V _{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

Symbol	Description	Conditions	Calibration Accuracy				Unit
			C1	C2,I2	C3,I3, I3YY	C4,I4	
25- Ω R_S	Internal series termination with calibration (25- Ω setting)	$V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$	± 15	± 15	± 15	± 15	%

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices ^{(1), (2)}

Symbol	Description	V _{CCIO} Conditions (V) ⁽³⁾	Value ⁽⁴⁾	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V _{CCIO} (V)			V _{IL} (V)		V _{IH} (V)		V _{OL} (V)	V _{OH} (V)	I _{OL} (mA)	I _{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTTL	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.4	2.4	2	−2
LVC MOS	2.85	3	3.15	−0.3	0.8	1.7	3.6	0.2	V _{CCIO} − 0.2	0.1	−0.1
2.5 V	2.375	2.5	2.625	−0.3	0.7	1.7	3.6	0.4	2	1	−1
1.8 V	1.71	1.8	1.89	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.45	V _{CCIO} − 0.45	2	−2
1.5 V	1.425	1.5	1.575	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	−2
1.2 V	1.14	1.2	1.26	−0.3	0.35 * V _{CCIO}	0.65 * V _{CCIO}	V _{CCIO} + 0.3	0.25 * V _{CCIO}	0.75 * V _{CCIO}	2	−2

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 1 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾	—	40	—	710	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾	—	100	—	710	100	—	710	100	—	710	MHz
Rise time	Measure at ±60 mV of differential signal ⁽²⁶⁾	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal ⁽²⁶⁾	—	—	400	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 2 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to -0.5	—	—	0 to -0.5	—	—	0 to -0.5	—	%
On-chip termination resistors ⁽²¹⁾	—	—	100	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} ⁽⁵⁾	Dedicated reference clock pin	—	—	1.6	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	-0.4	—	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled) ⁽³⁾	Dedicated reference clock pin	1050/1000/900/850 ⁽²⁾			1050/1000/900/850 ⁽²⁾			1050/1000/900/850 ⁽²⁾			mV
	RX reference clock pin	1.0/0.9/0.85 ⁽⁴⁾			1.0/0.9/0.85 ⁽⁴⁾			1.0/0.9/0.85 ⁽⁴⁾			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) ⁽²⁰⁾	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥ 1 MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁷⁾	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)
R_{REF} ⁽¹⁹⁾	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	—	1800 $\pm 1\%$	—	Ω
Transceiver Clocks											
fixedclk clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	—	100 or 125	—	MHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors ⁽²¹⁾	85- Ω setting	—	85 \pm 30%	—	—	85 \pm 30%	—	—	85 \pm 30%	—	Ω
	100- Ω setting	—	100 \pm 30%	—	—	100 \pm 30%	—	—	100 \pm 30%	—	Ω
	120- Ω setting	—	120 \pm 30%	—	—	120 \pm 30%	—	—	120 \pm 30%	—	Ω
	150- Ω setting	—	150 \pm 30%	—	—	150 \pm 30%	—	—	150 \pm 30%	—	Ω
V_{ICM} (AC and DC coupled)	$V_{CCR_GXB} = 0.85\text{ V}$ or 0.9 V full bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 0.85\text{ V}$ or 0.9 V half bandwidth	—	600	—	—	600	—	—	600	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}/1.05\text{ V}$ full bandwidth	—	700	—	—	700	—	—	700	—	mV
	$V_{CCR_GXB} = 1.0\text{ V}$ half bandwidth	—	750	—	—	750	—	—	750	—	mV
t_{LTR} ⁽¹¹⁾	—	—	—	10	—	—	10	—	—	10	μs
t_{LTD} ⁽¹²⁾	—	4	—	—	4	—	—	4	—	—	μs
t_{LTD_manual} ⁽¹³⁾	—	4	—	—	4	—	—	4	—	—	μs
$t_{LTR_LTD_manual}$ ⁽¹⁴⁾	—	15	—	—	15	—	—	15	—	—	μs
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (AC Gain) ⁽¹⁰⁾	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB

Figure 2 shows the differential transmitter output waveform.

Figure 2. Differential Transmitter Output Waveform



Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)



Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) ⁽¹⁾

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to −0.5	—	—	0 to −0.5	—	%
On-chip termination resistors ⁽¹⁹⁾	—	—	100	—	—	100	—	Ω
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V _{MIN}	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V _{ICM} (AC coupled)	Dedicated reference clock pin	1050/1000 ⁽²⁾			1050/1000 ⁽²⁾			mV
	RX reference clock pin	1.0/0.9/0.85 ⁽²²⁾			1.0/0.9/0.85 ⁽²²⁾			V
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Figure 4 shows the differential transmitter output waveform.

Figure 4. Differential Transmitter/Receiver Output/Input Waveform



Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Table 33. Memory Block Performance Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
M20K Block	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	0	1	525	525	455	400	525	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Notes to Table 33:

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.
- (3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

Description	Min	Typ	Max	Unit
I _{bias} , diode source current	8	—	200	μA
V _{bias} , voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface.

General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.



The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\text{HCLK_in}}$ (input clock frequency) True Differential I/O Standards	Clock boost factor $W = 1$ to 40 ⁽⁴⁾	5	—	800	5	—	800	5	—	625	5	—	525	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards ⁽³⁾	Clock boost factor $W = 1$ to 40 ⁽⁴⁾	5	—	800	5	—	800	5	—	625	5	—	525	MHz
$f_{\text{HCLK_in}}$ (input clock frequency) Single Ended I/O Standards	Clock boost factor $W = 1$ to 40 ⁽⁴⁾	5	—	520	5	—	520	5	—	420	5	—	420	MHz
$f_{\text{HCLK_OUT}}$ (output clock frequency)	—	5	—	800	5	—	800	5	—	625 ⁽⁵⁾	5	—	525 ⁽⁵⁾	MHz

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 3 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	160	—	—	160	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	250	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	—	—	300	ps
Receiver														
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 ^{(11), (12), (13), (14), (15), (16)}	150	—	1434	150	—	1434	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4	150	—	1600	150	—	1600	150	—	1600	150	—	1250	Mbps
	LVDS RX with DPA ^{(12), (14), (15), (16)}	150	—	1600	150	—	1600	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	⁽⁶⁾	—	⁽⁷⁾	⁽⁶⁾	—	⁽⁷⁾	⁽⁶⁾	—	⁽⁷⁾	⁽⁶⁾	—	⁽⁷⁾	Mbps
	SERDES factor J = 1, uses SDR Register	⁽⁶⁾	—	⁽⁷⁾	⁽⁶⁾	—	⁽⁷⁾	⁽⁶⁾	—	⁽⁷⁾	⁽⁶⁾	—	⁽⁷⁾	Mbps

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 4 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HSDR} (data rate)	SERDES factor J = 3 to 10	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	(6)	—	(8)	Mbps
	SERDES factor J = 2, uses DDR Registers	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	(6)	—	(7)	Mbps
DPA Mode														
DPA run length	—	—	—	1000 0	—	—	1000 0	—	—	1000 0	—	—	1000 0	UI
Soft CDR mode														
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	—	—	300	± PPM
Non DPA Mode														
Sampling Window	—	—	—	300	—	—	300	—	—	300	—	—	300	ps

Notes to Table 36:

- (1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.
- (2) When J = 1 or 2, bypass the SERDES block.
- (3) This only applies to DPA and soft-CDR modes.
- (4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.
- (5) This is achieved by using the **LVDS** clock network.
- (6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.
- (8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.
- (9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
- (10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- (11) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.
- (12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.
- (13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.
- (14) Requires package skew compensation with PCB trace length.
- (15) Do not mix single-ended I/O buffer within LVDS I/O bank.
- (16) Chip-to-chip communication only with a maximum load of 5 pF.
- (17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices ⁽¹⁾, (Part 2 of 2) ⁽²⁾, ⁽³⁾

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

Notes to Table 42:

- (1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.
- (2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.
- (3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the <code>dyn_term_ctrl</code> and <code>oe</code> signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the `oe` and `dyn_term_ctrl` signals.

Figure 10. Timing Diagram for `oe` and `dyn_term_ctrl` Signals

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 ⁽¹⁾	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 ⁽¹⁾	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 ⁽¹⁾	ns

Notes to Table 46:

- (1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
Stratix V GX	5SGXA3	H35, F40, F35 ⁽²⁾	213,798,880	562,392
		H29, F35 ⁽³⁾	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) ^{(4), (5)}
Stratix V E ⁽¹⁾	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

Notes to Table 47:

- (1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.
- (2) 36-transceiver devices.
- (3) 24-transceiver devices.
- (4) File size for the periphery image.
- (5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.tff) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.



For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Variant	Member Code	Active Serial ⁽¹⁾			Fast Passive Parallel ⁽²⁾		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GX	A3	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	A4	4	100	0.534	32	100	0.067
	A5	4	100	0.675	32	100	0.084
	A7	4	100	0.675	32	100	0.084
	A9	4	100	0.857	32	100	0.107
	AB	4	100	0.857	32	100	0.107
	B5	4	100	0.676	32	100	0.085
	B6	4	100	0.676	32	100	0.085
	B9	4	100	0.857	32	100	0.107
	BB	4	100	0.857	32	100	0.107
GT	C5	4	100	0.675	32	100	0.084
	C7	4	100	0.675	32	100	0.084

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Variant	Member Code	Active Serial ⁽¹⁾			Fast Passive Parallel ⁽²⁾		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GS	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
E	E9	4	100	0.857	32	100	0.107
	EB	4	100	0.857	32	100	0.107

Notes to Table 48:

- (1) DCLK frequency of 100 MHz using external CLKUSR.
 (2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different DCLK-to-DATA [] ratio when you enable the design security, decompression, or both features. Table 49 lists the DCLK-to-DATA [] ratio for each combination.

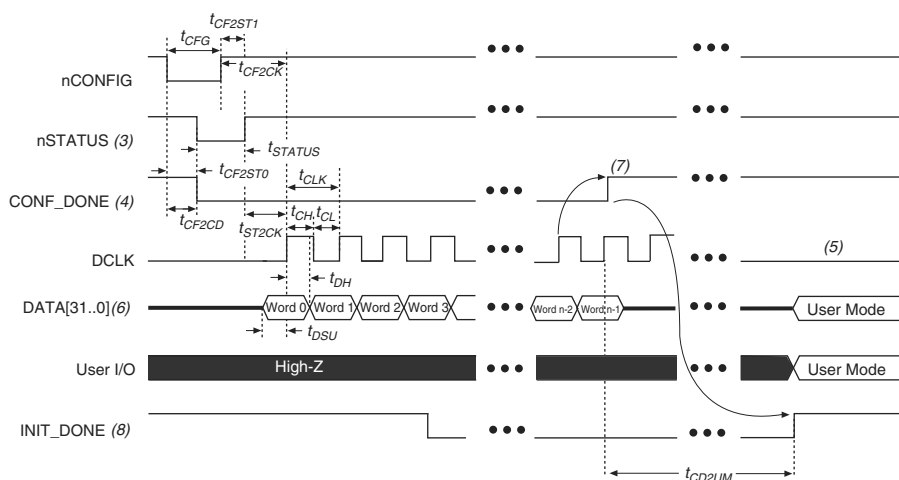
Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 1 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

FPP Configuration Timing when DCLK-to-DATA [] = 1

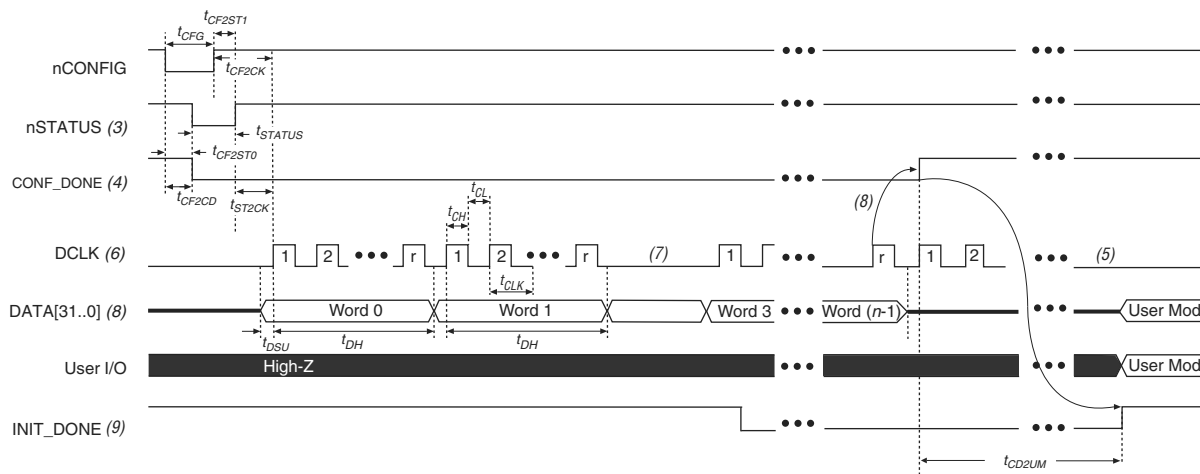
Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 ^{(1), (2)}



Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP $\times 16$, use DATA [15..0]. For FPP $\times 8$, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Figure 13. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 (1), (2)**Notes to Figure 13:**

- (1) Use this timing waveform and parameters when the DCLK-to-DATA[] ratio is >1. To find out the DCLK-to-DATA[] ratio for your system, refer to Table 49 on page 55.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time as specified by the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 49 on page 55.
- (7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[31..0] pins prior to sending the first DCLK rising edge.
- (8) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme ^{(1), (2)}

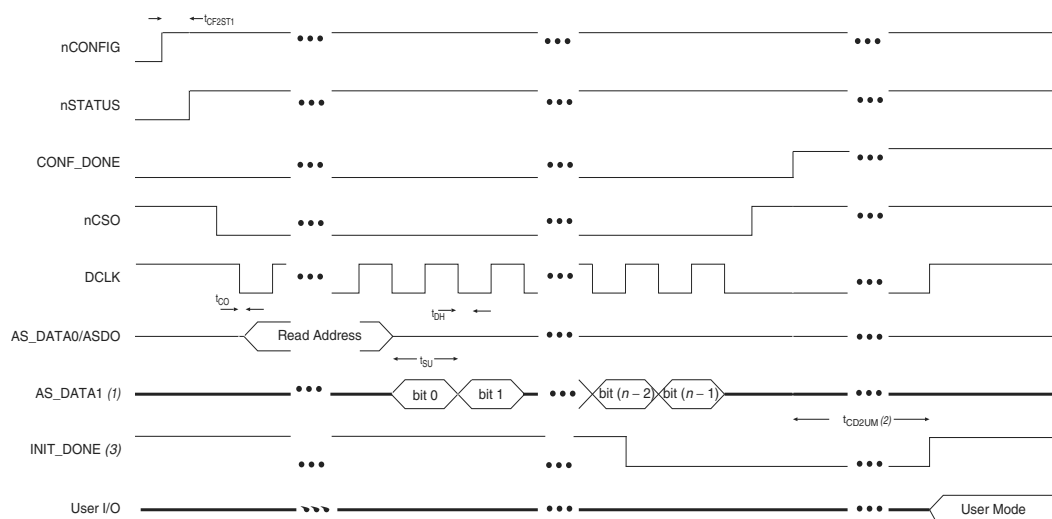
Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing



Notes to Figure 14:

- (1) If you are using AS ×4 mode, this signal represents the AS_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t_H	Data hold time after falling edge on DCLK	0	—	ns