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## Understanding [Embedded - FPGAs (Field Programmable Gate Array)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

## Details

| | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 234720 |
| Number of Logic Elements/Cells | 622000 |
| Total RAM Bits | 51200000 |
| Number of I/O | 696 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-FBGA (40x40) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxma7k2f40i3 |

**Table 6. Recommended Operating Conditions for Stratix V Devices  (Part 2 of 2)**

| Symbol | Description | Condition | Min [4] | Typ | Max [4] | Unit |
|---|---|---|---|---|---|---|
| $t_{RAMP}$ | Power supply ramp time | Standard POR | 200 µs | — | 100 ms | — |
|  |  | Fast POR | 200 µs | — | 4 ms | — |

**Notes to Table 6:**

(1)  $V_{CCPD}$ must be 2.5 V when $V_{CCIO}$ is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. $V_{CCPD}$ must be 3.0 V when $V_{CCIO}$ is 3.0 V.

(2)  If you do not use the design security feature in Stratix V devices, connect $V_{CCBAT}$ to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors $V_{CCBAT}$. Stratix V devices will not exit POR if $V_{CCBAT}$ stays at logic low.

(3)  C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4)  The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

**Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)**

| Symbol | Description | Devices | Minimum [4] | Typical | Maximum [4] | Unit |
|---|---|---|---|---|---|---|
| $V_{CCA\_GXBL}$ [1], [3] | Transceiver channel PLL power supply (left side) | GX, GS, GT | 2.85 | 3.0 | 3.15 | V |
|  |  |  | 2.375 | 2.5 | 2.625 |  |
| $V_{CCA\_GXBR}$ [1], [3] | Transceiver channel PLL power supply (right side) | GX, GS | 2.85 | 3.0 | 3.15 | V |
|  |  |  | 2.375 | 2.5 | 2.625 |  |
| $V_{CCA\_GTBR}$ | Transceiver channel PLL power supply (right side) | GT | 2.85 | 3.0 | 3.15 | V |
| $V_{CCHIP\_L}$ | Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
|  | Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHIP\_R}$ | Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
|  | Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_L}$ | Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
|  | Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCHSSI\_R}$ | Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades) | GX, GS, GT | 0.87 | 0.9 | 0.93 | V |
|  | Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| $V_{CCR\_GXBL}$ [2] | Receiver analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
|  |  |  | 0.87 | 0.90 | 0.93 |  |
|  |  |  | 0.97 | 1.0 | 1.03 |  |
|  |  |  | 1.03 | 1.05 | 1.07 |  |

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8.  Transceiver Power Supply Voltage Requirements**

| Conditions | Core Speed Grade | VCCR_GXB & VCCT_GXB [(2)] | VCCA_GXB | VCCH_GXB | Unit |
|---|---|---|---|---|---|
| If BOTH of the following conditions are true:<br>■ Data rate > 10.3 Gbps.<br>■ DFE is used. | All | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true [(1)]:<br>■ ATX PLL is used.<br>■ Data rate > 6.5Gbps.<br>■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | All | 1.0 | | | |
| If ALL of the following conditions are true:<br>■ ATX PLL is not used.<br>■ Data rate ≤ 6.5Gbps.<br>■ DFE, AEQ, and EyeQ are not used. | C1, C2, I2, and I3YY | 0.90 | 2.5 | | |
| | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85 | 2.5 | | |

**Notes to Table 8:**

(1)  Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2)  If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

## DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

### Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

**Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices  (Part 2 of 2)**

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|--------|-------------|-----------|------|------|------|------|------|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 50-Ω $R_S$ | Internal series termination without calibration (50-Ω setting) | $V_{CCIO}$ = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |
| 100-Ω $R_D$ | Internal differential termination (100-Ω setting) | $V_{CCPD}$ = 2.5 V | ±25 | ±25 | ±25 | ±25 | % |

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

**Equation 1.  OCT Variation Without Recalibration for Stratix V Devices** [1], [2], [3], [4], [5], [6]

$$R_{OCT} = R_{SCAL}\Big(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\Big)$$

**Notes to Equation 1:**

(1)  The $R_{OCT}$ value shows the range of OCT resistance with the variation of temperature and $V_{CCIO}$.
(2)  $R_{SCAL}$ is the OCT resistance value at power-up.
(3)  ΔT is the variation of temperature with respect to the temperature at power-up.
(4)  ΔV is the variation of voltage with respect to the $V_{CCIO}$ at power-up.
(5)  dR/dT is the percentage change of $R_{SCAL}$ with temperature.
(6)  dR/dV is the percentage change of $R_{SCAL}$ with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

**Table 13.  OCT Variation after Power-Up Calibration for Stratix V Devices  (Part 1 of 2)** [1]

| Symbol | Description | $V_{CCIO}$ (V) | Typical | Unit |
|--------|-------------|------|---------|------|
| dR/dV | OCT variation with voltage without recalibration | 3.0 | 0.0297 | %/mV |
| | | 2.5 | 0.0344 | |
| | | 1.8 | 0.0499 | |
| | | 1.5 | 0.0744 | |
| | | 1.2 | 0.1241 | |

### Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

**Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices** [1], [2]

| Symbol | Description | $V_{CCIO}$ Conditions (V) [3] | Value [4] | Unit |
|--------|-------------|------------------------------|-----------|------|
| $R_{PU}$ | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

**Notes to Table 16:**

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than $V_{CCIO}$.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

### I/O Standard Specifications

Table 17 through Table 22 list the input voltage ($V_{IH}$ and $V_{IL}$), output voltage ($V_{OH}$ and $V_{OL}$), and current drive characteristics ($I_{OH}$ and $I_{OL}$) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The $V_{OL}$ and $V_{OH}$ values are valid at the corresponding $I_{OH}$ and $I_{OL}$, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

**Table 17. Single-Ended I/O Standards for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{IL}$ (V) | | $V_{IH}$ (V) | | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{OL}$ (mA) | $I_{OH}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTL | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | −2 |
| LVCMOS | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.2 | $V_{CCIO} - 0.2$ | 0.1 | −0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | −0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | −1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | −0.3 | $0.35 * V_{CCIO}$ | $0.65 * V_{CCIO}$ | $V_{CCIO} + 0.3$ | 0.45 | $V_{CCIO} - 0.45$ | 2 | −2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | −0.3 | $0.35 * V_{CCIO}$ | $0.65 * V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 * V_{CCIO}$ | $0.75 * V_{CCIO}$ | 2 | −2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | −0.3 | $0.35 * V_{CCIO}$ | $0.65 * V_{CCIO}$ | $V_{CCIO} + 0.3$ | $0.25 * V_{CCIO}$ | $0.75 * V_{CCIO}$ | 2 | −2 |

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{REF}$ (V) | | | $V_{TT}$ (V) | | |
|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | $V_{REF}$ − 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.833 | 0.9 | 0.969 | $V_{REF}$ − 0.04 | $V_{REF}$ | $V_{REF}$ + 0.04 |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.418 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| SSTL-12 Class I, II | 1.14 | 1.20 | 1.26 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | 0.49 * $V_{CCIO}$ | 0.5 * VCCIO | 0.51 * $V_{CCIO}$ |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.85 | 0.9 | 0.95 | — | $V_{CCIO}$/2 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.68 | 0.75 | 0.9 | — | $V_{CCIO}$/2 | — |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.47 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.53 * $V_{CCIO}$ | — | $V_{CCIO}$/2 | — |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.49 * $V_{CCIO}$ | 0.5 * $V_{CCIO}$ | 0.51 * $V_{CCIO}$ | — | — | — |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | $V_{OL}$ (V) | $V_{OH}$ (V) | $I_{ol}$ (mA) | $I_{oh}$ (mA) |
|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| SSTL-2 Class I | −0.3 | $V_{REF}$ − 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ − 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ − 0.608 | $V_{TT}$ + 0.608 | 8.1 | −8.1 |
| SSTL-2 Class II | −0.3 | $V_{REF}$ − 0.15 | $V_{REF}$ + 0.15 | $V_{CCIO}$ + 0.3 | $V_{REF}$ − 0.31 | $V_{REF}$ + 0.31 | $V_{TT}$ − 0.81 | $V_{TT}$ + 0.81 | 16.2 | −16.2 |
| SSTL-18 Class I | −0.3 | $V_{REF}$ − 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ − 0.25 | $V_{REF}$ + 0.25 | $V_{TT}$ − 0.603 | $V_{TT}$ + 0.603 | 6.7 | −6.7 |
| SSTL-18 Class II | −0.3 | $V_{REF}$ − 0.125 | $V_{REF}$ + 0.125 | $V_{CCIO}$ + 0.3 | $V_{REF}$ − 0.25 | $V_{REF}$ + 0.25 | 0.28 | $V_{CCIO}$ − 0.28 | 13.4 | −13.4 |
| SSTL-15 Class I | — | $V_{REF}$ − 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ − 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 8 | −8 |
| SSTL-15 Class II | — | $V_{REF}$ − 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ − 0.175 | $V_{REF}$ + 0.175 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | 16 | −16 |
| SSTL-135 Class I, II | — | $V_{REF}$ − 0.09 | $V_{REF}$ + 0.09 | — | $V_{REF}$ − 0.16 | $V_{REF}$ + 0.16 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-125 Class I, II | — | $V_{REF}$ − 0.85 | $V_{REF}$ + 0.85 | — | $V_{REF}$ − 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |
| SSTL-12 Class I, II | — | $V_{REF}$ − 0.1 | $V_{REF}$ + 0.1 | — | $V_{REF}$ − 0.15 | $V_{REF}$ + 0.15 | 0.2 * $V_{CCIO}$ | 0.8 * $V_{CCIO}$ | — | — |

**Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)**

| I/O Standard | $V_{CCIO}$ (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.16 | $V_{CCIO}$ + 0.3 | — | 0.5* $V_{CCIO}$ | — | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.3 | $V_{CCIO}$ + 0.48 |
| HSUL-12 | 1.14 | 1.2 | 1.3 | 0.26 | 0.26 | 0.5* $V_{CCIO}$ − 0.12 | 0.5* $V_{CCIO}$ | 0.5* $V_{CCIO}$ + 0.12 | 0.4* $V_{CCIO}$ | 0.5* $V_{CCIO}$ | 0.6* $V_{CCIO}$ | 0.44 | 0.44 |

**Table 22. Differential I/O Standard Specifications for Stratix V Devices [7]**

| I/O Standard | $V_{CCIO}$ (V) [10] | | | $V_{ID}$ (mV) [8] | | | $V_{ICM(DC)}$ (V) | | | $V_{OD}$ (V) [6] | | | $V_{OCM}$ (V) [6] | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | Min | Typ | Max | Min | Condition | Max | Min | Condition | Max | Min | Typ | Max | Min | Typ | Max |
| PCML | Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18. | | | | | | | | | | | | | | |
| 2.5 V LVDS [1] | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.05 | $D_{MAX} \leq$ 700 Mbps | 1.8 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| | | | | | | — | 1.05 | $D_{MAX} >$ 700 Mbps | 1.55 | 0.247 | — | 0.6 | 1.125 | 1.25 | 1.375 |
| BLVDS [5] | 2.375 | 2.5 | 2.625 | 100 | — | — | — | — | — | — | — | — | — | — | — |
| RSDS (HIO) [2] | 2.375 | 2.5 | 2.625 | 100 | $V_{CM}$ = 1.25 V | — | 0.3 | — | 1.4 | 0.1 | 0.2 | 0.6 | 0.5 | 1.2 | 1.4 |
| Mini-LVDS (HIO) [3] | 2.375 | 2.5 | 2.625 | 200 | — | 600 | 0.4 | — | 1.325 | 0.25 | — | 0.6 | 1 | 1.2 | 1.4 |
| LVPECL [4], [9] | — | — | — | 300 | — | — | 0.6 | $D_{MAX} \leq$ 700 Mbps | 1.8 | — | — | — | — | — | — |
| | — | — | — | 300 | — | — | 1 | $D_{MAX} >$ 700 Mbps | 1.6 | — | — | — | — | — | — |

**Notes to Table 22:**

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed $V_{ICM}$, $V_{OD}$, and $V_{OCM}$ specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110 \ \Omega$.

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

## Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices** [1] **(Part 4 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors [21] | 85–Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100–Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120–Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| $V_{ICM}$ (AC and DC coupled) | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V full bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 0.85 V or 0.9 V half bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V/1.05 V full bandwidth | — | 700 | — | — | 700 | — | — | 700 | — | mV |
| | $V_{CCR\_GXB}$ = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | — | 750 | — | mV |
| $t_{LTR}$ [11] | — | — | — | 10 | — | — | 10 | — | — | 10 | µs |
| $t_{LTD}$ [12] | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTD\_manual}$ [13] | — | 4 | — | — | 4 | — | — | 4 | — | — | µs |
| $t_{LTR\_LTD\_manual}$ [14] | — | 15 | — | — | 15 | — | — | 15 | — | — | µs |
| Run Length | — | — | — | 200 | — | — | 200 | — | — | 200 | UI |
| Programmable equalization (AC Gain) [10] | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | — | — | 16 | dB |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices** [1] **(Part 7 of 7)**

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll\_lock}$ [16] | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |

**Notes to Table 23:**

(1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the $V_{CCR\_GXB}$ power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

(4) This supply follows VCCR_GXB.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(8) The input reference clock frequency options depend on the data rate and the device speed grade.

(9) The line data rate may be limited by PCS-FPGA interface speed grade.

(10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(11) $t_{LTR}$ is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(12) $t_{LTD}$ is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(13) $t_{LTD\_manual}$ is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(14) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(15) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(16) $t_{pll\_lock}$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(18) The maximum peak to peak differential input voltage $V_{ID}$ after device configuration is equal to 4 × (absolute $V_{MAX}$ for receiver pin - $V_{ICM}$).

(19) For ES devices, $R_{REF}$ is 2000 Ω ±1%.

(20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(22) Refer to Figure 2.

(23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(24) I3YY devices can achieve data rates up to 10.3125 Gbps.

(25) When you use fPLL as a TXPLL of the transceiver.

(26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

(27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 26 shows the approximate maximum data rate using the 10G PCS.

**Table 26. Stratix V 10G PCS Approximate Maximum Data Rate** [1]

| Mode [2] | Transceiver Speed Grade | PMA Width | 64 | 40 | 40 | 40 | 32 | 32 |
|---|---|---|---|---|---|---|---|---|
| | | **PCS Width** | **64** | **66/67** | **50** | **40** | **64/66/67** | **32** |
| FIFO or Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 14.1 | 14.1 | 10.69 | 14.1 | 13.6 | 13.6 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 12.5 | 12.5 |
| | | C3, I3, I3L core speed grade | 12.5 | 12.5 | 10.69 | 12.5 | 10.88 | 10.88 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 Gbps | | | | | |
| | | C3, I3, I3L core speed grade | | | | | | |
| | | C4, I4 core speed grade | | | | | | |
| | | I3YY core speed grade | 10.3125 Gbps | | | | | |

**Notes to Table 26**:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)** [1]

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| **Reference Clock** | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Input Reference Clock Frequency (CMU PLL) [6] | — | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) [6] | — | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | 20% to 80% | — | — | 400 | — | — | 400 | ps |
| Fall time | 80% to 20% | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to −0.5 | — | — | 0 to −0.5 | — | % |
| On-chip termination resistors [19] | — | — | 100 | — | — | 100 | — | Ω |
| Absolute $V_{MAX}$ [3] | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | |
| Absolute $V_{MIN}$ | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| $V_{ICM}$ (AC coupled) | Dedicated reference clock pin | 1050/1000 [2] | | | 1050/1000 [2] | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 [22] | | | 1.0/0.9/0.85 [22] | | | V |
| $V_{ICM}$ (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |

Figure 4 shows the differential transmitter output waveform.

**Figure 4.  Differential Transmitter/Receiver Output/Input Waveform**

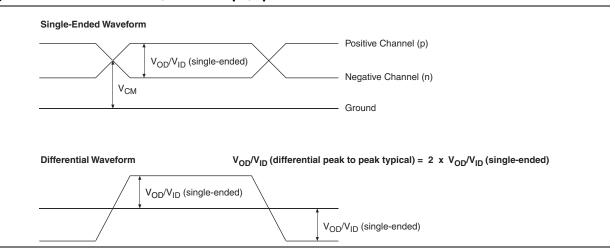**Single-Ended Waveform**

Positive Channel (p)

$V_{OD}/V_{ID}$ (single-ended)

Negative Channel (n)

$V_{CM}$

Ground

**Differential Waveform**          **$V_{OD}/V_{ID}$ (differential peak to peak typical) =  2  x  $V_{OD}/V_{ID}$ (single-ended)**

$V_{OD}/V_{ID}$ (single-ended)

$V_{OD}/V_{ID}$ (single-ended)

Figure 5 shows the Stratix V AC gain curves for GT channels.

**Figure 5.  AC Gain Curves for GT Channels**

Figure 6 shows the Stratix V DC gain curves for GT channels.

**Figure 6. DC Gain Curves for GT Channels**

## Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

■ Interlaken

■ 40G (XLAUI)/100G (CAUI)

■ 10GBase-KR

■ QSGMII

■ XAUI

■ SFI

■ Gigabit Ethernet (Gbe / GIGE)

■ SPAUI

■ Serial Rapid IO (SRIO)

■ CPRI

■ OBSAI

■ Hyper Transport (HT)

■ SATA

■ SAS

■ CEI

**Table 36. High-Speed I/O Specifications for Stratix V Devices** [1], [2] **(Part 2 of 4)**

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4, I4 | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| **Transmitter** | | | | | | | | | | | | | | |
| True Differential I/O Standards - $f_{HSDR}$ (data rate) | SERDES factor J = 3 to 10 [9], [11], [12], [13], [14], [15], [16] | [6] | — | 1600 | [6] | — | 1434 | [6] | — | 1250 | [6] | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA [12], [14], [15], [16] | [6] | — | 1600 | [6] | — | 1600 | [6] | — | 1600 | [6] | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | [6] | — | [7] | [6] | — | [7] | [6] | — | [7] | [6] | — | [7] | Mbps |
| | SERDES factor J = 1, uses SDR Register | [6] | — | [7] | [6] | — | [7] | [6] | — | [7] | [6] | — | [7] | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - $f_{HSDR}$ (data rate) [10] | SERDES factor J = 4 to 10 [17] | [6] | — | 1100 | [6] | — | 1100 | [6] | — | 840 | [6] | — | 840 | Mbps |
| $t_{x\ Jitter}$ - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| $t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

**Table 46.  JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol | Description | Min | Max | Unit |
|--------|-------------|-----|-----|------|
| $t_{JPH}$ | JTAG port hold time | 5 | — | ns |
| $t_{JPCO}$ | JTAG port clock to output | — | 11 [1] | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | — | 14 [1] | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | — | 14 [1] | ns |

**Notes to Table 46:**

(1) A 1 ns adder is required for each $V_{CCIO}$ voltage step down from 3.0 V. For example, $t_{JPCO}$ = 12 ns if $V_{CCIO}$ of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

# Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

**Table 47.  Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) [4], [5] |
|--------|--------|---------|--------------------------------|----------------------------------|
| Stratix V GX | 5SGXA3 | H35, F40, F35 [2] | 213,798,880 | 562,392 |
| | | H29, F35 [3] | 137,598,880 | 564,504 |
| | 5SGXA4 | — | 213,798,880 | 563,672 |
| | 5SGXA5 | — | 269,979,008 | 562,392 |
| | 5SGXA7 | — | 269,979,008 | 562,392 |
| | 5SGXA9 | — | 342,742,976 | 700,888 |
| | 5SGXAB | — | 342,742,976 | 700,888 |
| | 5SGXB5 | — | 270,528,640 | 584,344 |
| | 5SGXB6 | — | 270,528,640 | 584,344 |
| | 5SGXB9 | — | 342,742,976 | 700,888 |
| | 5SGXBB | — | 342,742,976 | 700,888 |
| Stratix V GT | 5SGTC5 | — | 269,979,008 | 562,392 |
| | 5SGTC7 | — | 269,979,008 | 562,392 |
| Stratix V GS | 5SGSD3 | — | 137,598,880 | 564,504 |
| | 5SGSD4 | F1517 | 213,798,880 | 563,672 |
| | | — | 137,598,880 | 564,504 |
| | 5SGSD5 | — | 213,798,880 | 563,672 |
| | 5SGSD6 | — | 293,441,888 | 565,528 |
| | 5SGSD8 | — | 293,441,888 | 565,528 |

**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family | Device | Package | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) [4], [5] |
|---|---|---|---|---|
| Stratix V E [1] | 5SEE9 | — | 342,742,976 | 700,888 |
| | 5SEEB | — | 342,742,976 | 700,888 |

**Notes to Table 47:**

(1)  Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2)  36-transceiver devices.

(3)  24-transceiver devices.

(4)  File size for the periphery image.

(5)  The IOCSR **.rbf** size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (**.hex**) or tabular text file (**.ttf**) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices*. For creating configuration files, refer to the *Quartus II Help*.

Table 48 lists the minimum configuration time estimates for Stratix V devices.

**Table 48. Minimum Configuration Time Estimation for Stratix V Devices**

| Variant | Member Code | Active Serial [1] | | | Fast Passive Parallel [2] | | |
|---|---|---|---|---|---|---|---|
| | | Width | DCLK (MHz) | Min Config Time (s) | Width | DCLK (MHz) | Min Config Time (s) |
| GX | A3 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | | 4 | 100 | 0.344 | 32 | 100 | 0.043 |
| | A4 | 4 | 100 | 0.534 | 32 | 100 | 0.067 |
| | A5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | A9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | AB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | B5 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B6 | 4 | 100 | 0.676 | 32 | 100 | 0.085 |
| | B9 | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| | BB | 4 | 100 | 0.857 | 32 | 100 | 0.107 |
| GT | C5 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |
| | C7 | 4 | 100 | 0.675 | 32 | 100 | 0.084 |

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

**Table 50. FPP Timing Parameters for Stratix V Devices** [1]

| Symbol | Parameter | Minimum | Maximum | Units |
|--------|-----------|---------|---------|-------|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | µs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 [2] | µs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 [3] | µs |
| $t_{CF2CK}$ [6] | nCONFIG high to first rising edge on DCLK | 1,506 | — | µs |
| $t_{ST2CK}$ [6] | nSTATUS high to first rising edge of DCLK | 2 | — | µs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency (FPP ×8/×16) | — | 125 | MHz |
| | DCLK frequency (FPP ×32) | — | 100 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode [4] | 175 | 437 | µs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU}$ + (8576 × CLKUSR period) [5] | — | — |

**Notes to Table 50:**

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

(5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(6) If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

## FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

**Table 54.  PS Timing Parameters for Stratix V Devices**

| Symbol | Parameter | Minimum | Maximum | Units |
|---|---|---|---|---|
| $t_{CF2CD}$ | nCONFIG low to CONF_DONE low | — | 600 | ns |
| $t_{CF2ST0}$ | nCONFIG low to nSTATUS low | — | 600 | ns |
| $t_{CFG}$ | nCONFIG low pulse width | 2 | — | μs |
| $t_{STATUS}$ | nSTATUS low pulse width | 268 | 1,506 [1] | μs |
| $t_{CF2ST1}$ | nCONFIG high to nSTATUS high | — | 1,506 [2] | μs |
| $t_{CF2CK}$ [5] | nCONFIG high to first rising edge on DCLK | 1,506 | — | μs |
| $t_{ST2CK}$ [5] | nSTATUS high to first rising edge of DCLK | 2 | — | μs |
| $t_{DSU}$ | DATA[] setup time before rising edge on DCLK | 5.5 | — | ns |
| $t_{DH}$ | DATA[] hold time after rising edge on DCLK | 0 | — | ns |
| $t_{CH}$ | DCLK high time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CL}$ | DCLK low time | $0.45 \times 1/f_{MAX}$ | — | s |
| $t_{CLK}$ | DCLK period | $1/f_{MAX}$ | — | s |
| $f_{MAX}$ | DCLK frequency | — | 125 | MHz |
| $t_{CD2UM}$ | CONF_DONE high to user mode [3] | 175 | 437 | μs |
| $t_{CD2CU}$ | CONF_DONE high to CLKUSR enabled | $4 \times$ maximum DCLK period | — | — |
| $t_{CD2UMC}$ | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times CLKUSR \text{ period})$ [4] | — | — |

**Notes to Table 54:**

(1)  This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2)  This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3)  The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4)  To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5)  If nSTATUS is monitored, follow the $t_{ST2CK}$ specification. If nSTATUS is not monitored, follow the $t_{CF2CK}$ specification.

# Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

**Table 55.  Initialization Clock Source Option and the Maximum Frequency**

| Initialization Clock Source | Configuration Schemes | Maximum Frequency | Minimum Number of Clock Cycles [1] |
|---|---|---|---|
| Internal Oscillator | AS, PS, FPP | 12.5 MHz | |
| CLKUSR | AS, PS, FPP [2] | 125 MHz | 8576 |
| DCLK | PS, FPP | 125 MHz | |

**Notes to Table 55:**

(1)  The minimum number of clock cycles required for device initialization.

(2)  To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

## Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

**Table 56. Remote System Upgrade Circuitry Timing Specifications**

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| $t_{RU\_nCONFIG}$ [1] | 250 | — | ns |
| $t_{RU\_nRSTIMER}$ [2] | 250 | — | ns |

**Notes to Table 56:**

(1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

## User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

**Table 57. 12.5-MHz Internal Oscillator Specifications**

| Minimum | Typical | Maximum | Units |
|---|---|---|---|
| 5.3 | 7.9 | 12.5 | MHz |

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

## Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

**Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)**

| Parameter [1] | Available Settings | Min Offset [2] | Fast Model | | Slow Model | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D1 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D2 | 32 | 0 | 0.230 | 0.244 | 0.415 | 0.415 | 0.459 | 0.503 | 0.417 | 0.456 | 0.500 | ns |

**Table 60. Glossary  (Part 4 of 4)**

| Letter | Subject | Definitions |
|--------|---------|-------------|
| **V** | $V_{CM(DC)}$ | DC common mode input voltage. |
| | $V_{ICM}$ | Input common mode voltage—The common mode of the differential signal at the receiver. |
| | $V_{ID}$ | Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver. |
| | $V_{DIF(AC)}$ | AC differential input voltage—Minimum AC input differential voltage required for switching. |
| | $V_{DIF(DC)}$ | DC differential input voltage— Minimum DC input differential voltage required for switching. |
| | $V_{IH}$ | Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high. |
| | $V_{IH(AC)}$ | High-level AC input voltage |
| | $V_{IH(DC)}$ | High-level DC input voltage |
| | $V_{IL}$ | Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low. |
| | $V_{IL(AC)}$ | Low-level AC input voltage |
| | $V_{IL(DC)}$ | Low-level DC input voltage |
| | $V_{OCM}$ | Output common mode voltage—The common mode of the differential signal at the transmitter. |
| | $V_{OD}$ | Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter. |
| | $V_{SWING}$ | Differential input voltage |
| | $V_X$ | Input differential cross point voltage |
| | $V_{OX}$ | Output differential cross point voltage |
| **W** | W | High-speed I/O block—clock boost factor |
| **X** Y Z | — | — |