### Intel - 5SGXMA7K3F35C3 Datasheet





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### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

### Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1152-BBGA, FCBGA
Supplier Device Package	1152-FBGA (35x35)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma7k3f35c3

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Table 5 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% of the duty cycle. For example, a signal that overshoots to 3.95 V can be at 3.95 V for only ~21% over the lifetime of the device; for a device lifetime of 10 years, the overshoot duration amounts to ~2 years.

		saring transitions		
Symbol	Description	Condition (V)	Overshoot Duration as % @ T <sub>J</sub> = 100°C	Unit
		3.8	100	%
		3.85	64	%
		3.9	36	%
		3.95	21	%
Vi (AC)	AC input voltage	4	12	%
		4.05	7	%
		4.1	4	%
		4.15	2	%
		4.2	1	%

Table 5. Maximum Allowed Overshoot During Transitions

### Figure 1. Stratix V Device Overshoot Duration



Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
		Fast POR	200 µs		4 ms	

### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

# Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit	
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V	
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v	
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V	
(1), (3)	side)	ux, us	2.375	2.5	2.625	v	
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V	
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V	
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V	
			0.82	0.85	0.88		
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	V	
(2) _	Therefore analog power supply (left Slue)	GX, GS, GI	0.97	1.0	1.03	v	
			1.03	1.05	1.07		

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
			0.82	0.85	0.88	
V <sub>CCR_GXBR</sub>	Receiver analog power supply (right side)		0.87	0.90	0.93	v
(2)	neceiver analog power supply (right side)	۵۸, ۵۵, ۵۱	0.97	1.0	1.03	v
			1.03	1.05	1.07	
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
			0.82	0.85	0.88	
V <sub>CCT_GXBL</sub>	Transmitter analog newer supply (left side)	GX GS GT	0.87	0.90	0.93	V
	Transmitter analog power supply (left side)	un, uo, ui	0.97	1.0	1.03	
			1.03	1.05	1.07	
		GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCT GXBR</sub>	Transmitter analog newer supply (right side)		0.87	0.90	0.93	
(2) _	Transmitter analog power supply (light side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	<b>Recommended Transceiver Power Supply Operating Conditions for Stratix V GX</b> ,	<b>GS</b> , and <b>GT</b> Devices
(Part 2	of 2)	

### Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

1/0 Standard		V <sub>ccio</sub> (V)			V <sub>REF</sub> (V)		V <sub>ττ</sub> (V)			
i/O Stanuaru	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V <sub>REF</sub> – 0.04	V <sub>REF</sub>	V <sub>REF</sub> + 0.04	
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>	
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>	
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	0.49 * V <sub>CCIO</sub>	0.5 * VCCIO	0.51 * V <sub>CCIO</sub>	
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V <sub>CCI0</sub> /2	_	
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V <sub>CCI0</sub> /2	_	
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.53 * V <sub>CCIO</sub>	_	V <sub>CCI0</sub> /2	_	
HSUL-12	1.14	1.2	1.3	0.49 * V <sub>CCIO</sub>	0.5 * V <sub>CCIO</sub>	0.51 * V <sub>CCIO</sub>	_	_		

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devi	ces
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Table 19.	Single-Ended SSTL	, HSTL, and HSUL I/	/O Standards Signal S	<b>Specifications for</b>	Stratix V Devices	(Part 1 of 2)
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1/0 Standard	V <sub>IL(DC)</sub> (V)		V <sub>IH(D</sub>	V <sub>IH(DC)</sub> (V)		V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	I <sub>oh</sub>
i/o Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	I <sub>ol</sub> (IIIA)	(mÄ)
SSTL-2 Class I	-0.3	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.31 V <sub>REF</sub> + 0.31		V <sub>TT</sub> – 0.608	V <sub>TT</sub> + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.31	V <sub>REF</sub> + 0.31	V <sub>TT</sub> – 0.81	V <sub>TT</sub> + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	V <sub>TT</sub> – 0.603	V <sub>TT</sub> + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V <sub>REF</sub> – 0.125	V <sub>REF</sub> + 0.125	V <sub>CCI0</sub> + 0.3	V <sub>REF</sub> – 0.25	V <sub>REF</sub> + 0.25	0.28	V <sub>CCI0</sub> – 0.28	13.4	-13.4
SSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	8	-8
SSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.175	V <sub>REF</sub> + 0.175	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	16	-16
SSTL-135 Class I, II	_	V <sub>REF</sub> – 0.09	V <sub>REF</sub> + 0.09	—	V <sub>REF</sub> – 0.16	V <sub>REF</sub> + 0.16	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	—	_
SSTL-125 Class I, II		V <sub>REF</sub> – 0.85	V <sub>REF</sub> + 0.85	_	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>		
SSTL-12 Class I, II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.2 * V <sub>CCI0</sub>	0.8 * V <sub>CCI0</sub>	_	

## **Switching Characteristics**

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

### **Transceiver Performance Specifications**

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23.	Transceiver 3	Specifications	for Stratix	V GX	and GS	Devices	(1)	(Part 1	nf 7	۱
Table 20.	TIANSUCIACI	opeonitionationa	IUI UIIAIIA	I UA	anu uu	DEVICES	• •	(1 61 6 1		

Symbol/	Conditions	Transceiver Speed Grade 1		Transceiver Speed Grade 2			Trai	er Speed e 3	Unit			
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	0	
Reference Clock												
Supported I/O	Dedicated reference clock pin	Dedicated reference clock pin										
Standards	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS										
Input Reference Clock Frequency (CMU PLL) <sup>(8)</sup>	_	40		710	40	_	710	40	_	710	MHz	
Input Reference Clock Frequency (ATX PLL) <sup>(8)</sup>		100		710	100		710	100	_	710	MHz	
Rise time	Measure at ±60 mV of differential signal <sup>(26)</sup>			400	_		400			400	ns	
Fall time	Measure at ±60 mV of differential signal <sup>(26)</sup>		_	400	_		400			400	- ps	
Duty cycle		45		55	45		55	45	—	55	%	
Spread-spectrum modulating clock frequency	PCI Express® (PCIe <sup>®</sup> )	30		33	30		33	30	_	33	kHz	

### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trar	isceive Grade	r Speed 2	Tran	isceive Grade	er Speed e 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Inter-transceiver block transmitter channel-to- channel skew	xN PMA bonded mode	_	_	500	_	_	500	_	_	500	ps
CMU PLL	•										
Supported Data Range	_	600	_	12500	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	—	1			1			1			μs
t <sub>pll_lock</sub> <sup>(16)</sup>		—		10	—	_	10	—	_	10	μs
ATX PLL											
	VCO post-divider L=2	8000	_	14100	8000	_	12500	8000	_	8500/ 10312.5 (24)	Mbps
Supported Data	L=4	4000	_	7050	4000	_	6600	4000	—	6600	Mbps
Rate Range	L=8	2000		3525	2000		3300	2000		3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	1000	_	1762.5	Mbps
t <sub>pll_powerdown</sub> (15)	—	1	_	—	1	_	—	1	_	—	μs
t <sub>pll_lock</sub> (16)	—		—	10		—	10	—		10	μs
fPLL	•										
Supported Data Range	_	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	600	_	3250/ 3125 <sup>(25)</sup>	Mbps
t <sub>pll_powerdown</sub> <sup>(15)</sup>	_	1	—		1	—		1			μs

Symbol/	Conditions	Transceiver Speed Grade 1			Trai	nsceive Grade	r Speed 2	Trar	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
t <sub>pll_lock</sub> (16)	_			10			10		_	10	μs

#### Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 7 of 7)

#### Notes to Table 23:

(2) The reference clock common mode voltage is equal to the V<sub>CCR\_GXB</sub> power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

- (4) This supply follows VCCR\_GXB.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t<sub>LTR</sub> is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t<sub>LTD</sub> is time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high.
- (13) t<sub>LTD\_manual</sub> is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14)  $t_{LTR\_LTD\_manual}$  is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15)  $t_{pll_powerdown}$  is the PLL powerdown minimum pulse width.
- (16) t<sub>pll lock</sub> is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (18) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to 4 × (absolute  $V_{MAX}$  for receiver pin  $V_{ICM}$ ).
- (19) For ES devices,  $R_{BEF}$  is 2000  $\Omega \pm 1\%$ .
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20\*log(f/622).
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

<sup>(1)</sup> Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

	Table 28.	<b>Transceiver S</b>	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit				
Description		Min	Тур	Max	Min	Тур	Max					
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps				
Differential on-chip	GT channels	_	100	—		100	_	Ω				
termination resistors	GX channels				(8)							
	GT channels	_	500	_		500	_	mV				
V <sub>OCM</sub> (AC Coupled)	GX channels		•	•	(8)		•					
Dice/Fell time	GT channels	_	15	—	—	15	—	ps				
Rise/Fail lime	GX channels		(8)									
Intra-differential pair skew	GX channels				(8)							
Intra-transceiver block transmitter channel-to- channel skew	GX channels		(8)									
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)										
CMU PLL												
Supported Data Range	—	600		12500	600		8500	Mbps				
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs				
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs				
ATX PLL												
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps				
	L=4	4000	—	6600	4000	_	6600	Mbps				
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps				
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps				
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps				
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs				
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs				
fPLL												
Supported Data Range		600		3250/ 3.125 <sup>(23)</sup>	600		3250/ 3.125 <sup>(23)</sup>	Mbps				
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs				

Table 28. Tra	nsceiver Specifi	cations for Stra	tix V GT Devices	(Part 5 of 5) <sup>(1)</sup>
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Symbol/ Description	Conditions	S	Transceivei peed Grade	2	ן Sr	Unit		
Description		Min	Тур	Max	Min	Тур	Max	
t <sub>pll_lock</sub> <sup>(14)</sup>	—	—	_	10	—	—	10	μs

#### Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the Stratix V Device Overview.
- (2) The reference clock common mode voltage is equal to the VCCR\_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t<sub>1 TR</sub> is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t<sub>LTD</sub> is time required for the receiver CDR to start recovering valid data after the rx is lockedtodata signal goes high.
- (11)  $t_{LTD\_manual}$  is the time required for the receiver CDR to start recovering valid data after the rx\_is\_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (12) t<sub>LTR\_LTD\_manual</sub> is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx\_is\_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (13) tpll\_powerdown is the PLL powerdown minimum pulse width.
- (14) tpll lock is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCle at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage  $V_{ID}$  after device configuration is equal to 4 × (absolute  $V_{MAX}$  for receiver pin  $V_{ICM}$ ).
- (17) For ES devices, RREF is 2000  $\Omega \pm 1\%$ .
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20\*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR\_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Figure 4 shows the differential transmitter output waveform.





Figure 5 shows the Stratix V AC gain curves for GT channels.

Figure 5. AC Gain Curves for GT Channels

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
<sup>L</sup> FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj 10</sub> (5),	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>foutpj 10</sub> <sup>(5),</sup>	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I3YY	C4,I4			Unit
Symbol	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
	SERDES factor J = 3 to 10 <sup>(9)</sup> , <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
True Differential I/O Standards	SERDES factor J $\geq 4$ LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t <sub>x Jitter</sub> - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps		_	0.1			0.1			0.1		_	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_		300	_	_	300	_		325	ps
with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

### Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Symbol	Conditions		C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY			C4,14			Unit	
əyiinuu	Conultions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Umt
	SERDES factor J = 3 to 10	(6)		(8)	(6)	_	(8)	(6)		(8)	(6)		(8)	Mbps
f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)		(7)	(6)	_	(7)	(6)	_	(7)	(6)		(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
DPA Mode														
DPA run length	_			1000 0		_	1000 0	_		1000 0	_		1000 0	UI
Soft CDR mode														
Soft-CDR PPM tolerance	_	_	_	300	_	_	300	_	_	300	_	_	300	± PPM
Non DPA Mode														
Sampling Window	_			300			300			300			300	ps

### Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The F<sub>MAX</sub> specification is based on the fast clock used for serial data. The interface F<sub>MAX</sub> is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Clock	Parameter	Symbol	C	1	C2, C2L	, 12, 12L	C3, I3 I3	8, <b>13L</b> , YY	C4	,14	Unit
NGLWUIK			Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-25	25	-25	25	-30	30	-35	35	ps
PHY Clock	Cycle-to-cycle period jitter	$t_{\rm JIT(cc)}$	-50	50	-50	50	-60	60	-70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-37.5	37.5	-37.5	37.5	-45	45	-56	56	ps

### Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 2 of 2) (2), (3)

### Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

### **OCT Calibration Block Specifications**

Table 43 lists the OCT calibration block specifications for Stratix V devices.

### Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Тур	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	_	20	MHz
T <sub>OCTCAL</sub>	Number of OCTUSRCLK clock cycles required for OCT $\rm R_S/R_T$ calibration		1000	_	Cycles
T <sub>OCTSHIFT</sub>	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	_	32	_	Cycles
T <sub>RS_RT</sub>	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT $R_S$ and $R_T$ (Figure 10)		2.5		ns

Figure 10 shows the timing diagram for the oe and dyn\_term\_ctrl signals.

### Figure 10. Timing Diagram for oe and dyn\_term\_ctrl Signals



Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) <sup>(4), (5)</sup>
Stratix V E <sup>(1)</sup>	5SEE9	—	342,742,976	700,888
	5SEEB	—	342,742,976	700,888

### Table 47. Uncompressed .rbf Sizes for Stratix V Devices

### Notes to Table 47:

(1) Stratix V E devices do not have PCI Express® (PCIe®) hard IP. Stratix V E devices do not support the CvP configuration scheme.

(2) 36-transceiver devices.

(3) 24-transceiver devices.

(4) File size for the periphery image.

(5) The IOCSR .rbf size is specifically for the CvP feature.

Use the data in Table 47 to estimate the file size before design compilation. Different configuration file formats, such as a hexadecimal (.hex) or tabular text file (.ttf) format, have different file sizes. For the different types of configuration file and file sizes, refer to the Quartus II software. However, for a specific version of the Quartus II software, any design targeted for the same device has the same uncompressed configuration file size. If you are using compression, the file size can vary after each compilation because the compression ratio depends on your design.

• For more information about setting device configuration options, refer to *Configuration, Design Security, and Remote System Upgrades in Stratix V Devices.* For creating configuration files, refer to the *Quartus II Help.* 

Table 48 lists the minimum configuration time estimates for Stratix V devices.

Table 48. Minimum Configuration Time Estimation for Stratix V Devi
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	Marchar	Active Serial <sup>(1)</sup>			Fast Passive Parallel <sup>(2)</sup>			
Variant	Code	Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)	
	٨٥	4	100	0.534	32	100	0.067	
	AJ	4	100	0.344	32	100	0.043	
	A4	4	100	0.534	32	100	0.067	
GX	A5	4	100	0.675	32	100	0.084	
	A7	4	100	0.675	32	100	0.084	
	A9	4	100	0.857	32	100	0.107	
	AB	4	100	0.857	32	100	0.107	
	B5	4	100	0.676	32	100	0.085	
	B6	4	100	0.676	32	100	0.085	
	B9	4	100	0.857	32	100	0.107	
	BB	4	100	0.857	32	100	0.107	
ст	C5	4	100	0.675	32	100	0.084	
ul	C7	4	100	0.675	32	100	0.084	

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
	Disabled	Disabled	1
FPP ×32	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8

Table 49.	DCLK-to-DATA[]	Ratio <sup>(1)</sup>	(Part 2 of 2)
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Note to Table 49:

(1) Depending on the DCLK-to-DATA [] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA [] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

### Figure 11. Single Device FPP Configuration Using an External Host



#### Notes to Figure 11:

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device.  $V_{CCPGM}$  must be high enough to meet the  $V_{IH}$  specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with  $V_{CCPGM}$ .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

IF the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Table 50 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 50. FPP Timing Parameters for Stratix V Devices (1)

Symbol	Parameter	Minimum	Maximum	Units
t <sub>CF2CD</sub>	nCONFIG low to CONF_DONE low		600	ns
t <sub>CF2ST0</sub>	nCONFIG low to nSTATUS low		600	ns
t <sub>CFG</sub>	nCONFIG low pulse width	2	_	μS
t <sub>status</sub>	nSTATUS low pulse width	268	1,506 <sup>(2)</sup>	μS
t <sub>CF2ST1</sub>	nCONFIG high to nSTATUS high		1,506 <sup>(3)</sup>	μS
t <sub>CF2CK</sub> (6)	nCONFIG high to first rising edge on DCLK	1,506		μS
t <sub>ST2CK</sub> (6)	nSTATUS high to first rising edge of DCLK	2		μS
t <sub>DSU</sub>	DATA [] setup time before rising edge on DCLK	5.5		ns
t <sub>DH</sub>	DATA [] hold time after rising edge on DCLK	0	_	ns
t <sub>CH</sub>	DCLK high time	$0.45\times 1/f_{MAX}$		S
t <sub>CL</sub>	DCLK low time	$0.45\times 1/f_{MAX}$		S
t <sub>CLK</sub>	DCLK period	1/f <sub>MAX</sub>	_	S
£	DCLK frequency (FPP ×8/×16)	—	125	MHz
IMAX	DCLK frequency (FPP ×32)	—	100	MHz
t <sub>CD2UM</sub>	CONF_DONE high to user mode <sup>(4)</sup>	175	437	μS
t <sub>CD2CU</sub>	CONTR DOWN high to Grund analysis	4 × maximum		
	CONF_DONE HIGH to CLEOSE enabled	DCLK period		_
t <sub>cD2UMC</sub>	CONF_DONE high to user mode with CLKUSR option on	$t_{CD2CU}$ + (8576 × CLKUSR period) <sup>(5)</sup>	_	

### Notes to Table 50:

(1) Use these timing parameters when the decompression and design security features are disabled.

(2) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(3) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

- (4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.
- (5) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (6) If nSTATUS is monitored, follow the t<sub>ST2CK</sub> specification. If nSTATUS is not monitored, follow the t<sub>CF2CK</sub> specification.

### FPP Configuration Timing when DCLK-to-DATA [] > 1

Figure 13 shows the timing waveform for FPP configuration when using a MAX II device, MAX V device, or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is more than 1.

### **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
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Parameter	Minimum	Unit	
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

### **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum Typical		Maximum	Units	
5.3	7.9	12.5	MHz	

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

### **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Austication Min Fast Model						Slow N	lodel				
(1)	Settings	<b>Offset</b> (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

### Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes				
		<ul> <li>Added the I3YY speed grade and changed the data rates for the GX channel in Table 1.</li> </ul>				
		<ul> <li>Added the I3YY speed grade to the V<sub>CC</sub> description in Table 6.</li> </ul>				
		<ul> <li>Added the I3YY speed grade to V<sub>CCHIP_L</sub>, V<sub>CCHIP_R</sub>, V<sub>CCHSSI_L</sub>, and V<sub>CCHSSI_R</sub> descriptions in Table 7.</li> </ul>				
		■ Added 240-Ω to Table 11.				
		Changed CDR PPM tolerance in Table 23.				
		<ul> <li>Added additional max data rate for fPLL in Table 23.</li> </ul>				
		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25.</li> </ul>				
		<ul> <li>Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26.</li> </ul>				
		<ul> <li>Changed CDR PPM tolerance in Table 28.</li> </ul>				
		<ul> <li>Added additional max data rate for fPLL in Table 28.</li> </ul>				
		<ul> <li>Changed the mode descriptions for MLAB and M20K in Table 33.</li> </ul>				
		<ul> <li>Changed the Max value of f<sub>HSCLK_OUT</sub> for the C2, C2L, I2, I2L speed grades in Table 36.</li> </ul>				
November 2014	3.3	<ul> <li>Changed the frequency ranges for C1 and C2 in Table 39.</li> </ul>				
		<ul> <li>Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47.</li> </ul>				
		<ul> <li>Added note about nSTATUS to Table 50, Table 51, Table 54.</li> </ul>				
		<ul> <li>Changed the available settings in Table 58.</li> </ul>				
		<ul> <li>Changed the note in "Periphery Performance".</li> </ul>				
		<ul> <li>Updated the "I/O Standard Specifications" section.</li> </ul>				
		<ul> <li>Updated the "Raw Binary File Size" section.</li> </ul>				
		<ul> <li>Updated the receiver voltage input range in Table 22.</li> </ul>				
		<ul> <li>Updated the max frequency for the LVDS clock network in Table 36.</li> </ul>				
		■ Updated the DCLK note to Figure 11.				
		<ul> <li>Updated Table 23 VO<sub>CM</sub> (DC Coupled) condition.</li> </ul>				
		Updated Table 6 and Table 7.				
		<ul> <li>Added the DCLK specification to Table 55.</li> </ul>				
		Updated the notes for Table 47.				
		<ul> <li>Updated the list of parameters for Table 56.</li> </ul>				
November 2013	3.2	Updated Table 28				
November 2013	3.1	Updated Table 33				
November 2013	3.0	Updated Table 23 and Table 28				
October 2013	2.9	<ul> <li>Updated the "Transceiver Characterization" section</li> </ul>				
		<ul> <li>Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59</li> </ul>				
Uctober 2013	2.8	<ul> <li>Added Figure 1 and Figure 3</li> </ul>				
		<ul> <li>Added the "Transceiver Characterization" section</li> </ul>				
		<ul> <li>Removed all "Preliminary" designations.</li> </ul>				