Intel - 5SGXMA7K3F40C4 Datasheet

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Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	696
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-BBGA, FCBGA
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma7k3f40c4

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCD_FPLL}	PLL digital power supply	–0.5	1.8	V
V_{CCA_FPLL}	PLL analog power supply	–0.5	3.4	V
V_I	DC input voltage	–0.5	3.8	V
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C
I_{OUT}	DC output current per pin	–25	40	mA

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	–0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	–0.5	3.75	V
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	–0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	–0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	–0.5	1.35	V
V_{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	–0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	–0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	–0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB (2)	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: ■ Data rate > 10.3 Gbps. ■ DFE is used.	All	1.05	3.0	1.5	V
If ANY of the following conditions are true (1): ■ ATX PLL is used. ■ Data rate > 6.5Gbps. ■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.	All	1.0			
If ALL of the following conditions are true: ■ ATX PLL is not used. ■ Data rate ≤ 6.5Gbps. ■ DFE, AEQ, and EyeQ are not used.	C1, C2, I2, and I3YY	0.90	2.5		
	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		

Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Symbol	Description	Conditions	Resistance Tolerance				Unit
			C1	C2,I2	C3, I3, I3YY	C4, I4	
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5 V	±30	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2 V	±35	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCPD} = 2.5 V	±25	±25	±25	±25	%

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

Equation 1. OCT Variation Without Recalibration for Stratix V Devices *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle \frac{dR}{dT} \times \Delta T\rangle \pm \langle \frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 1:

(1) The R_{OCT} value shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power-up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power-up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2) *(1)*

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dV	OCT variation with voltage without recalibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices (1), (2)

Symbol	Description	V_{CCIO} Conditions (V) (3)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option.	3.0 ±5%	25	kΩ
		2.5 ±5%	25	kΩ
		1.8 ±5%	25	kΩ
		1.5 ±5%	25	kΩ
		1.35 ±5%	25	kΩ
		1.25 ±5%	25	kΩ
		1.2 ±5%	25	kΩ

Notes to Table 16:

(1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG `TCK` pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to "Glossary" on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2
1.5 V	1.425	1.5	1.575	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 * V_{CCIO}	0.65 * V_{CCIO}	V_{CCIO} + 0.3	0.25 * V_{CCIO}	0.75 * V_{CCIO}	2	–2

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices

I/O Standard	V_{CCIO} (V)			V_{REF} (V)			V_{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	0.49 * V_{CCIO}	0.5 * VCCIO	0.51 * V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V_{CCIO}	0.5 * V_{CCIO}	0.53 * V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 * V_{CCIO}	0.5 * V_{CCIO}	0.51 * V_{CCIO}	—	—	—

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} – 0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} – 0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} – 0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 * V_{CCIO}	0.8 * V_{CCIO}	16	–16
SSTL-135 Class I, II	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-125 Class I, II	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—
SSTL-12 Class I, II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.15	V_{REF} + 0.15	0.2 * V_{CCIO}	0.8 * V_{CCIO}	—	—

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1* V_{CCIO}	0.9* V_{CCIO}	—	—

Table 20. Differential SSTL I/O Standards for Stratix V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	*(1)*	V_{CCIO}/2 – 0.15	—	V_{CCIO}/2 + 0.15	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	*(1)*	V_{CCIO}/2 – 0.15	V_{CCIO}/2	V_{CCIO}/2 + 0.15	2($V_{IH(AC)}$ - V_{REF})	2($V_{IL(AC)}$ - V_{REF})
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	*(1)*	V_{CCIO}/2 – 0.15	V_{CCIO}/2	V_{CCIO}/2 + 0.15	2($V_{IH(AC)}$ - V_{REF})	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	V_{REF} –0.15	V_{CCIO}/2	V_{REF} + 0.15	–0.30	0.30

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	**Typ**	**Max**	**Min**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Max**
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V_{CCIO} – 0.12	0.5* V_{CCIO}	0.5*V_{CCIO} + 0.12	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.44	0.44

Table 22. Differential I/O Standard Specifications for Stratix V Devices *(7)*

I/O Standard	V_{CCIO} (V) *(10)*			V_{ID} (mV) *(8)*			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(6)*			V_{OCM} (V) *(6)*		
	Min	**Typ**	**Max**	**Min**	**Condition**	**Max**	**Min**	**Condition**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18.														
2.5 V LVDS *(1)*	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	$D_{MAX} \leq$ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} >$ 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS *(5)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO) *(2)*	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) *(3)*	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL *(4), (9)*	—	—	—	300	—	—	0.6	$D_{MAX} \leq$ 700 Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	$D_{MAX} >$ 700 Mbps	1.6	—	—	—	—	—	—

Notes to Table 22:

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110\ \Omega$.

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in “Transceiver Performance Specifications” on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices *(1)* **(Part 5 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	2	—	—	2	—	—	2	—	dB
	DC Gain Setting = 2	—	4	—	—	4	—	—	4	—	dB
	DC Gain Setting = 3	—	6	—	—	6	—	—	6	—	dB
	DC Gain Setting = 4	—	8	—	—	8	—	—	8	—	dB
Transmitter											
Supported I/O Standards	—	1.4-V and 1.5-V PCML									
Data rate (Standard PCS)	—	600	—	12200	600	—	12200	600	—	8500/ 10312.5 *(24)*	Mbps
Data rate (10G PCS)	—	600	—	14100	600	—	12500	600	—	8500/ 10312.5 *(24)*	Mbps
Differential on-chip termination resistors	85-Ω setting	—	85 ± 20%	—	—	85 ± 20%	—	—	85 ± 20%	—	Ω
	100-Ω setting	—	100 ± 20%	—	—	100 ± 20%	—	—	100 ± 20%	—	Ω
	120-Ω setting	—	120 ± 20%	—	—	120 ± 20%	—	—	120 ± 20%	—	Ω
	150-Ω setting	—	150 ± 20%	—	—	150 ± 20%	—	—	150 ± 20%	—	Ω
V_{OCM} (AC coupled)	0.65-V setting	—	650	—	—	650	—	—	650	—	mV
V_{OCM} (DC coupled)	—	—	650	—	—	650	—	—	650	—	mV
Rise time *(7)*	20% to 80%	30	—	160	30	—	160	30	—	160	ps
Fall time *(7)*	80% to 20%	30	—	160	30	—	160	30	—	160	ps
Intra-differential pair skew	Tx V_{CM} = 0.5 V and slew rate of 15 ps	—	—	15	—	—	15	—	—	15	ps
Intra-transceiver block transmitter channel-to-channel skew	x6 PMA bonded mode	—	—	120	—	—	120	—	—	120	ps

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) (1)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Reference Clock								
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL						
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Input Reference Clock Frequency (CMU PLL) (6)	—	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) (6)	—	100	—	710	100	—	710	MHz
Rise time	20% to 80%	—	—	400	—	—	400	ps
Fall time	80% to 20%	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5	—	—	0 to –0.5	—	%
On-chip termination resistors (19)	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} (3)	Dedicated reference clock pin	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	-0.4	—	—	-0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled)	Dedicated reference clock pin	1050/1000 (2)			1050/1000 (2)			mV
	RX reference clock pin	1.0/0.9/0.85 (22)			1.0/0.9/0.85 (22)			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	mV

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) *(1)*

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Transmitter REFCLK Phase Noise (622 MHz) *(18)*	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	
	10 kHz	—	—	-100	—	—	-100	
	100 kHz	—	—	-110	—	—	-110	
	≥ 1 MHz	—	—	-120	—	—	-120	
Transmitter REFCLK Phase Jitter (100 MHz) *(15)*	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
RREF *(17)*	—	—	1800 ± 1%	—	—	1800 ± 1%	—	Ω
Transceiver Clocks								
`fixedclk` clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (`mgmt_clk_clk`) frequency	—	100	—	125	100	—	125	MHz
Receiver								
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Data rate (Standard PCS) *(21)*	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS) *(21)*	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Absolute V_{MAX} for a receiver pin *(3)*	GT channels	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	GT channels	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration *(20)*	GT channels	—	—	1.6	—	—	1.6	V
	GX channels	*(8)*						
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration *(16)*, *(20)*	GT channels V_{CCR_GTB} = 1.05 V (V_{ICM} = 0.65 V)	—	—	2.2	—	—	2.2	V
	GX channels	*(8)*						
Minimum differential eye opening at receiver serial input pins *(4)*, *(20)*	GT channels	200	—	—	200	—	—	mV
	GX channels	*(8)*						

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

Symbol	Performance			Unit
	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	
Global and Regional Clock	717	650	580	MHz
Periphery Clock	550	500	500	MHz

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 2 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
M20K Block	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	525	525	455	400	525	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	200	μA
V_{bias}, voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	—

Table 36. High-Speed I/O Specifications for Stratix V Devices *(1), (2)* (Part 3 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{DUTY}	Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	160	—	—	160	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with three external output resistor networks	—	—	250	—	—	250	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	—	—	300	ps
Receiver														
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10 *(11), (12), (13), (14), (15), (16)*	150	—	1434	150	—	1434	150	—	1250	150	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS RX with DPA *(12), (14), (15), (16)*	150	—	1600	150	—	1600	150	—	1600	150	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	Mbps
	SERDES factor J = 1, uses SDR Register	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	Mbps

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 4 of 4)

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	*(6)*	—	*(8)*	*(6)*	—	*(8)*	*(6)*	—	*(8)*	*(6)*	—	*(8)*	Mbps
	SERDES factor J = 2, uses DDR Registers	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	Mbps
	SERDES factor J = 1, uses SDR Register	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	*(6)*	—	*(7)*	Mbps
DPA Mode														
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode														
Soft-CDR PPM tolerance	—	—	—	300	—	—	300	—	—	300	—	—	300	± PPM
Non DPA Mode														
Sampling Window	—	—	—	300	—	—	300	—	—	300	—	—	300	ps

Notes to Table 36:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.

(2) When J = 1 or 2, bypass the SERDES block.

(3) This only applies to DPA and soft-CDR modes.

(4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.

(5) This is achieved by using the **LVDS** clock network.

(6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.

(7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (fOUT) provided you can close the design timing and the signal integrity simulation is clean.

(8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

(9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.

(10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.

(11) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.

(12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.

(13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.

(14) Requires package skew compensation with PCB trace length.

(15) Do not mix single-ended I/O buffer within LVDS I/O bank.

(16) Chip-to-chip communication only with a maximum load of 5 pF.

(17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 2 of 2)

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices (1)

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is ±78 ps or ±39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 1 of 2) (2), (3)

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	–50	50	–50	50	–55	55	–55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–100	100	–100	100	–110	110	–110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–50	50	–50	50	–82.5	82.5	–82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	–75	75	–75	75	–82.5	82.5	–82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–150	150	–150	150	–165	165	–165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–75	75	–75	75	–90	90	–90	90	ps

Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins *(1)*

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the `nSTATUS` is released high and your device is ready to begin configuration.

For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification *(1)*

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the `MSEL` settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period *(2)*	30	—	ns
t_{JCP}	TCK clock period *(2)*	167	—	ns
t_{JCH}	TCK clock high time *(2)*	14	—	ns
t_{JCL}	TCK clock low time *(2)*	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Variant	Member Code	Active Serial (1)			Fast Passive Parallel (2)		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GS	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
E	E9	4	100	0.857	32	100	0.107
	EB	4	100	0.857	32	100	0.107

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different `DCLK`-to-`DATA[]` ratio when you enable the design security, decompression, or both features. Table 49 lists the `DCLK`-to-`DATA[]` ratio for each combination.

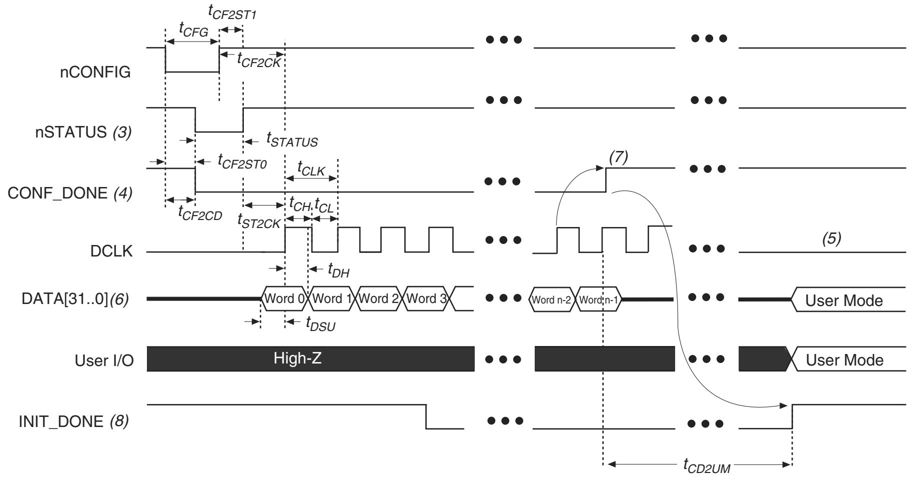
Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the `DCLK`-to-`DATA[]` ratio is 1.

Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 *(1), (2)*



Notes to Figure 12:

(1) Use this timing waveform when the `DCLK`-to-`DATA[]` ratio is 1.

(2) The beginning of this waveform shows the device in user mode. In user mode, `nCONFIG`, `nSTATUS`, and `CONF_DONE` are at logic-high levels. When `nCONFIG` is pulled low, a reconfiguration cycle begins.

(3) After power-up, the Stratix V device holds `nSTATUS` low for the time of the POR delay.

(4) After power-up, before and during configuration, `CONF_DONE` is low.

(5) Do not leave `DCLK` floating after configuration. `DCLK` is ignored after configuration is complete. It can toggle high or low if required.

(6) For FPP ×16, use `DATA[15..0]`. For FPP ×8, use `DATA[7..0]`. `DATA[31..0]` are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. `CONF_DONE` is released high when the Stratix V device receives all the configuration data successfully. After `CONF_DONE` goes high, send two additional falling edges on `DCLK` to begin initialization and enter user mode.

(8) After the option bit to enable the `INIT_DONE` pin is configured into the device, the `INIT_DONE` goes low.

Active Serial Configuration Timing

Table 52 lists the `DCLK` frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme *(1), (2)*

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

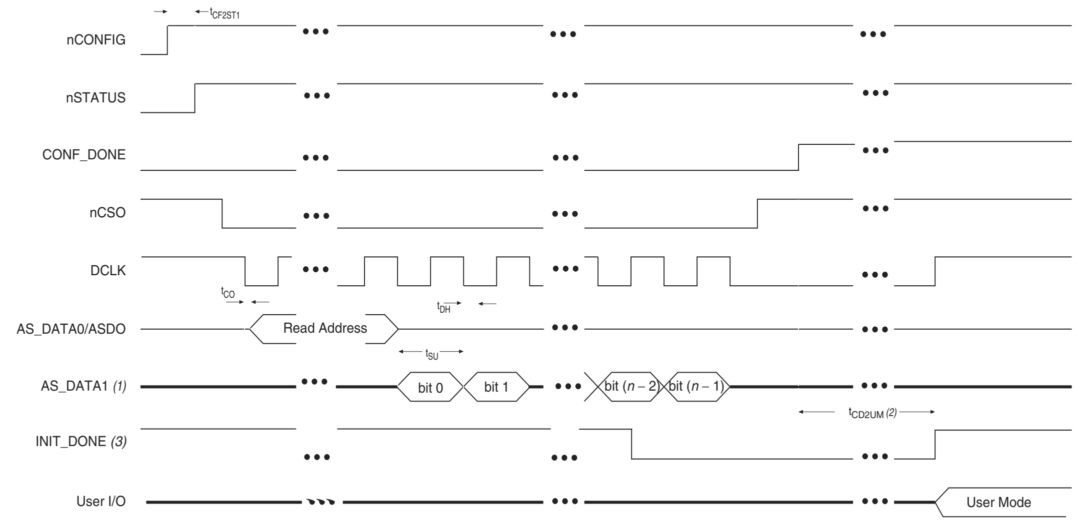
Notes to Table 52:

(1) This applies to the `DCLK` frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support `DCLK` frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing



Notes to Figure 14:

(1) If you are using AS ×4 mode, this signal represents the `AS_DATA[3..0]` and EPCQ sends in 4-bits of data for each `DCLK` cycle.

(2) The initialization clock can be from internal oscillator or `CLKUSR` pin.

(3) After the option bit to enable the `INIT_DONE` pin is configured into the device, the `INIT_DONE` goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices *(1), (2)* (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CO}	`DCLK` falling edge to `AS_DATA0/ASDO` output	—	2	ns
t_{SU}	Data setup time before falling edge on `DCLK`	1.5	—	ns
t_{H}	Data hold time after falling edge on `DCLK`	0	—	ns

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
November 2014	3.3	■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. ■ Added the I3YY speed grade to the V_{CC} description in Table 6. ■ Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. ■ Added 240-Ω to Table 11. ■ Changed CDR PPM tolerance in Table 23. ■ Added additional max data rate for fPLL in Table 23. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. ■ Changed CDR PPM tolerance in Table 28. ■ Added additional max data rate for fPLL in Table 28. ■ Changed the mode descriptions for MLAB and M20K in Table 33. ■ Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. ■ Changed the frequency ranges for C1 and C2 in Table 39. ■ Changed the **.rbf** file sizes for 5SGSD6 and 5SGSD8 in Table 47. ■ Added note about `nSTATUS` to Table 50, Table 51, Table 54. ■ Changed the available settings in Table 58. ■ Changed the note in “Periphery Performance”. ■ Updated the “I/O Standard Specifications” section. ■ Updated the “Raw Binary File Size” section. ■ Updated the receiver voltage input range in Table 22. ■ Updated the max frequency for the LVDS clock network in Table 36. ■ Updated the `DCLK` note to Figure 11. ■ Updated Table 23 VO_{CM} (DC Coupled) condition. ■ Updated Table 6 and Table 7. ■ Added the `DCLK` specification to Table 55. ■ Updated the notes for Table 47. ■ Updated the list of parameters for Table 56.
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 ■ Added Figure 1 and Figure 3 ■ Added the “Transceiver Characterization” section ■ Removed all “Preliminary” designations.