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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                     |
|--------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                            |
| Number of LABs/CLBs            | 234720                                                                                                                              |
| Number of Logic Elements/Cells | 622000                                                                                                                              |
| Total RAM Bits                 | 51200000                                                                                                                            |
| Number of I/O                  | 840                                                                                                                                 |
| Number of Gates                | -                                                                                                                                   |
| Voltage - Supply               | 0.82V ~ 0.88V                                                                                                                       |
| Mounting Type                  | Surface Mount                                                                                                                       |
| Operating Temperature          | 0°C ~ 85°C (TJ)                                                                                                                     |
| Package / Case                 | 1932-BBGA, FCBGA                                                                                                                    |
| Supplier Device Package        | 1932-FBGA, FC (45x45)                                                                                                               |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/5sgxma7n3f45c4n">https://www.e-xfl.com/product-detail/intel/5sgxma7n3f45c4n</a> |

**Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)**

| Symbol                | Description                    | Minimum | Maximum | Unit |
|-----------------------|--------------------------------|---------|---------|------|
| V <sub>CCD_FPLL</sub> | PLL digital power supply       | −0.5    | 1.8     | V    |
| V <sub>CCA_FPLL</sub> | PLL analog power supply        | −0.5    | 3.4     | V    |
| V <sub>I</sub>        | DC input voltage               | −0.5    | 3.8     | V    |
| T <sub>J</sub>        | Operating junction temperature | −55     | 125     | °C   |
| T <sub>STG</sub>      | Storage temperature (No bias)  | −65     | 150     | °C   |
| I <sub>OUT</sub>      | DC output current per pin      | −25     | 40      | mA   |

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

**Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices**

| Symbol                | Description                                                  | Devices    | Minimum | Maximum | Unit |
|-----------------------|--------------------------------------------------------------|------------|---------|---------|------|
| V <sub>CCA_GXBL</sub> | Transceiver channel PLL power supply (left side)             | GX, GS, GT | −0.5    | 3.75    | V    |
| V <sub>CCA_GXBR</sub> | Transceiver channel PLL power supply (right side)            | GX, GS     | −0.5    | 3.75    | V    |
| V <sub>CCA_GTBR</sub> | Transceiver channel PLL power supply (right side)            | GT         | −0.5    | 3.75    | V    |
| V <sub>CCHIP_L</sub>  | Transceiver hard IP power supply (left side)                 | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCHIP_R</sub>  | Transceiver hard IP power supply (right side)                | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCHSSI_L</sub> | Transceiver PCS power supply (left side)                     | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCHSSI_R</sub> | Transceiver PCS power supply (right side)                    | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCR_GXBL</sub> | Receiver analog power supply (left side)                     | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCR_GXBR</sub> | Receiver analog power supply (right side)                    | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCR_GTBR</sub> | Receiver analog power supply for GT channels (right side)    | GT         | −0.5    | 1.35    | V    |
| V <sub>CCT_GXBL</sub> | Transmitter analog power supply (left side)                  | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCT_GXBR</sub> | Transmitter analog power supply (right side)                 | GX, GS, GT | −0.5    | 1.35    | V    |
| V <sub>CCT_GTBR</sub> | Transmitter analog power supply for GT channels (right side) | GT         | −0.5    | 1.35    | V    |
| V <sub>CCL_GTBR</sub> | Transmitter clock network power supply (right side)          | GT         | −0.5    | 1.35    | V    |
| V <sub>CCH_GXBL</sub> | Transmitter output buffer power supply (left side)           | GX, GS, GT | −0.5    | 1.8     | V    |
| V <sub>CCH_GXBR</sub> | Transmitter output buffer power supply (right side)          | GX, GS, GT | −0.5    | 1.8     | V    |

#### Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

### I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

**Table 9. I/O Pin Leakage Current for Stratix V Devices <sup>(1)</sup>**

| Symbol   | Description        | Conditions                                 | Min | Typ | Max | Unit          |
|----------|--------------------|--------------------------------------------|-----|-----|-----|---------------|
| $I_I$    | Input pin          | $V_I = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | —   | 30  | $\mu\text{A}$ |
| $I_{OZ}$ | Tri-stated I/O pin | $V_O = 0 \text{ V to } V_{CCIO\text{MAX}}$ | -30 | —   | 30  | $\mu\text{A}$ |

**Note to Table 9:**

(1) If  $V_O = V_{CCIO}$  to  $V_{CCIO\text{MAX}}$ , 100  $\mu\text{A}$  of leakage current per I/O is expected.

### Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

**Table 10. Bus Hold Parameters for Stratix V Devices**

| Parameter               | Symbol            | Conditions                                     | V <sub>CCIO</sub> |      |       |      |       |      |       |      |       |      | Unit |
|-------------------------|-------------------|------------------------------------------------|-------------------|------|-------|------|-------|------|-------|------|-------|------|------|
|                         |                   |                                                | 1.2 V             |      | 1.5 V |      | 1.8 V |      | 2.5 V |      | 3.0 V |      |      |
|                         |                   |                                                | Min               | Max  | Min   | Max  | Min   | Max  | Min   | Max  | Min   | Max  |      |
| Low sustaining current  | I <sub>SUSL</sub> | V <sub>IN</sub> > V <sub>IL</sub><br>(maximum) | 22.5              | —    | 25.0  | —    | 30.0  | —    | 50.0  | —    | 70.0  | —    | μA   |
| High sustaining current | I <sub>SUSH</sub> | V <sub>IN</sub> < V <sub>IH</sub><br>(minimum) | −22.5             | —    | −25.0 | —    | −30.0 | —    | −50.0 | —    | −70.0 | —    | μA   |
| Low overdrive current   | I <sub>ODL</sub>  | 0V < V <sub>IN</sub> < V <sub>CCIO</sub>       | —                 | 120  | —     | 160  | —     | 200  | —     | 300  | —     | 500  | μA   |
| High overdrive current  | I <sub>ODH</sub>  | 0V < V <sub>IN</sub> < V <sub>CCIO</sub>       | —                 | −120 | —     | −160 | —     | −200 | —     | −300 | —     | −500 | μA   |
| Bus-hold trip point     | V <sub>TRIP</sub> | —                                              | 0.45              | 0.95 | 0.50  | 1.00 | 0.68  | 1.07 | 0.70  | 1.70 | 0.80  | 2.00 | V    |

### On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

**Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices <sup>(1)</sup> (Part 1 of 2)**

| Symbol             | Description                                                         | Conditions                                            | Calibration Accuracy |          |                |          | Unit |
|--------------------|---------------------------------------------------------------------|-------------------------------------------------------|----------------------|----------|----------------|----------|------|
|                    |                                                                     |                                                       | C1                   | C2,I2    | C3,I3,<br>I3YY | C4,I4    |      |
| 25- $\Omega$ $R_S$ | Internal series termination with calibration (25- $\Omega$ setting) | $V_{\text{CCIO}} = 3.0, 2.5, 1.8, 1.5, 1.2 \text{ V}$ | $\pm 15$             | $\pm 15$ | $\pm 15$       | $\pm 15$ | %    |

**Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) <sup>(1)</sup>**

| Symbol | Description                                          | V <sub>CCIO</sub> (V) | Typical | Unit              |
|--------|------------------------------------------------------|-----------------------|---------|-------------------|
| dR/dT  | OCT variation with temperature without recalibration | 3.0                   | 0.189   | %/ <sup>o</sup> C |
|        |                                                      | 2.5                   | 0.208   |                   |
|        |                                                      | 1.8                   | 0.266   |                   |
|        |                                                      | 1.5                   | 0.273   |                   |
|        |                                                      | 1.2                   | 0.317   |                   |

**Note to Table 13:**

(1) Valid for a V<sub>CCIO</sub> range of  $\pm 5\%$  and a temperature range of 0° to 85°C.

**Pin Capacitance**

Table 14 lists the Stratix V device family pin capacitance.

**Table 14. Pin Capacitance for Stratix V Devices**

| Symbol             | Description                                                      | Value | Unit |
|--------------------|------------------------------------------------------------------|-------|------|
| C <sub>IOTB</sub>  | Input capacitance on the top and bottom I/O pins                 | 6     | pF   |
| C <sub>IOLR</sub>  | Input capacitance on the left and right I/O pins                 | 6     | pF   |
| C <sub>OUTFB</sub> | Input capacitance on dual-purpose clock output and feedback pins | 6     | pF   |

**Hot Socketing**

Table 15 lists the hot socketing specifications for Stratix V devices.

**Table 15. Hot Socketing Specifications for Stratix V Devices**

| Symbol                    | Description                                | Maximum             |
|---------------------------|--------------------------------------------|---------------------|
| I <sub>IOPIN</sub> (DC)   | DC current per I/O pin                     | 300 $\mu$ A         |
| I <sub>IOPIN</sub> (AC)   | AC current per I/O pin                     | 8 mA <sup>(1)</sup> |
| I <sub>XCVR-TX</sub> (DC) | DC current per transceiver transmitter pin | 100 mA              |
| I <sub>XCVR-RX</sub> (DC) | DC current per transceiver receiver pin    | 50 mA               |

**Note to Table 15:**

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns,  $|I_{IOPIN}| = C \, dv/dt$ , in which C is the I/O pin capacitance and dv/dt is the slew rate.

**Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devices**

| I/O Standard            | $V_{CCIO}$ (V) |      |       | $V_{REF}$ (V)     |                  |                   | $V_{TT}$ (V)      |                  |                   |
|-------------------------|----------------|------|-------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|
|                         | Min            | Typ  | Max   | Min               | Typ              | Max               | Min               | Typ              | Max               |
| SSTL-2<br>Class I, II   | 2.375          | 2.5  | 2.625 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.833             | 0.9              | 0.969             | $V_{REF} - 0.04$  | $V_{REF}$        | $V_{REF} + 0.04$  |
| SSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-135<br>Class I, II | 1.283          | 1.35 | 1.418 | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-125<br>Class I, II | 1.19           | 1.25 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| SSTL-12<br>Class I, II  | 1.14           | 1.20 | 1.26  | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ |
| HSTL-18<br>Class I, II  | 1.71           | 1.8  | 1.89  | 0.85              | 0.9              | 0.95              | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-15<br>Class I, II  | 1.425          | 1.5  | 1.575 | 0.68              | 0.75             | 0.9               | —                 | $V_{CCIO}/2$     | —                 |
| HSTL-12<br>Class I, II  | 1.14           | 1.2  | 1.26  | $0.47 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.53 * V_{CCIO}$ | —                 | $V_{CCIO}/2$     | —                 |
| HSUL-12                 | 1.14           | 1.2  | 1.3   | $0.49 * V_{CCIO}$ | $0.5 * V_{CCIO}$ | $0.51 * V_{CCIO}$ | —                 | —                | —                 |

**Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 1 of 2)**

| I/O Standard            | $V_{IL(DC)}$ (V) |                   | $V_{IH(DC)}$ (V)  |                  | $V_{IL(AC)}$ (V)  | $V_{IH(AC)}$ (V)  | $V_{OL}$ (V)     | $V_{OH}$ (V)      | $I_{OI}$ (mA) | $I_{OH}$ (mA) |
|-------------------------|------------------|-------------------|-------------------|------------------|-------------------|-------------------|------------------|-------------------|---------------|---------------|
|                         | Min              | Max               | Min               | Max              | Max               | Min               | Max              | Min               |               |               |
| SSTL-2<br>Class I       | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.608$ | $V_{TT} + 0.608$  | 8.1           | -8.1          |
| SSTL-2<br>Class II      | -0.3             | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $V_{CCIO} + 0.3$ | $V_{REF} - 0.31$  | $V_{REF} + 0.31$  | $V_{TT} - 0.81$  | $V_{TT} + 0.81$   | 16.2          | -16.2         |
| SSTL-18<br>Class I      | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | $V_{TT} - 0.603$ | $V_{TT} + 0.603$  | 6.7           | -6.7          |
| SSTL-18<br>Class II     | -0.3             | $V_{REF} - 0.125$ | $V_{REF} + 0.125$ | $V_{CCIO} + 0.3$ | $V_{REF} - 0.25$  | $V_{REF} + 0.25$  | 0.28             | $V_{CCIO} - 0.28$ | 13.4          | -13.4         |
| SSTL-15<br>Class I      | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 8             | -8            |
| SSTL-15<br>Class II     | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.175$ | $V_{REF} + 0.175$ | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | 16            | -16           |
| SSTL-135<br>Class I, II | —                | $V_{REF} - 0.09$  | $V_{REF} + 0.09$  | —                | $V_{REF} - 0.16$  | $V_{REF} + 0.16$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-125<br>Class I, II | —                | $V_{REF} - 0.85$  | $V_{REF} + 0.85$  | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |
| SSTL-12<br>Class I, II  | —                | $V_{REF} - 0.1$   | $V_{REF} + 0.1$   | —                | $V_{REF} - 0.15$  | $V_{REF} + 0.15$  | $0.2 * V_{CCIO}$ | $0.8 * V_{CCIO}$  | —             | —             |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 2 of 7)**

| Symbol/<br>Description                                             | Conditions                                             | Transceiver Speed<br>Grade 1     |                   |      | Transceiver Speed<br>Grade 2     |                   |      | Transceiver Speed<br>Grade 3     |                   |      | Unit        |
|--------------------------------------------------------------------|--------------------------------------------------------|----------------------------------|-------------------|------|----------------------------------|-------------------|------|----------------------------------|-------------------|------|-------------|
|                                                                    |                                                        | Min                              | Typ               | Max  | Min                              | Typ               | Max  | Min                              | Typ               | Max  |             |
| Spread-spectrum<br>downspread                                      | PCIe                                                   | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5      | —    | —                                | 0 to<br>-0.5      | —    | %           |
| On-chip<br>termination<br>resistors <sup>(21)</sup>                | —                                                      | —                                | 100               | —    | —                                | 100               | —    | —                                | 100               | —    | $\Omega$    |
| Absolute $V_{MAX}$ <sup>(5)</sup>                                  | Dedicated<br>reference<br>clock pin                    | —                                | —                 | 1.6  | —                                | —                 | 1.6  | —                                | —                 | 1.6  | V           |
|                                                                    | RX reference<br>clock pin                              | —                                | —                 | 1.2  | —                                | —                 | 1.2  | —                                | —                 | 1.2  |             |
| Absolute $V_{MIN}$                                                 | —                                                      | -0.4                             | —                 | —    | -0.4                             | —                 | —    | -0.4                             | —                 | —    | V           |
| Peak-to-peak<br>differential input<br>voltage                      | —                                                      | 200                              | —                 | 1600 | 200                              | —                 | 1600 | 200                              | —                 | 1600 | mV          |
| $V_{ICM}$ (AC<br>coupled) <sup>(3)</sup>                           | Dedicated<br>reference<br>clock pin                    | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                   |      | 1050/1000/900/850 <sup>(2)</sup> |                   |      | mV          |
|                                                                    | RX reference<br>clock pin                              | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | 1.0/0.9/0.85 <sup>(4)</sup>      |                   |      | V           |
| $V_{ICM}$ (DC coupled)                                             | HCSL I/O<br>standard for<br>PCIe<br>reference<br>clock | 250                              | —                 | 550  | 250                              | —                 | 550  | 250                              | —                 | 550  | mV          |
| Transmitter<br>REFCLK Phase<br>Noise<br>(622 MHz) <sup>(20)</sup>  | 100 Hz                                                 | —                                | —                 | -70  | —                                | —                 | -70  | —                                | —                 | -70  | dBc/Hz      |
|                                                                    | 1 kHz                                                  | —                                | —                 | -90  | —                                | —                 | -90  | —                                | —                 | -90  | dBc/Hz      |
|                                                                    | 10 kHz                                                 | —                                | —                 | -100 | —                                | —                 | -100 | —                                | —                 | -100 | dBc/Hz      |
|                                                                    | 100 kHz                                                | —                                | —                 | -110 | —                                | —                 | -110 | —                                | —                 | -110 | dBc/Hz      |
|                                                                    | $\geq 1$ MHz                                           | —                                | —                 | -120 | —                                | —                 | -120 | —                                | —                 | -120 | dBc/Hz      |
| Transmitter<br>REFCLK Phase<br>Jitter<br>(100 MHz) <sup>(17)</sup> | 10 kHz to<br>1.5 MHz<br>(PCIe)                         | —                                | —                 | 3    | —                                | —                 | 3    | —                                | —                 | 3    | ps<br>(rms) |
| $R_{REF}$ <sup>(19)</sup>                                          | —                                                      | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 1800<br>$\pm 1\%$ | —    | —                                | 1800<br>$\pm 1\%$ | —    | $\Omega$    |
| <b>Transceiver Clocks</b>                                          |                                                        |                                  |                   |      |                                  |                   |      |                                  |                   |      |             |
| fixedclk clock<br>frequency                                        | PCIe<br>Receiver<br>Detect                             | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125  | —    | —                                | 100<br>or<br>125  | —    | MHz         |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 3 of 7)**

| Symbol/<br>Description                                                                                                                | Conditions                                                                   | Transceiver Speed<br>Grade 1                         |     |       | Transceiver Speed<br>Grade 2 |     |       | Transceiver Speed<br>Grade 3 |     |                                     | Unit |
|---------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|------------------------------------------------------|-----|-------|------------------------------|-----|-------|------------------------------|-----|-------------------------------------|------|
|                                                                                                                                       |                                                                              | Min                                                  | Typ | Max   | Min                          | Typ | Max   | Min                          | Typ | Max                                 |      |
| Reconfiguration clock<br>( <code>mgmt_clk_clk</code> )<br>frequency                                                                   | —                                                                            | 100                                                  | —   | 125   | 100                          | —   | 125   | 100                          | —   | 125                                 | MHz  |
| <b>Receiver</b>                                                                                                                       |                                                                              |                                                      |     |       |                              |     |       |                              |     |                                     |      |
| Supported I/O Standards                                                                                                               | —                                                                            | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS |     |       |                              |     |       |                              |     |                                     |      |
| Data rate<br>(Standard PCS)<br><sup>(9), (23)</sup>                                                                                   | —                                                                            | 600                                                  | —   | 12200 | 600                          | —   | 12200 | 600                          | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
| Data rate<br>(10G PCS) <sup>(9), (23)</sup>                                                                                           | —                                                                            | 600                                                  | —   | 14100 | 600                          | —   | 12500 | 600                          | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
| Absolute $V_{MAX}$ for<br>a receiver pin <sup>(5)</sup>                                                                               | —                                                                            | —                                                    | —   | 1.2   | —                            | —   | 1.2   | —                            | —   | 1.2                                 | V    |
| Absolute $V_{MIN}$ for<br>a receiver pin                                                                                              | —                                                                            | −0.4                                                 | —   | —     | −0.4                         | —   | —     | −0.4                         | —   | —                                   | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) before device<br>configuration <sup>(22)</sup>      | —                                                                            | —                                                    | —   | 1.6   | —                            | —   | 1.6   | —                            | —   | 1.6                                 | V    |
| Maximum peak-<br>to-peak<br>differential input<br>voltage $V_{ID}$ (diff p-<br>p) after device<br>configuration <sup>(18), (22)</sup> | $V_{CCR\_GXB} = 1.0\text{ V}/1.05\text{ V}$<br>( $V_{ICM} = 0.70\text{ V}$ ) | —                                                    | —   | 2.0   | —                            | —   | 2.0   | —                            | —   | 2.0                                 | V    |
|                                                                                                                                       | $V_{CCR\_GXB} = 0.90\text{ V}$<br>( $V_{ICM} = 0.6\text{ V}$ )               | —                                                    | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                                 | V    |
|                                                                                                                                       | $V_{CCR\_GXB} = 0.85\text{ V}$<br>( $V_{ICM} = 0.6\text{ V}$ )               | —                                                    | —   | 2.4   | —                            | —   | 2.4   | —                            | —   | 2.4                                 | V    |
| Minimum<br>differential eye<br>opening at<br>receiver serial<br>input pins <sup>(6), (22), (27)</sup>                                 | —                                                                            | 85                                                   | —   | —     | 85                           | —   | —     | 85                           | —   | —                                   | mV   |

**Table 23. Transceiver Specifications for Stratix V GX and GS Devices <sup>(1)</sup> (Part 6 of 7)**

| Symbol/<br>Description                                                | Conditions                                   | Transceiver Speed<br>Grade 1 |     |                               | Transceiver Speed<br>Grade 2 |     |                               | Transceiver Speed<br>Grade 3 |     |                                     | Unit |
|-----------------------------------------------------------------------|----------------------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------------|------|
|                                                                       |                                              | Min                          | Typ | Max                           | Min                          | Typ | Max                           | Min                          | Typ | Max                                 |      |
| Inter-transceiver<br>block transmitter<br>channel-to-<br>channel skew | xN PMA<br>bonded mode                        | —                            | —   | 500                           | —                            | —   | 500                           | —                            | —   | 500                                 | ps   |
| <b>CMU PLL</b>                                                        |                                              |                              |     |                               |                              |     |                               |                              |     |                                     |      |
| Supported Data<br>Range                                               | —                                            | 600                          | —   | 12500                         | 600                          | —   | 12500                         | 600                          | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —                                            | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                                   | μs   |
| t <sub>pll_lock</sub> <sup>(16)</sup>                                 | —                                            | —                            | —   | 10                            | —                            | —   | 10                            | —                            | —   | 10                                  | μs   |
| <b>ATX PLL</b>                                                        |                                              |                              |     |                               |                              |     |                               |                              |     |                                     |      |
| Supported Data<br>Rate Range                                          | VCO<br>post-divider<br>L=2                   | 8000                         | —   | 14100                         | 8000                         | —   | 12500                         | 8000                         | —   | 8500/<br>10312.5<br><sup>(24)</sup> | Mbps |
|                                                                       | L=4                                          | 4000                         | —   | 7050                          | 4000                         | —   | 6600                          | 4000                         | —   | 6600                                | Mbps |
|                                                                       | L=8                                          | 2000                         | —   | 3525                          | 2000                         | —   | 3300                          | 2000                         | —   | 3300                                | Mbps |
|                                                                       | L=8,<br>Local/Central<br>Clock Divider<br>=2 | 1000                         | —   | 1762.5                        | 1000                         | —   | 1762.5                        | 1000                         | —   | 1762.5                              | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —                                            | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                                   | μs   |
| t <sub>pll_lock</sub> <sup>(16)</sup>                                 | —                                            | —                            | —   | 10                            | —                            | —   | 10                            | —                            | —   | 10                                  | μs   |
| <b>fPLL</b>                                                           |                                              |                              |     |                               |                              |     |                               |                              |     |                                     |      |
| Supported Data<br>Range                                               | —                                            | 600                          | —   | 3250/<br>3125 <sup>(25)</sup> | 600                          | —   | 3250/<br>3125 <sup>(25)</sup> | 600                          | —   | 3250/<br>3125 <sup>(25)</sup>       | Mbps |
| t <sub>pll_powerdown</sub> <sup>(15)</sup>                            | —                                            | 1                            | —   | —                             | 1                            | —   | —                             | 1                            | —   | —                                   | μs   |

Table 24 shows the maximum transmitter data rate for the clock network.

**Table 24. Clock Network Maximum Data Rate Transmitter Specifications <sup>(1)</sup>**

| Clock Network                  | ATX PLL                |                    |                                       | CMU PLL <sup>(2)</sup> |                    |                                       | fPLL                   |                    |                                       |
|--------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
|                                | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span                          |
| x1 <sup>(3)</sup>              | 14.1                   | —                  | 6                                     | 12.5                   | —                  | 6                                     | 3.125                  | —                  | 3                                     |
| x6 <sup>(3)</sup>              | —                      | 14.1               | 6                                     | —                      | 12.5               | 6                                     | —                      | 3.125              | 6                                     |
| x6 PLL Feedback <sup>(4)</sup> | —                      | 14.1               | Side-wide                             | —                      | 12.5               | Side-wide                             | —                      | —                  | —                                     |
| xN (PCIe)                      | —                      | 8.0                | 8                                     | —                      | 5.0                | 8                                     | —                      | —                  | —                                     |
| xN (Native PHY IP)             | 8.0                    | 8.0                | Up to 13 channels above and below PLL | 7.99                   | 7.99               | Up to 13 channels above and below PLL | 3.125                  | 3.125              | Up to 13 channels above and below PLL |
|                                | —                      | 8.01 to 9.8304     | Up to 7 channels above and below PLL  |                        |                    |                                       |                        |                    |                                       |

**Notes to Table 24:**

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

**Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) <sup>(1)</sup>**

| Symbol/<br>Description                                                     | Conditions                      | Transceiver<br>Speed Grade 2 |               |        | Transceiver<br>Speed Grade 3 |               |        | Unit      |
|----------------------------------------------------------------------------|---------------------------------|------------------------------|---------------|--------|------------------------------|---------------|--------|-----------|
|                                                                            |                                 | Min                          | Typ           | Max    | Min                          | Typ           | Max    |           |
| Differential on-chip termination resistors <sup>(7)</sup>                  | GT channels                     | —                            | 100           | —      | —                            | 100           | —      | $\Omega$  |
| Differential on-chip termination resistors for GX channels <sup>(19)</sup> | 85- $\Omega$ setting            | —                            | 85 $\pm$ 30%  | —      | —                            | 85 $\pm$ 30%  | —      | $\Omega$  |
|                                                                            | 100- $\Omega$ setting           | —                            | 100 $\pm$ 30% | —      | —                            | 100 $\pm$ 30% | —      | $\Omega$  |
|                                                                            | 120- $\Omega$ setting           | —                            | 120 $\pm$ 30% | —      | —                            | 120 $\pm$ 30% | —      | $\Omega$  |
|                                                                            | 150- $\Omega$ setting           | —                            | 150 $\pm$ 30% | —      | —                            | 150 $\pm$ 30% | —      | $\Omega$  |
| V <sub>ICM</sub> (AC coupled)                                              | GT channels                     | —                            | 650           | —      | —                            | 650           | —      | mV        |
| VICM (AC and DC coupled) for GX Channels                                   | VCCR_GXB = 0.85 V or 0.9 V      | —                            | 600           | —      | —                            | 600           | —      | mV        |
|                                                                            | VCCR_GXB = 1.0 V full bandwidth | —                            | 700           | —      | —                            | 700           | —      | mV        |
|                                                                            | VCCR_GXB = 1.0 V half bandwidth | —                            | 750           | —      | —                            | 750           | —      | mV        |
| t <sub>LTR</sub> <sup>(9)</sup>                                            | —                               | —                            | —             | 10     | —                            | —             | 10     | $\mu$ s   |
| t <sub>LTD</sub> <sup>(10)</sup>                                           | —                               | 4                            | —             | —      | 4                            | —             | —      | $\mu$ s   |
| t <sub>LTD_manual</sub> <sup>(11)</sup>                                    | —                               | 4                            | —             | —      | 4                            | —             | —      | $\mu$ s   |
| t <sub>LTR_LTD_manual</sub> <sup>(12)</sup>                                | —                               | 15                           | —             | —      | 15                           | —             | —      | $\mu$ s   |
| Run Length                                                                 | GT channels                     | —                            | —             | 72     | —                            | —             | 72     | CID       |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| CDR PPM                                                                    | GT channels                     | —                            | —             | 1000   | —                            | —             | 1000   | $\pm$ PPM |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| Programmable equalization (AC Gain) <sup>(5)</sup>                         | GT channels                     | —                            | —             | 14     | —                            | —             | 14     | dB        |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| Programmable DC gain <sup>(6)</sup>                                        | GT channels                     | —                            | —             | 7.5    | —                            | —             | 7.5    | dB        |
|                                                                            | GX channels                     | <sup>(8)</sup>               |               |        |                              |               |        |           |
| Differential on-chip termination resistors <sup>(7)</sup>                  | GT channels                     | —                            | 100           | —      | —                            | 100           | —      | $\Omega$  |
| <b>Transmitter</b>                                                         |                                 |                              |               |        |                              |               |        |           |
| Supported I/O Standards                                                    | —                               | 1.4-V and 1.5-V PCML         |               |        |                              |               |        |           |
| Data rate (Standard PCS)                                                   | GX channels                     | 600                          | —             | 8500   | 600                          | —             | 8500   | Mbps      |
| Data rate (10G PCS)                                                        | GX channels                     | 600                          | —             | 12,500 | 600                          | —             | 12,500 | Mbps      |

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

## Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

### Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

**Table 30. Clock Tree Performance for Stratix V Devices <sup>(1)</sup>**

| Symbol                    | Performance              |                       |        | Unit |
|---------------------------|--------------------------|-----------------------|--------|------|
|                           | C1, C2, C2L, I2, and I2L | C3, I3, I3L, and I3YY | C4, I4 |      |
| Global and Regional Clock | 717                      | 650                   | 580    | MHz  |
| Periphery Clock           | 550                      | 500                   | 500    | MHz  |

**Note to Table 30:**

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

**Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)**

| Symbol    | Parameter                                            | Min    | Typ  | Max   | Unit |
|-----------|------------------------------------------------------|--------|------|-------|------|
| $f_{RES}$ | Resolution of VCO frequency ( $f_{INPFD} = 100$ MHz) | 390625 | 5.96 | 0.023 | Hz   |

**Notes to Table 31:**

- (1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.
- (2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.
- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is  $f_{IN}/N$  when  $N = 1$ .
- (5) Peak-to-peak jitter with a probability level of  $10^{-12}$  (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition:
  - a. Upstream PLL:  $0.59\text{MHz} \leq \text{Upstream PLL BW} < 1$  MHz
  - b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the  $f_{VCO}$  specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 - 0.95 must be  $\geq 1000$  MHz, while  $f_{VCO}$  for fractional value range 0.20 - 0.80 must be  $\geq 1200$  MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05-0.95 must be  $\geq 1000$  MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.20-0.80 must be  $\geq 1200$  MHz.

## DSP Block Specifications

Table 32 lists the Stratix V DSP block performance specifications.

**Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)**

| Mode                                         | Peformance |         |         |     |               |     |     | Unit |
|----------------------------------------------|------------|---------|---------|-----|---------------|-----|-----|------|
|                                              | C1         | C2, C2L | I2, I2L | C3  | I3, I3L, I3YY | C4  | I4  |      |
| Modes using one DSP                          |            |         |         |     |               |     |     |      |
| Three 9 x 9                                  | 600        | 600     | 600     | 480 | 480           | 420 | 420 | MHz  |
| One 18 x 18                                  | 600        | 600     | 600     | 480 | 480           | 420 | 400 | MHz  |
| Two partial 18 x 18 (or 16 x 16)             | 600        | 600     | 600     | 480 | 480           | 420 | 400 | MHz  |
| One 27 x 27                                  | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One 36 x 18                                  | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One sum of two 18 x 18(One sum of 2 16 x 16) | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One sum of square                            | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One 18 x 18 plus 36 (a x b) + c              | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| Modes using two DSPs                         |            |         |         |     |               |     |     |      |
| Three 18 x 18                                | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One sum of four 18 x 18                      | 475        | 475     | 475     | 380 | 380           | 300 | 300 | MHz  |
| One sum of two 27 x 27                       | 465        | 465     | 450     | 380 | 380           | 300 | 290 | MHz  |
| One sum of two 36 x 18                       | 475        | 475     | 475     | 380 | 380           | 300 | 300 | MHz  |
| One complex 18 x 18                          | 500        | 500     | 500     | 400 | 400           | 350 | 350 | MHz  |
| One 36 x 36                                  | 475        | 475     | 475     | 380 | 380           | 300 | 300 | MHz  |

**Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)**

| Memory     | Mode                                                                                             | Resources Used |        | Performance |         |     |     |         |               |     | Unit |
|------------|--------------------------------------------------------------------------------------------------|----------------|--------|-------------|---------|-----|-----|---------|---------------|-----|------|
|            |                                                                                                  | ALUTs          | Memory | C1          | C2, C2L | C3  | C4  | I2, I2L | I3, I3L, I3YY | I4  |      |
| M20K Block | Single-port, all supported widths                                                                | 0              | 1      | 700         | 700     | 650 | 550 | 700     | 500           | 450 | MHz  |
|            | Simple dual-port, all supported widths                                                           | 0              | 1      | 700         | 700     | 650 | 550 | 700     | 500           | 450 | MHz  |
|            | Simple dual-port with the read-during-write option set to <b>Old Data</b> , all supported widths | 0              | 1      | 525         | 525     | 455 | 400 | 525     | 455           | 400 | MHz  |
|            | Simple dual-port with ECC enabled, 512 × 32                                                      | 0              | 1      | 450         | 450     | 400 | 350 | 450     | 400           | 350 | MHz  |
|            | Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32                      | 0              | 1      | 600         | 600     | 500 | 450 | 600     | 500           | 450 | MHz  |
|            | True dual port, all supported widths                                                             | 0              | 1      | 700         | 700     | 650 | 550 | 700     | 500           | 450 | MHz  |
|            | ROM, all supported widths                                                                        | 0              | 1      | 700         | 700     | 650 | 550 | 700     | 500           | 450 | MHz  |

**Notes to Table 33:**

- (1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.
- (2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F<sub>MAX</sub>.
- (3) The F<sub>MAX</sub> specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

**Temperature Sensing Diode Specifications**

Table 34 lists the internal TSD specification.

**Table 34. Internal Temperature Sensing Diode Specification**

| Temperature Range | Accuracy | Offset Calibrated Option | Sampling Rate  | Conversion Time | Resolution | Minimum Resolution with no Missing Codes |
|-------------------|----------|--------------------------|----------------|-----------------|------------|------------------------------------------|
| –40°C to 100°C    | ±8°C     | No                       | 1 MHz, 500 KHz | < 100 ms        | 8 bits     | 8 bits                                   |

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

**Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices**

| Description                              | Min   | Typ   | Max   | Unit |
|------------------------------------------|-------|-------|-------|------|
| I <sub>bias</sub> , diode source current | 8     | —     | 200   | μA   |
| V <sub>bias</sub> , voltage across diode | 0.3   | —     | 0.9   | V    |
| Series resistance                        | —     | —     | < 1   | Ω    |
| Diode ideality factor                    | 1.006 | 1.008 | 1.010 | —    |

**Table 36. High-Speed I/O Specifications for Stratix V Devices <sup>(1)</sup>, <sup>(2)</sup> (Part 3 of 4)**

| Symbol                                                     | Conditions                                                                                                                          | C1             |     |                | C2, C2L, I2, I2L |     |                | C3, I3, I3L, I3YY |     |                | C4, I4         |     |                | Unit |
|------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------|----------------|-----|----------------|------------------|-----|----------------|-------------------|-----|----------------|----------------|-----|----------------|------|
|                                                            |                                                                                                                                     | Min            | Typ | Max            | Min              | Typ | Max            | Min               | Typ | Max            | Min            | Typ | Max            |      |
| $t_{DUTY}$                                                 | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards                                           | 45             | 50  | 55             | 45               | 50  | 55             | 45                | 50  | 55             | 45             | 50  | 55             | %    |
| $t_{RISE}$ & $t_{FALL}$                                    | True Differential I/O Standards                                                                                                     | —              | —   | 160            | —                | —   | 160            | —                 | —   | 200            | —              | —   | 200            | ps   |
|                                                            | Emulated Differential I/O Standards with three external output resistor networks                                                    | —              | —   | 250            | —                | —   | 250            | —                 | —   | 250            | —              | —   | 300            | ps   |
| TCCS                                                       | True Differential I/O Standards                                                                                                     | —              | —   | 150            | —                | —   | 150            | —                 | —   | 150            | —              | —   | 150            | ps   |
|                                                            | Emulated Differential I/O Standards                                                                                                 | —              | —   | 300            | —                | —   | 300            | —                 | —   | 300            | —              | —   | 300            | ps   |
| <b>Receiver</b>                                            |                                                                                                                                     |                |     |                |                  |     |                |                   |     |                |                |     |                |      |
| True Differential I/O Standards - $f_{HSDRDP}$ (data rate) | SERDES factor J = 3 to 10 <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup> | 150            | —   | 1434           | 150              | —   | 1434           | 150               | —   | 1250           | 150            | —   | 1050           | Mbps |
|                                                            | SERDES factor J $\geq 4$                                                                                                            | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                            | LVDS RX with DPA <sup>(12)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>                                              | 150            | —   | 1600           | 150              | —   | 1600           | 150               | —   | 1600           | 150            | —   | 1250           | Mbps |
|                                                            | SERDES factor J = 2, uses DDR Registers                                                                                             | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |
|                                                            | SERDES factor J = 1, uses SDR Register                                                                                              | <sup>(6)</sup> | —   | <sup>(7)</sup> | <sup>(6)</sup>   | —   | <sup>(7)</sup> | <sup>(6)</sup>    | —   | <sup>(7)</sup> | <sup>(6)</sup> | —   | <sup>(7)</sup> | Mbps |

**Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)**

| Speed Grade | Min | Max | Unit |
|-------------|-----|-----|------|
| C4,I4       | 8   | 16  | ps   |

**Notes to Table 40:**

- (1) The typical value equals the average of the minimum and maximum values.
- (2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is  $[625 \text{ ps} + (10 \times 10 \text{ ps}) \pm 20 \text{ ps}] = 725 \text{ ps} \pm 20 \text{ ps}$ .

Table 41 lists the DQS phase shift error for Stratix V devices.

**Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock ( $t_{\text{DQS\_PSERR}}$ ) for Stratix V Devices <sup>(1)</sup>**

| Number of DQS Delay Buffers | C1  | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|-----------------------------|-----|------------------|-------------------|-------|------|
| 1                           | 28  | 28               | 30                | 32    | ps   |
| 2                           | 56  | 56               | 60                | 64    | ps   |
| 3                           | 84  | 84               | 90                | 96    | ps   |
| 4                           | 112 | 112              | 120               | 128   | ps   |

**Notes to Table 41:**

- (1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is  $\pm 78 \text{ ps}$  or  $\pm 39 \text{ ps}$ .

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

**Table 42. Memory Output Clock Jitter Specification for Stratix V Devices <sup>(1), (Part 1 of 2)</sup> <sup>(2), (3)</sup>**

| Clock Network | Parameter                    | Symbol                 | C1   |     | C2, C2L, I2, I2L |     | C3, I3, I3L, I3YY |      | C4,I4 |      | Unit |
|---------------|------------------------------|------------------------|------|-----|------------------|-----|-------------------|------|-------|------|------|
|               |                              |                        | Min  | Max | Min              | Max | Min               | Max  | Min   | Max  |      |
| Regional      | Clock period jitter          | $t_{\text{JIT(per)}}$  | –50  | 50  | –50              | 50  | –55               | 55   | –55   | 55   | ps   |
|               | Cycle-to-cycle period jitter | $t_{\text{JIT(cc)}}$   | –100 | 100 | –100             | 100 | –110              | 110  | –110  | 110  | ps   |
|               | Duty cycle jitter            | $t_{\text{JIT(duty)}}$ | –50  | 50  | –50              | 50  | –82.5             | 82.5 | –82.5 | 82.5 | ps   |
| Global        | Clock period jitter          | $t_{\text{JIT(per)}}$  | –75  | 75  | –75              | 75  | –82.5             | 82.5 | –82.5 | 82.5 | ps   |
|               | Cycle-to-cycle period jitter | $t_{\text{JIT(cc)}}$   | –150 | 150 | –150             | 150 | –165              | 165  | –165  | 165  | ps   |
|               | Duty cycle jitter            | $t_{\text{JIT(duty)}}$ | –75  | 75  | –75              | 75  | –90               | 90   | –90   | 90   | ps   |

## Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

**Table 44. Worst-Case DCD on Stratix V I/O Pins <sup>(1)</sup>**

| Symbol            | C1  |     | C2, C2L, I2, I2L |     | C3, I3, I3L, I3YY |     | C4, I4 |     | Unit |
|-------------------|-----|-----|------------------|-----|-------------------|-----|--------|-----|------|
|                   | Min | Max | Min              | Max | Min               | Max | Min    | Max |      |
| Output Duty Cycle | 45  | 55  | 45               | 55  | 45                | 55  | 45     | 55  | %    |

**Note to Table 44:**

(1) The DCD numbers do not cover the core clock network.

## Configuration Specification

### POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.



For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

**Table 45. Fast and Standard POR Delay Specification <sup>(1)</sup>**

| POR Delay | Minimum | Maximum |
|-----------|---------|---------|
| Fast      | 4 ms    | 12 ms   |
| Standard  | 100 ms  | 300 ms  |

**Note to Table 45:**

(1) You can select the POR delay based on the MSEL settings as described in the MSEL Pin Settings section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

### JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol                  | Description                        | Min | Max | Unit |
|-------------------------|------------------------------------|-----|-----|------|
| t <sub>JCP</sub>        | TCK clock period <sup>(2)</sup>    | 30  | —   | ns   |
| t <sub>JCP</sub>        | TCK clock period <sup>(2)</sup>    | 167 | —   | ns   |
| t <sub>JCH</sub>        | TCK clock high time <sup>(2)</sup> | 14  | —   | ns   |
| t <sub>JCL</sub>        | TCK clock low time <sup>(2)</sup>  | 14  | —   | ns   |
| t <sub>JPSU (TDI)</sub> | TDI JTAG port setup time           | 2   | —   | ns   |
| t <sub>JPSU (TMS)</sub> | TMS JTAG port setup time           | 3   | —   | ns   |

**Table 46. JTAG Timing Parameters and Values for Stratix V Devices**

| Symbol     | Description                              | Min | Max               | Unit |
|------------|------------------------------------------|-----|-------------------|------|
| $t_{JPH}$  | JTAG port hold time                      | 5   | —                 | ns   |
| $t_{JPCO}$ | JTAG port clock to output                | —   | 11 <sup>(1)</sup> | ns   |
| $t_{JPZX}$ | JTAG port high impedance to valid output | —   | 14 <sup>(1)</sup> | ns   |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | —   | 14 <sup>(1)</sup> | ns   |

**Notes to Table 46:**

- (1) A 1 ns adder is required for each  $V_{CCIO}$  voltage step down from 3.0 V. For example,  $t_{JPCO}$  = 12 ns if  $V_{CCIO}$  of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.
- (2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

## Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (.rbf) sizes for Stratix V devices.

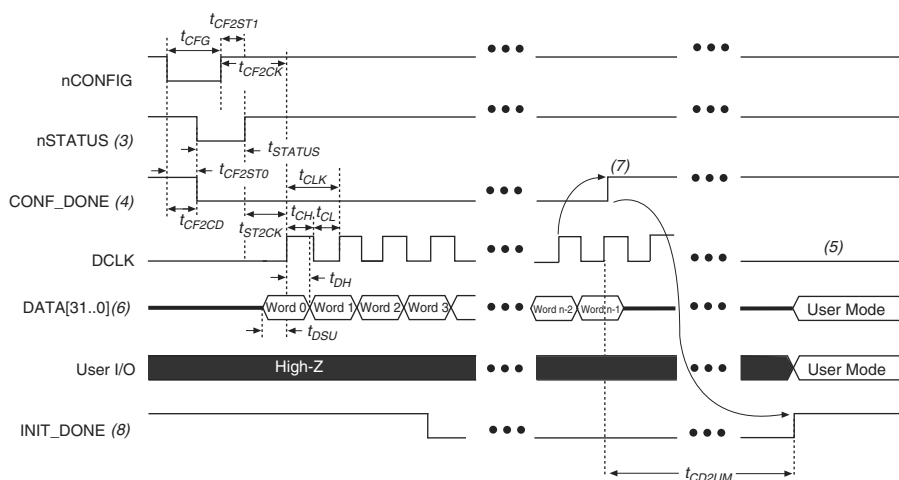
**Table 47. Uncompressed .rbf Sizes for Stratix V Devices**

| Family       | Device | Package                      | Configuration .rbf Size (bits) | IOCSR .rbf Size (bits) <sup>(4), (5)</sup> |
|--------------|--------|------------------------------|--------------------------------|--------------------------------------------|
| Stratix V GX | 5SGXA3 | H35, F40, F35 <sup>(2)</sup> | 213,798,880                    | 562,392                                    |
|              |        | H29, F35 <sup>(3)</sup>      | 137,598,880                    | 564,504                                    |
|              | 5SGXA4 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGXA5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA7 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGXA9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXAB | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXB5 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB6 | —                            | 270,528,640                    | 584,344                                    |
|              | 5SGXB9 | —                            | 342,742,976                    | 700,888                                    |
|              | 5SGXBB | —                            | 342,742,976                    | 700,888                                    |
| Stratix V GT | 5SGTC5 | —                            | 269,979,008                    | 562,392                                    |
|              | 5SGTC7 | —                            | 269,979,008                    | 562,392                                    |
| Stratix V GS | 5SGSD3 | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD4 | F1517                        | 213,798,880                    | 563,672                                    |
|              |        | —                            | 137,598,880                    | 564,504                                    |
|              | 5SGSD5 | —                            | 213,798,880                    | 563,672                                    |
|              | 5SGSD6 | —                            | 293,441,888                    | 565,528                                    |
|              | 5SGSD8 | —                            | 293,441,888                    | 565,528                                    |

## FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

**Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 <sup>(1)</sup>, <sup>(2)</sup>**



### Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF\_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF\_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP x16, use DATA [15..0]. For FPP x8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF\_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF\_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT\_DONE pin is configured into the device, the INIT\_DONE goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

**Table 54. PS Timing Parameters for Stratix V Devices**

| Symbol                     | Parameter                                         | Minimum                                                         | Maximum              | Units   |
|----------------------------|---------------------------------------------------|-----------------------------------------------------------------|----------------------|---------|
| $t_{CF2CD}$                | nCONFIG low to CONF_DONE low                      | —                                                               | 600                  | ns      |
| $t_{CF2ST0}$               | nCONFIG low to nSTATUS low                        | —                                                               | 600                  | ns      |
| $t_{CFG}$                  | nCONFIG low pulse width                           | 2                                                               | —                    | $\mu$ s |
| $t_{STATUS}$               | nSTATUS low pulse width                           | 268                                                             | 1,506 <sup>(1)</sup> | $\mu$ s |
| $t_{CF2ST1}$               | nCONFIG high to nSTATUS high                      | —                                                               | 1,506 <sup>(2)</sup> | $\mu$ s |
| $t_{CF2CK}$ <sup>(5)</sup> | nCONFIG high to first rising edge on DCLK         | 1,506                                                           | —                    | $\mu$ s |
| $t_{ST2CK}$ <sup>(5)</sup> | nSTATUS high to first rising edge of DCLK         | 2                                                               | —                    | $\mu$ s |
| $t_{DSU}$                  | DATA [] setup time before rising edge on DCLK     | 5.5                                                             | —                    | ns      |
| $t_{DH}$                   | DATA [] hold time after rising edge on DCLK       | 0                                                               | —                    | ns      |
| $t_{CH}$                   | DCLK high time                                    | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CL}$                   | DCLK low time                                     | $0.45 \times 1/f_{MAX}$                                         | —                    | s       |
| $t_{CLK}$                  | DCLK period                                       | $1/f_{MAX}$                                                     | —                    | s       |
| $f_{MAX}$                  | DCLK frequency                                    | —                                                               | 125                  | MHz     |
| $t_{CD2UM}$                | CONF_DONE high to user mode <sup>(3)</sup>        | 175                                                             | 437                  | $\mu$ s |
| $t_{CD2CU}$                | CONF_DONE high to CLKUSR enabled                  | 4 × maximum DCLK period                                         | —                    | —       |
| $t_{CD2UMC}$               | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ <sup>(4)</sup> | —                    | —       |

**Notes to Table 54:**

- (1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.
- (3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the “Initialization” section.
- (5) If nSTATUS is monitored, follow the  $t_{ST2CK}$  specification. If nSTATUS is not monitored, follow the  $t_{CF2CK}$  specification.

## Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

**Table 55. Initialization Clock Source Option and the Maximum Frequency**

| Initialization Clock Source | Configuration Schemes      | Maximum Frequency | Minimum Number of Clock Cycles <sup>(1)</sup> |
|-----------------------------|----------------------------|-------------------|-----------------------------------------------|
| Internal Oscillator         | AS, PS, FPP                | 12.5 MHz          | 8576                                          |
| CLKUSR                      | AS, PS, FPP <sup>(2)</sup> | 125 MHz           |                                               |
| DCLK                        | PS, FPP                    | 125 MHz           |                                               |

**Notes to Table 55:**

- (1) The minimum number of clock cycles required for device initialization.
- (2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.

## Document Revision History

Table 61 lists the revision history for this chapter.

**Table 61. Document Revision History (Part 1 of 3)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|---------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| June 2018     | 3.9     | <ul style="list-style-type: none"> <li>■ Added the “Stratix V Device Overshoot Duration” figure.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| April 2017    | 3.8     | <ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “PS Timing Parameters for Stratix V Devices” table.</li> <li>■ Changed the condition for <math>100\text{-}\Omega</math> <math>R_D</math> in the “OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum value for <math>t_{CD2UMC}</math> in the “FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1” table.</li> <li>■ Changed the minimum number of clock cycles value in the “Initialization Clock Source Option and the Maximum Frequency” table.</li> </ul> |
| June 2016     | 3.7     | <ul style="list-style-type: none"> <li>■ Added the <math>V_{ID}</math> minimum specification for LVPECL in the “Differential I/O Standard Specifications for Stratix V Devices” table</li> <li>■ Added the <math>I_{OUT}</math> specification to the “Absolute Maximum Ratings for Stratix V Devices” table.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| December 2015 | 3.6     | <ul style="list-style-type: none"> <li>■ Added a footnote to the “High-Speed I/O Specifications for Stratix V Devices” table.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| December 2015 | 3.5     | <ul style="list-style-type: none"> <li>■ Changed the transmitter, receiver, and ATX PLL data rate specifications in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the configuration .rbf sizes in the “Uncompressed .rbf Sizes for Stratix V Devices” table.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
| July 2015     | 3.4     | <ul style="list-style-type: none"> <li>■ Changed the data rate specification for transceiver speed grade 3 in the following tables: <ul style="list-style-type: none"> <li>■ “Transceiver Specifications for Stratix V GX and GS Devices”</li> <li>■ “Stratix V Standard PCS Approximate Maximum Date Rate”</li> <li>■ “Stratix V 10G PCS Approximate Maximum Data Rate”</li> </ul> </li> <li>■ Changed the conditions for reference clock rise and fall time, and added a note to the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Added a note to the “Minimum differential eye opening at receiver serial input pins” specification in the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> <li>■ Changed the <math>t_{CO}</math> maximum value in the “AS Timing Parameters for AS ‘1 and AS ‘4 Configurations in Stratix V Devices” table.</li> <li>■ Removed the CDR ppm tolerance specification from the “Transceiver Specifications for Stratix V GX and GS Devices” table.</li> </ul>                                                  |

**Table 61. Document Revision History (Part 3 of 3)**

| Date          | Version | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|---------------|---------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| May 2013      | 2.7     | <ul style="list-style-type: none"> <li>■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60</li> <li>■ Added Table 24, Table 48</li> <li>■ Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>                                                                                                                                                                                                                                                                                                                               |
| February 2013 | 2.6     | <ul style="list-style-type: none"> <li>■ Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> <li>■ Updated “Maximum Allowed Overshoot and Undershoot Voltage”</li> </ul>                                                                                                                                                                                                                                                                                                                                               |
| December 2012 | 2.5     | <ul style="list-style-type: none"> <li>■ Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> <li>■ Added Table 33</li> <li>■ Added “Fast Passive Parallel Configuration Timing”</li> <li>■ Added “Active Serial Configuration Timing”</li> <li>■ Added “Passive Serial Configuration Timing”</li> <li>■ Added “Remote System Upgrades”</li> <li>■ Added “User Watchdog Internal Circuitry Timing Specification”</li> <li>■ Added “Initialization”</li> <li>■ Added “Raw Binary File Size”</li> </ul> |
| June 2012     | 2.4     | <ul style="list-style-type: none"> <li>■ Added Figure 1, Figure 2, and Figure 3.</li> <li>■ Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> <li>■ Various edits throughout to fix bugs.</li> <li>■ Changed title of document to <i>Stratix V Device Datasheet</i>.</li> <li>■ Removed document from the Stratix V handbook and made it a separate document.</li> </ul>                            |
| February 2012 | 2.3     | <ul style="list-style-type: none"> <li>■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| December 2011 | 2.2     | <ul style="list-style-type: none"> <li>■ Added Table 2–31.</li> <li>■ Updated Table 2–28 and Table 2–34.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
| November 2011 | 2.1     | <ul style="list-style-type: none"> <li>■ Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> <li>■ Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> <li>■ Various edits throughout to fix SPRs.</li> </ul>                                                                                                                                                                                                                                                                                          |
| May 2011      | 2.0     | <ul style="list-style-type: none"> <li>■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.</li> <li>■ Updated the “DQ Logic Block and Memory Output Clock Jitter Specifications” title.</li> <li>■ Chapter moved to Volume 1.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                     |
| December 2010 | 1.1     | <ul style="list-style-type: none"> <li>■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.</li> <li>■ Converted chapter to the new template.</li> <li>■ Minor text edits.</li> </ul>                                                                                                                                                                                                                                                                                                                                                                           |
| July 2010     | 1.0     | Initial release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |