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Intel - 5SGXMA7N3F45I4N Datasheet



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	234720
Number of Logic Elements/Cells	622000
Total RAM Bits	51200000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma7n3f45i4n

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

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Transceiver Speed Grade				Core Spe	ed Grade			
	C1	C2, C2L	C3	C4	12, 12L	13, 13L	I 3YY	14
3 GX channel—8.5 Gbps	_	Yes	Yes	Yes	_	Yes	Yes ⁽⁴⁾	Yes

Table 1. Stratix V GX and GS Commercial and Industrial Speed Grade Offering ^{(1), (2), (3)} (Part 2 of 2)

Notes to Table 1:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

(3) C2L, I2L, and I3L speed grades are for low-power devices.

(4) I3YY speed grades can achieve up to 10.3125 Gbps.

Table 2 lists the industrial and commercial speed grades for the Stratix V GT devices. **Table 2. Stratix V GT Commercial and Industrial Speed Grade Offering** ⁽¹⁾, ⁽²⁾

Transseiver Speed Grade	Core Speed Grade						
Transceiver Speeu draue	C1	C2	12	13			
2 GX channel—12.5 Gbps GT channel—28.05 Gbps	Yes	Yes	_	_			
3 GX channel—12.5 Gbps GT channel—25.78 Gbps	Yes	Yes	Yes	Yes			

Notes to Table 2:

(1) C = Commercial temperature grade; I = Industrial temperature grade.

(2) Lower number refers to faster speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Stratix V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.



Conditions other than those listed in Table 3 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

TANIC J. ANSULULC MAXIMUM NALINYS IVI SUALIX V DEVICES (FAIL I UI Z)	Table 3.	Absolute Maximum	Ratings	for Stratix \	/ Devices	(Part 1 of 2)
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Symbol	Description	Minimum	Maximum	Unit
V _{CC}	Power supply for core voltage and periphery circuitry	-0.5	1.35	V
V _{CCPT}	Power supply for programmable power technology	-0.5	1.8	V
V _{CCPGM}	Power supply for configuration pins	-0.5	3.9	V
V _{CC_AUX}	Auxiliary supply for the programmable power technology	-0.5	3.4	V
V _{CCBAT}	Battery back-up power supply for design security volatile key register	-0.5	3.9	V
V _{CCPD}	I/O pre-driver power supply	-0.5	3.9	V
V _{CCIO}	I/O power supply	-0.5	3.9	V

Symbol	Description	Devices	Minimum ⁽⁴⁾	Typical	Maximum ⁽⁴⁾	Unit
			0.82	0.85	0.88	
V _{CCR_GXBR}	Receiver analog power supply (right side)		0.87	0.90	0.93	v
(2)		ux, us, ui	0.97	1.0	1.03	v
Symbol V _{CCR_GXBR} Ref V _{CCR_GTBR} Ref V _{CCT_GXBL} Tr V _{CCT_GXBR} Tr V _{CCT_GTBR} Tr			1.03	1.05	1.07	
V _{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V _{CCT_GXBL}			0.82	0.85	0.88	
	Transmitter analog power supply (left side)	GX GS GT	0.87	0.90	0.93	V
	Transmitter analog power supply (left side)	un, uo, ui	0.97	1.0	1.03	
			1.03	1.05	1.07	
		GX, GS, GT	0.82	0.85	0.88	V
V _{CCT GXBR}	Transmitter analog power supply (right side)		0.87	0.90	0.93	
(2) _			0.97	1.0	1.03	
			1.03	1.05	1.07	
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
V_{CCL_GTBR}	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V _{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V _{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	Recommended Transceiver Power Supply Operating Conditions for Stratix V GX ,	GS , and GT Devices
(Part 2	of 2)	

Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB ⁽²⁾	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
 DFE is used. 					
If ANY of the following conditions are true ⁽¹⁾ :			3.0		
 ATX PLL is used. 					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
 ATX PLL is not used. 					
■ Data rate \leq 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
 DFE, AEQ, and EyeQ are not used. 					

Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9.	I/O Pin	Leakage	Current for	Stratix V	Devices (1)
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Symbol	Description	Conditions	Min	Тур	Max	Unit
I _I	Input pin	$V_I = 0 V \text{ to } V_{CCIOMAX}$	-30	_	30	μA
I _{OZ}	Tri-stated I/O pin	$V_0 = 0 V \text{ to } V_{\text{CCIOMAX}}$	-30		30	μA

Note to Table 9:

(1) If $V_0 = V_{CCI0}$ to $V_{CCI0Max}$, 100 μ A of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

			V _{CCIO}										
Parameter	Symbol	Conditions	1.2	2 V	1.	5 V	1.8	B V	2.5	5 V	3.0	V	Unit
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I _{SUSL}	V _{IN} > V _{IL} (maximum)	22.5	_	25.0	_	30.0	_	50.0	_	70.0	_	μA
High sustaining current	I _{SUSH}	V _{IN} < V _{IH} (minimum)	-22.5		-25.0	_	-30.0	_	-50.0	_	-70.0		μA
Low overdrive current	I _{odl}	$0V < V_{IN} < V_{CCIO}$		120		160		200	_	300		500	μA
High overdrive current	I _{odh}	$0V < V_{IN} < V_{CCIO}$		-120		-160		-200		-300		-500	μΑ
Bus-hold trip point	V _{TRIP}	_	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	۷

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 1 of 2)

			Calibration Accuracy				
Symbol	Description	Conditions	C1	C2,12	C3,I3, I3YY	C4,14	Unit
25- $Ω$ R _S	Internal series termination with calibration (25- Ω setting)	V _{CCI0} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

1/0 Standard		V _{ccio} (V)			V _{REF} (V)		ν _{ττ} (ν)			
i/O Stanuaru	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	V _{REF} – 0.04	V _{REF}	V _{REF} + 0.04	
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V _{REF} – 0.04	V _{REF}	V _{REF} + 0.04	
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}	
SSTL-135 Class I, II	1.283	1.35	1.418	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	
SSTL-125 Class I, II	1.19	1.25	1.26	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}	
SSTL-12 Class I, II	1.14	1.20	1.26	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	0.49 * V _{CCIO}	0.5 * VCCIO	0.51 * V _{CCIO}	
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	_	V _{CCI0} /2	_	
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	_	V _{CCI0} /2	_	
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 * V _{CCIO}	0.5 * V _{CCIO}	0.53 * V _{CCIO}	_	V _{CCI0} /2	_	
HSUL-12	1.14	1.2	1.3	0.49 * V _{CCIO}	0.5 * V _{CCIO}	0.51 * V _{CCIO}	_			

Table 18. Single-Ended SSTL, HSTL, and HSUL I/O Reference Voltage Specifications for Stratix V Devi	ces
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Table 19.	Single-Ended SSTL	, HSTL, and HSUL I/	/O Standards Signal S	Specifications for	Stratix V Devices	(Part 1 of 2)
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1/0 Standard	V _{IL(DI}	_{c)} (V)	V _{IH(DC)} (V)		V _{IL(AC)} (V)	V _{IH(AC)} (V)	V _{ol} (V)	V _{oh} (V)	I (mA)	I _{oh}
i/o Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	I _{ol} (IIIA)	(mÄ)
SSTL-2 Class I	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCI0} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.608	V _{TT} + 0.608	8.1	-8.1
SSTL-2 Class II	-0.3	V _{REF} – 0.15	V _{REF} + 0.15	V _{CCI0} + 0.3	V _{REF} – 0.31	V _{REF} + 0.31	V _{TT} – 0.81	V _{TT} + 0.81	16.2	-16.2
SSTL-18 Class I	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCI0} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	V _{TT} – 0.603	V _{TT} + 0.603	6.7	-6.7
SSTL-18 Class II	-0.3	V _{REF} – 0.125	V _{REF} + 0.125	V _{CCI0} + 0.3	V _{REF} – 0.25	V _{REF} + 0.25	0.28	V _{CCI0} – 0.28	13.4	-13.4
SSTL-15 Class I	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.175	V _{REF} + 0.175	0.2 * V _{CCI0}	0.8 * V _{CCI0}	8	-8
SSTL-15 Class II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.175	V _{REF} + 0.175	0.2 * V _{CCI0}	0.8 * V _{CCI0}	16	-16
SSTL-135 Class I, II	_	V _{REF} – 0.09	V _{REF} + 0.09	—	V _{REF} – 0.16	V _{REF} + 0.16	0.2 * V _{CCI0}	0.8 * V _{CCI0}	—	_
SSTL-125 Class I, II		V _{REF} – 0.85	V _{REF} + 0.85	_	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCI0}	0.8 * V _{CCI0}		
SSTL-12 Class I, II	_	V _{REF} – 0.1	V _{REF} + 0.1	_	V _{REF} – 0.15	V _{REF} + 0.15	0.2 * V _{CCI0}	0.8 * V _{CCI0}	_	

Symbol/	Conditions	Trai	nsceive Grade	r Speed 1	Trai	Transceiver Speed Grade 2			Transceiver Speed Grade 3			
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max		
Reconfiguration clock (mgmt_clk_clk) frequency	_	100		125	100		125	100	_	125	MHz	
Receiver												
Supported I/O Standards	_			1.4-V PCMI	L, 1.5-V	PCML,	2.5-V PCM	L, LVPE	CL, and	d LVDS		
Data rate (Standard PCS) (9), (23)	_	600	_	12200	600	_	12200	600	_	8500/ 10312.5 (24)	Mbps	
Data rate (10G PCS) ^{(9),} ⁽²³⁾	_	600	_	14100	600	_	12500	600	_	8500/ 10312.5 (24)	Mbps	
Absolute V _{MAX} for a receiver pin ⁽⁵⁾	_	_	_	1.2	_	_	1.2	_	_	1.2	V	
Absolute V _{MIN} for a receiver pin	_	-0.4	_	_	-0.4	_	_	-0.4	_	_	V	
Maximum peak- to-peak differential input voltage V _{ID} (diff p- p) before device configuration ⁽²²⁾	_	_	_	1.6	_	_	1.6	_		1.6	V	
Maximum peak- to-peak	V _{CCR_GXB} = 1.0 V/1.05 V (V _{ICM} = 0.70 V)	_	_	2.0	_	_	2.0	_	_	2.0	V	
differential input voltage V_{ID} (diff p- p) after device	V _{CCR_GXB} = 0.90 V (V _{ICM} = 0.6 V)			2.4			2.4			2.4	V	
(22)	$V_{CCR_GXB} = 0.85 V$ (V _{ICM} = 0.6 V)			2.4			2.4		_	2.4	V	
Minimum differential eye opening at receiver serial input pins ^{(6), (22),} (27)	_	85			85			85	_	_	mV	

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Trai	Unit		
Description		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	
Differential on- chip termination resistors ⁽²¹⁾	85– Ω setting	_	85 ± 30%		_	85 ± 30%		—	85 ± 30%		Ω
	100–Ω setting	_	100 ± 30%		_	100 ± 30%		_	100 ± 30%	_	Ω
	120–Ω setting	_	120 ± 30%		_	120 ± 30%		_	120 ± 30%	_	Ω
	150-Ω setting	_	150 ± 30%		_	150 ± 30%	_	_	150 ± 30%	_	Ω
	V _{CCR_GXB} = 0.85 V or 0.9 V full bandwidth	_	600	_	_	600	_		600	_	mV
V _{ICM} (AC and DC	V _{CCR_GXB} = 0.85 V or 0.9 V half bandwidth		600	_		600	_		600	_	mV
(oupled)	V _{CCR_GXB} = 1.0 V/1.05 V full bandwidth		700	_	_	700	_	_	700	_	mV
	V _{CCR_GXB} = 1.0 V half bandwidth		750	_	_	750	_	_	750	_	mV
t _{LTR} ⁽¹¹⁾	—	_	_	10	_	—	10	_	—	10	μs
t _{LTD} ⁽¹²⁾	—	4	_		4	—		4	-	—	μs
t _{LTD_manual} ⁽¹³⁾	—	4			4	—		4	—	—	μs
t _{LTR_LTD_manual} ⁽¹⁴⁾	—	15	_		15	—		15	—	—	μs
Run Length		_		200	_	—	200	_	—	200	UI
Programmable equalization (AC Gain) ⁽¹⁰⁾	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)		_	16	_	_	16	_		16	dB

 Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

Mode ⁽²⁾	Transceiver	PMA Width	20	20	16	16	10	10	8	8
	Speed Grade	PCS/Core Width	40	20	32	16	20	10	16	8
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
FIFO	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.5	5.8	5.2	4.72
	_	C3, I3, I3L core speed grade	9.8	9.0	7.84	7.2	5.3	4.7	4.24	3.76
		C1, C2, C2L, I2, I2L core speed grade	8.5	8.5	8.5	8.5	6.5	5.8	5.2	4.72
	3	I3YY core speed grade	10.3125	10.3125	7.84	7.2	5.3	4.7	4.24	3.76
		C3, I3, I3L core speed grade	8.5	8.5	7.84	7.2	5.3	4.7	4.24	3.76
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.8	4.2	3.84	3.44
	1	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	ŋ	C1, C2, C2L, I2, I2L core speed grade	12.2	11.4	9.76	9.12	6.1	5.7	4.88	4.56
	۷	C3, I3, I3L core speed grade	9.8	9.0	7.92	7.2	4.9	4.5	3.96	3.6
Register		C1, C2, C2L, I2, I2L core speed grade	10.3125	10.3125	10.3125	10.3125	6.1	5.7	4.88	4.56
	3	I3YY core speed grade	10.3125	10.3125	7.92	7.2	4.9	4.5	3.96	3.6
FIFO	3 -	C3, I3, I3L core speed grade	8.5	8.5	7.92	7.2	4.9	4.5	3.96	3.6
		C4, I4 core speed grade	8.5	8.2	7.04	6.56	4.4	4.1	3.52	3.28

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate (1), (3)

Notes to Table 25:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

(3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 26 shows the approximate maximum data rate using the 10G PCS.

Mode ⁽²⁾	Transceiver	PMA Width	64	40	40	40	32	32		
mode ""	Speed Grade	PCS Width	64	66/67	50	40	64/66/67	32		
	1	C1, C2, C2L, I2, I2L core speed grade	14.1	14.1	10.69	14.1	13.6	13.6		
	2	C1, C2, C2L, I2, I2L core speed grade	12.5	12.5	10.69	12.5	12.5	12.5		
		C3, I3, I3L core speed grade	12.5	12.5	10.69	12.5	10.88	10.88		
FIFO or Register	2	C1, C2, C2L, I2, I2L core speed grade								
		C3, I3, I3L core speed grade	- 8.5 Gbps							
	5	C4, I4 core speed grade								
		I3YY core speed grade			10.312	25 Gbps				

Notes to Table 26:

(1) The maximum data rate is in Gbps.

(2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.

Symbol/ Description	Conditions	s	Transceive peed Grade	r 2	S	Unit				
Description		Min	Тур	Max	Min	Тур	Max			
Reference Clock								1		
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCN	IL, 1.4-V PC	ML, 1.5-V P(CML, 2.5-V I and HCSL	PCML, Diffe	rential LVPE	ECL, LVDS,		
otanuarus	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS								
Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾		40	_	710	40	_	710	MHz		
Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾	_	100	_	710	100	_	710	MHz		
Rise time	20% to 80%	_		400	_	_	400			
Fall time	80% to 20%			400	—	_	400	ps		
Duty cycle	—	45	_	55	45	_	55	%		
Spread-spectrum modulating clock frequency	PCI Express (PCIe)	30	_	33	30	_	33	kHz		
Spread-spectrum downspread	PCle	_	0 to -0.5	_	_	0 to -0.5	_	%		
On-chip termination resistors ⁽¹⁹⁾	_	_	100	_	_	100	_	Ω		
Absolute V _{MAX} ⁽³⁾	Dedicated reference clock pin	_	_	1.6	_	_	1.6	V		
	RX reference clock pin	_	_	1.2	_	_	1.2			
Absolute V _{MIN}	—	-0.4		—	-0.4	—		V		
Peak-to-peak differential input voltage	_	200	_	1600	200	_	1600	mV		
V _{ICM} (AC coupled)	Dedicated reference clock pin		1050/1000 ^{(,}	2)	1	050/1000 (2)	mV		
	RX reference clock pin	1	.0/0.9/0.85 (22)	1.	0/0.9/0.85 ((22)	V		
V _{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	_	550	250	_	550	mV		

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5)⁽¹⁾

Symbol/	Conditions	S	Transceive peed Grade	2	S	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Differential on-chip termination resistors ⁽⁷⁾	GT channels		100	_	_	100	_	Ω
	85- Ω setting	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-chip	100-Ω setting	_	100 ± 30%	_	_	100 ± 30%	_	Ω
for GX channels ⁽¹⁹⁾	120-Ω setting	_	120 ± 30%	_	—	120 ± 30%	—	Ω
	150-Ω setting	_	150 ± 30%	_	_	150 ± 30%	_	Ω
V _{ICM} (AC coupled)	GT channels	_	650	_	—	650	—	mV
	VCCR_GXB = 0.85 V or 0.9 V	_	600	_	_	600	_	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 1.0 V full bandwidth	_	700		_	700	_	mV
	VCCR_GXB = 1.0 V half bandwidth	_	750	_	_	750	_	mV
t _{LTR} ⁽⁹⁾	—	_	—	10	—	—	10	μs
t _{LTD} ⁽¹⁰⁾		4			4	_	_	μs
t _{LTD_manual} ⁽¹¹⁾		4	_		4	_	_	μs
t _{LTR_LTD_manual} ⁽¹²⁾	—	15	—	_	15	—	—	μs
Run Lenath	GT channels		—	72	—	—	72	CID
	GX channels				(8)			
CDR PPM	GT channels	_	—	1000	—	—	1000	± PPM
	GX channels				(8)			
Programmable	GT channels			14		_	14	dB
(AC Gain) ⁽⁵⁾	GX channels				(8)			
Programmable	GT channels	_		7.5	_		7.5	dB
DC gain ⁽⁶⁾	GX channels				(8)			
Differential on-chip termination resistors ⁽⁷⁾	GT channels	_	100	—	_	100	_	Ω
Transmitter								
Supported I/O Standards	_			1.4-V	and 1.5-V P	CML		
Data rate (Standard PCS)	GX channels	600	_	8500	600		8500	Mbps
Data rate (10G PCS)	GX channels	600		12,500	600		12,500	Mbps

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5)⁽¹⁾

Figure 6 shows the Stratix V DC gain curves for GT channels.

Figure 6. DC Gain Curves for GT Channels

Transceiver Characterization

This section summarizes the Stratix V transceiver characterization results for compliance with the following protocols:

- Interlaken
- 40G (XLAUI)/100G (CAUI)
- 10GBase-KR
- QSGMII
- XAUI
- SFI
- Gigabit Ethernet (Gbe / GIGE)
- SPAUI
- Serial Rapid IO (SRIO)
- CPRI
- OBSAI
- Hyper Transport (HT)
- SATA
- SAS
- CEI

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance								
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit					
Global and Regional Clock	717	650	580	MHz					
Periphery Clock	550	500	500	MHz					

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 2 of 2)

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a -2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices ⁽¹⁾

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,14	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a -2 speed grade is ± 78 ps or ± 39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1	^{),} (Part 1 of 2) ^{(2), (3)}
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Clock	Parameter	Symbol	C1 C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,14		Unit		
Network		-	Min	Max	Min	Max	Min	Max	Min	Max	
	Clock period jitter	$t_{JIT(per)}$	-50	50	-50	50	-55	55	-55	55	ps
Regional	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-100	100	-100	100	-110	110	-110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-50	50	-50	50	-82.5	82.5	-82.5	82.5	ps
	Clock period jitter	$t_{JIT(per)}$	-75	75	-75	75	-82.5	82.5	-82.5	82.5	ps
Global	Cycle-to-cycle period jitter	$t_{\text{JIT(cc)}}$	-150	150	-150	150	-165	165	-165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	-75	75	-75	75	-90	90	-90	90	ps

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is 1.





Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nstatus low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP ×16, use DATA [15..0]. For FPP ×8, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT DONE goes low.

Table 51 lists the timing parameters for Stratix V devices for FPP configuration when the DCLK-to-DATA [] ratio is more than 1.

Table 51.	FPP Timing	Parameters f	or Stratix V	Devices When	the DCLK-te	o-DATA[] Ratio	is >1 (1)
			•••••••••••••••••••••••••••••••••••••••			• • • • • • • • • • • • • • • • • • •		

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2		μS
t _{STATUS}	nSTATUS low pulse width	268	1,506 ⁽²⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506		μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2		μS
t _{DSU}	DATA [] setup time before rising edge on DCLK	5.5		ns
t _{DH}	DATA [] hold time after rising edge on DCLK	N-1/f _{DCLK} (5)		S
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$		S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$		S
t _{CLK}	DCLK period	1/f _{MAX}		S
f	DCLK frequency (FPP ×8/×16)	—	125	MHz
f _{MAX}	DCLK frequency (FPP ×32)	—	100	MHz
t _R	Input rise time	—	40	ns
t _F	Input fall time	—	40	ns
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t _{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 51:

- (1) Use these timing parameters when you use the decompression and design security features.
- (2) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
- (3) The minimum and maximum numbers apply only if you use the internal oscillator as the clock source for initializing the device.
- (4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (5) N is the DCLK-to-DATA ratio and f_{DCLK} is the DCLK frequency the system is operating.
- (6) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t _{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t _{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t _{CFG}	nCONFIG low pulse width	2	—	μS
t _{status}	nSTATUS low pulse width	268	1,506 ⁽¹⁾	μS
t _{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 ⁽²⁾	μS
t _{CF2CK} (5)	nCONFIG high to first rising edge on DCLK	1,506	—	μS
t _{ST2CK} (5)	nSTATUS high to first rising edge of DCLK	2	—	μS
t _{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t _{DH}	DATA [] hold time after rising edge on DCLK	0	—	ns
t _{CH}	DCLK high time	$0.45\times 1/f_{MAX}$	—	S
t _{CL}	DCLK low time	$0.45\times 1/f_{MAX}$	—	S
t _{CLK}	DCLK period	1/f _{MAX}	—	S
f _{MAX}	DCLK frequency	—	125	MHz
t _{CD2UM}	CONF_DONE high to user mode ⁽³⁾	175	437	μS
t _{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	_	_
t _{cd2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) ⁽⁴⁾	_	_

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55.	Initialization	Clock Source	e Option	and the	Maximum	Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles ⁽¹⁾
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP ⁽²⁾	125 MHz	8576
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software from the General panel of the Device and Pin Options dialog box.

Remote System Upgrades

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio

Parameter	Minimum	Maximum	Unit
t _{RU_nCONFIG} ⁽¹⁾	250	—	ns
t _{RU_nRSTIMER} ⁽²⁾	250	_	ns

Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset_timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

User Watchdog Internal Circuitry Timing Specification

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

Programmable IOE Delay

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Parameter	Available Settings	Min Offset (2)	Fast Model		Slow Model							
			Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

Table 60. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G H I	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: TMS
K L M N O		
Ρ	PLL Specifications	Diagram of PLL Specifications (1)
Q	_	—
R	RL	Receiver differential input discrete resistor (external to the Stratix V device).