# E·XFL

# Intel - 5SGXMA9N3F45I4N Datasheet



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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Obsolete
Number of LABs/CLBs	317000
Number of Logic Elements/Cells	840000
Total RAM Bits	53248000
Number of I/O	840
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1932-BBGA, FCBGA
Supplier Device Package	1932-FBGA, FC (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxma9n3f45i4n

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Symbol	Description	Condition	Min <sup>(4)</sup>	Тур	Max <sup>(4)</sup>	Unit
t <sub>RAMP</sub>	Power supply ramp time	Standard POR	200 µs	_	100 ms	—
		Fast POR	200 µs		4 ms	

#### Table 6. Recommended Operating Conditions for Stratix V Devices (Part 2 of 2)

#### Notes to Table 6:

(1)  $V_{CCPD}$  must be 2.5 V when  $V_{CCI0}$  is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V.  $V_{CCPD}$  must be 3.0 V when  $V_{CCI0}$  is 3.0 V.

(2) If you do not use the design security feature in Stratix V devices, connect V<sub>CCBAT</sub> to a 1.2- to 3.0-V power supply. Stratix V power-on-reset (POR) circuitry monitors V<sub>CCBAT</sub>. Stratix V devices will not exit POR if V<sub>CCBAT</sub> stays at logic low.

(3) C2L and I2L can also be run at 0.90 V for legacy boards that were designed for the C2 and I2 speed grades.

(4) The power supply value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 7 lists the transceiver power supply recommended operating conditions for Stratix V GX, GS, and GT devices.

# Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 1 of 2)

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCA GXBL</sub>	Transceiver channel PLL power supply (left		2.85	3.0	3.15	V
(1), (3)	side)	un, us, ui	2.375	2.5	2.625	v
V <sub>CCA_GXBR</sub>	Transceiver channel PLL power supply (right	CV CS	2.85	3.0	3.15	V
(1), (3)	side)	ux, us	2.375	2.5	2.625	v
V <sub>CCA_GTBR</sub>	Transceiver channel PLL power supply (right side)	GT	2.85	3.0	3.15	V
	Transceiver hard IP power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_L</sub>	Transceiver hard IP power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver hard IP power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHIP_R</sub>	Transceiver hard IP power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (left side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_L</sub>	Transceiver PCS power supply (left side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
	Transceiver PCS power supply (right side; C1, C2, I2, and I3YY speed grades)	GX, GS, GT	0.87	0.9	0.93	V
V <sub>CCHSSI_R</sub>	Transceiver PCS power supply (right side; C2L, C3, C4, I2L, I3, I3L, and I4 speed grades)	GX, GS, GT	0.82	0.85	0.88	V
			0.82	0.85	0.88	
V <sub>CCR_GXBL</sub>	Receiver analog nower supply (left side)		0.87	0.90	0.93	v
(2) _	Therefore analog power supply (left Slue)	un, uo, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	

Symbol	Description	Devices	Minimum <sup>(4)</sup>	Typical	Maximum <sup>(4)</sup>	Unit
V <sub>CCR_GXBR</sub>			0.82	0.85	0.88	
	Receiver analog power supply (right side)		0.87	0.90	0.93	v
(2)	neceiver analog power supply (right side)	ux, us, ui	0.97	1.0	1.03	v
			1.03	1.05	1.07	
V <sub>CCR_GTBR</sub>	Receiver analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
			0.82	0.85	0.88	
V <sub>CCT GXBL</sub>	Transmitter analog newer supply (left side)	GX, GS, GT	0.87	0.90	0.93	V
(2)	Transmitter analog power supply (left side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
		GX, GS, GT	0.82	0.85	0.88	V
V <sub>CCT GXBR</sub>	Transmitter analog newer supply (right side)		0.87	0.90	0.93	
(2) _	Transmitter analog power supply (light side)		0.97	1.0	1.03	
			1.03	1.05	1.07	
$V_{CCT_GTBR}$	Transmitter analog power supply for GT channels (right side)	GT	1.02	1.05	1.08	V
$V_{CCL\_GTBR}$	Transmitter clock network power supply	GT	1.02	1.05	1.08	V
V <sub>CCH_GXBL</sub>	Transmitter output buffer power supply (left side)	GX, GS, GT	1.425	1.5	1.575	V
V <sub>CCH_GXBR</sub>	Transmitter output buffer power supply (right side)	GX, GS, GT	1.425	1.5	1.575	V

Table 7.	<b>Recommended Transceiver Power Supply Operating Conditions for Stratix V GX</b> ,	<b>GS</b> , and <b>GT</b> Devices
(Part 2	of 2)	

### Notes to Table 7:

(1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.

(2) Refer to Table 8 to select the correct power supply level for your design.

(3) When using ATX PLLs, the supply must be 3.0 V.

(4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

**Table 8. Transceiver Power Supply Voltage Requirements** 

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB <sup>(2)</sup>	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true:	A11	1.05			
■ Data rate > 10.3 Gbps.	All	1.00			
<ul> <li>DFE is used.</li> </ul>					
If ANY of the following conditions are true <sup>(1)</sup> :			3.0		
<ul> <li>ATX PLL is used.</li> </ul>					
■ Data rate > 6.5Gbps.	All	1.0			
■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.				1.5	V
If ALL of the following	C1, C2, I2, and I3YY	0.90	2.5		
<ul> <li>ATX PLL is not used.</li> </ul>					
■ Data rate $\leq$ 6.5Gbps.	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		
<ul> <li>DFE, AEQ, and EyeQ are not used.</li> </ul>					

# Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR\_GXB and VCCT\_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR\_GXB and VCCT\_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

# **DC Characteristics**

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

#### **Supply Current**

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

			<b>Resistance Tolerance</b>				
Symbol	Description	Conditions	C1	C2,I2	C3, I3, I3YY	C4, I4	Unit
50-Ω R <sub>S</sub>	Internal series termination without calibration (50- $\Omega$ setting)	$V_{CCIO} = 1.8$ and 1.5 V	±30	±30	±40	±40	%
50-Ω R <sub>S</sub>	Internal series termination without calibration (50- $\Omega$ setting)	V <sub>CCI0</sub> = 1.2 V	±35	±35	±50	±50	%
100-Ω R <sub>D</sub>	Internal differential termination (100- $\Omega$ setting)	V <sub>CCPD</sub> = 2.5 V	±25	±25	±25	±25	%

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 2 of 2)

Calibration accuracy for the calibrated series and parallel OCTs are applicable at the moment of calibration. When voltage and temperature conditions change after calibration, the tolerance may change.

OCT calibration is automatically performed at power-up for OCT-enabled I/Os. Table 13 lists the OCT variation with temperature and voltage after power-up calibration. Use Table 13 to determine the OCT variation after power-up calibration and Equation 1 to determine the OCT variation without recalibration.

# Equation 1. OCT Variation Without Recalibration for Stratix V Devices (1), (2), (3), (4), (5), (6)

$$R_{OCT} \,=\, R_{SCAL} \Big( 1 + \langle \frac{dR}{dT} \times \Delta T \rangle \pm \langle \frac{dR}{dV} \times \Delta V \rangle \Big) \label{eq:ROCT}$$

#### Notes to Equation 1:

- (1) The  $R_{OCT}$  value shows the range of OCT resistance with the variation of temperature and  $V_{CCIO}$ .
- (2) R<sub>SCAL</sub> is the OCT resistance value at power-up.
- (3)  $\Delta T$  is the variation of temperature with respect to the temperature at power-up.
- (4)  $\Delta V$  is the variation of voltage with respect to the V<sub>CCIO</sub> at power-up.
- (5) dR/dT is the percentage change of  $R_{\text{SCAL}}$  with temperature.
- (6) dR/dV is the percentage change of  $\mathsf{R}_{\mathsf{SCAL}}$  with voltage.

Table 13 lists the on-chip termination variation after power-up calibration.

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 1 of 2)
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Symbol	Description	V <sub>CCIO</sub> (V)	Typical	Unit
dR/dV		3.0	0.0297	
	OCT variation with voltage without	2.5	0.0344	
		1.8	0.0499	%/mV
		1.5	0.0744	
		1.2	0.1241	

I/O Standard	V <sub>IL(DI</sub>	<sub>c)</sub> (V)	V <sub>IH(D</sub>	<sub>C)</sub> (V)	V <sub>IL(AC)</sub> (V)	V <sub>IH(AC)</sub> (V)	V <sub>ol</sub> (V)	V <sub>oh</sub> (V)	I (mA)	l <sub>oh</sub>
i/U Stanuaru	Min	Max	Min	Max	Max	Min	Max	Min	1 <sub>01</sub> (11174)	(mA)
HSTL-18 Class I	—	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	$V_{REF} - 0.2$	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	8	-8
HSTL-18 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-15 Class I	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCIO</sub> – 0.4	8	-8
HSTL-15 Class II	_	V <sub>REF</sub> – 0.1	V <sub>REF</sub> + 0.1	_	V <sub>REF</sub> - 0.2	V <sub>REF</sub> + 0.2	0.4	V <sub>CCI0</sub> – 0.4	16	-16
HSTL-12 Class I	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	8	-8
HSTL-12 Class II	-0.15	V <sub>REF</sub> - 0.08	V <sub>REF</sub> + 0.08	V <sub>CCIO</sub> + 0.15	V <sub>REF</sub> – 0.15	V <sub>REF</sub> + 0.15	0.25* V <sub>CCI0</sub>	0.75* V <sub>CCI0</sub>	16	-16
HSUL-12	—	V <sub>REF</sub> – 0.13	V <sub>REF</sub> + 0.13	_	V <sub>REF</sub> – 0.22	V <sub>REF</sub> + 0.22	0.1* V <sub>CCIO</sub>	0.9* V <sub>CCI0</sub>	_	

### Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

Table 20. Differential SSTL I/O Standards for Stratix V Devices

1/0 Standard	V <sub>CCIO</sub> (V)			V <sub>SWING(DC)</sub> (V)		V <sub>X(AC)</sub> (V)			V <sub>SWING(AC)</sub> (V)	
ijo Stalluaru	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V <sub>CCI0</sub> + 0.6	V <sub>CCI0</sub> /2- 0.2	_	V <sub>CCI0</sub> /2 + 0.2	0.62	V <sub>CCI0</sub> + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V <sub>CCIO</sub> + 0.6	V <sub>CCI0</sub> /2- 0.175	_	V <sub>CCI0</sub> /2 + 0.175	0.5	V <sub>CCI0</sub> + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	_	V <sub>CCI0</sub> /2 + 0.15	0.35	_
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCIO</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	2(V <sub>IL(AC)</sub> - V <sub>REF</sub> )
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	(1)	V <sub>CCI0</sub> /2- 0.15	V <sub>CCIO</sub> /2	V <sub>CCI0</sub> /2 + 0.15	2(V <sub>IH(AC)</sub> - V <sub>REF</sub> )	_
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	_	V <sub>REF</sub> 0.15	V <sub>CCI0</sub> /2	V <sub>REF</sub> + 0.15	-0.30	0.30

Note to Table 20:

(1) The maximum value for  $V_{SWING(DC)}$  is not defined. However, each single-ended signal needs to be within the respective single-ended limits  $(V_{IH(DC)} \text{ and } V_{IL(DC)})$ .

								•	-				
I/O	V <sub>CCIO</sub> (V)		V <sub>DIF(DC)</sub> (V)		V <sub>X(AC)</sub> (V)		V <sub>CM(DC)</sub> (V)			V <sub>DIF(/</sub>	<sub>AC)</sub> (V)		
Standard	Min	Тур	Max	Min	Max	Min	Тур	Max	Min	Тур	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	_	0.78	_	1.12	0.78	_	1.12	0.4	_
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	_	0.68	_	0.9	0.68		0.9	0.4	_

- You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
- **\*** For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.





Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Symbol/	Conditions	S	Transceive peed Grade	2	S	Fransceive Deed Grade	r 3	Unit
Description		Min	Тур	Max	Min	Тур	Max	
Differential on-chip termination resistors <sup>(7)</sup>	GT channels		100	_	_	100	_	Ω
	85- $\Omega$ setting	_	85 ± 30%	_	_	85 ± 30%	_	Ω
Differential on-chip	100-Ω setting	_	100 ± 30%	_	_	100 ± 30%	_	Ω
for GX channels <sup>(19)</sup>	120-Ω setting	_	120 ± 30%	_	—	120 ± 30%	—	Ω
	150-Ω setting	_	150 ± 30%	_	_	150 ± 30%	_	Ω
V <sub>ICM</sub> (AC coupled)	GT channels	_	650	_	—	650	—	mV
	VCCR_GXB = 0.85 V or 0.9 V	_	600	_	_	600	_	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 1.0 V full bandwidth	_	700		_	700	_	mV
	VCCR_GXB = 1.0 V half bandwidth	_	750	_	_	750	_	mV
t <sub>LTR</sub> <sup>(9)</sup>	—	_	—	10	—	—	10	μs
t <sub>LTD</sub> <sup>(10)</sup>		4			4	_	_	μs
t <sub>LTD_manual</sub> <sup>(11)</sup>		4	_		4	_	_	μs
t <sub>LTR_LTD_manual</sub> <sup>(12)</sup>	—	15	—	_	15	—	—	μs
Run Lenath	GT channels		—	72	—	—	72	CID
	GX channels				(8)			
CDR PPM	GT channels	_	—	1000	—	—	1000	± PPM
	GX channels				(8)			
Programmable	GT channels			14		_	14	dB
(AC Gain) <sup>(5)</sup>	GX channels				(8)			
Programmable	GT channels	_		7.5	_	_	7.5	dB
DC gain <sup>(6)</sup>	GX channels				(8)			
Differential on-chip termination resistors <sup>(7)</sup>	GT channels	_	100	—	_	100	_	Ω
Transmitter								
Supported I/O Standards	_			1.4-V	and 1.5-V P	CML		
Data rate (Standard PCS)	GX channels	600	_	8500	600		8500	Mbps
Data rate (10G PCS)	GX channels	600		12,500	600		12,500	Mbps

# Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5)<sup>(1)</sup>

	Table 28.	<b>Transceiver S</b>	pecifications	for Stratix V	GT Devices	(Part 4 of 5) (1)
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Symbol/	Conditions	s	Transceive peed Grade	r 2	ר Sp	Fransceive Deed Grade	r 3	Unit	
Description		Min	Тур	Max	Min	Тур	Max		
Data rate	GT channels	19,600	_	28,050	19,600		25,780	Mbps	
Differential on-chip	GT channels	_	100	—		100	_	Ω	
termination resistors	GX channels				(8)				
	GT channels	_	500	_		500	_	mV	
V <sub>OCM</sub> (AC Coupled)	GX channels		•	•	(8)		•		
Dice/Fell time	GT channels	_	15	—	—	15	—	ps	
Rise/Fail lime	GX channels				(8)				
Intra-differential pair skew	GX channels				(8)				
Intra-transceiver block transmitter channel-to- channel skew	GX channels		(8)						
Inter-transceiver block transmitter channel-to- channel skew	GX channels	(8)							
CMU PLL									
Supported Data Range	—	600		12500	600		8500	Mbps	
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs	
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs	
ATX PLL									
	VCO post- divider L=2	8000	_	12500	8000	_	8500	Mbps	
	L=4	4000	—	6600	4000	_	6600	Mbps	
Supported Data Rate	L=8	2000	—	3300	2000	_	3300	Mbps	
Range for GX Channels	L=8, Local/Central Clock Divider =2	1000	_	1762.5	1000	_	1762.5	Mbps	
Supported Data Rate Range for GT Channels	VCO post- divider L=2	9800	_	14025	9800	_	12890	Mbps	
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	_	—	μs	
t <sub>pll_lock</sub> <sup>(14)</sup>	—	_	—	10	_	_	10	μs	
fPLL									
Supported Data Range		600		3250/ 3.125 <sup>(23)</sup>	600		3250/ 3.125 <sup>(23)</sup>	Mbps	
t <sub>pll_powerdown</sub> <sup>(13)</sup>	—	1	—	—	1	—	—	μs	

- XFI
- ASI
- HiGig/HiGig+
- HiGig2/HiGig2+
- Serial Data Converter (SDC)
- GPON
- SDI
- SONET
- Fibre Channel (FC)
- PCIe
- QPI
- SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

# **Core Performance Specifications**

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

# **Clock Tree Specifications**

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices (1)

	Performance						
Symbol	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	Unit			
Global and Regional Clock	717	650	580	MHz			
Periphery Clock	550	500	500	MHz			

### Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Symbol	Parameter	Min	Тур	Max	Unit
+ (3) (4)	Input clock cycle-to-cycle jitter ( $f_{REF} \ge 100 \text{ MHz}$ )			0.15	UI (p-p)
LINCCJ (0), (1)	Input clock cycle-to-cycle jitter (f <sub>REF</sub> < 100 MHz)	-750		+750	ps (p-p)
+ (5)	Period Jitter for dedicated clock output (f_{OUT} $\geq$ 100 MHz)	_	_	175 <sup>(1)</sup>	ps (p-p)
CUTPJ_DC	Period Jitter for dedicated clock output (f <sub>OUT</sub> < 100 MHz)	_	_	17.5 <sup>(1)</sup>	mUI (p-p)
+ (5)	Period Jitter for dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTPJ_DC	Period Jitter for dedicated clock output in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
+ (5)	Cycle-to-Cycle Jitter for a dedicated clock output ( $f_{\text{OUT}} \geq 100 \text{ MHz})$		_	175	ps (p-p)
COUTCCJ_DC	Cycle-to-Cycle Jitter for a dedicated clock output $(f_{OUT} < 100 \text{ MHz})$		_	17.5	mUI (p-p)
+ (5)	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	250 <sup>(11)</sup> , 175 <sup>(12)</sup>	ps (p-p)
FOUTCCJ_DC	Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ( $f_{OUT} < 100 \text{ MHz}$ )+		_	25 <sup>(11)</sup> , 17.5 <sup>(12)</sup>	mUI (p-p)
t <sub>outpj 10</sub> (5),	Period Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )		_	600	ps (p-p)
(8)	Period Jitter for a clock output on a regular I/O $(f_{OUT} < 100 \text{ MHz})$		_	60	mUI (p-p)
t <sub>foutpj 10</sub> <sup>(5),</sup>	Period Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Period Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>outccj_io</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ( $f_{OUT} \geq 100 \mbox{ MHz})$	_	_	600	ps (p-p)
(8)	Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60 <sup>(10)</sup>	mUI (p-p)
t <sub>FOUTCCJ 10</sub> (5),	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ( $f_{OUT} \ge 100$ MHz)		_	600 <sup>(10)</sup>	ps (p-p)
(8), (11)	Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL (f <sub>OUT</sub> < 100 MHz)	_	_	60	mUI (p-p)
t <sub>CASC OUTPJ DC</sub>	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT} \ge 100 \text{ MHz}$ )	_	_	175	ps (p-p)
(5), (6)	Period Jitter for a dedicated clock output in cascaded PLLs ( $f_{OUT}$ < 100 MHz)	_	_	17.5	mUI (p-p)
f <sub>DRIFT</sub>	Frequency drift after PFDENA is disabled for a duration of 100 $\mu s$		_	±10	%
dK <sub>BIT</sub>	Bit number of Delta Sigma Modulator (DSM)	8	24	32	Bits
k <sub>VALUE</sub>	Numerator of Fraction	128	8388608	2147483648	—

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

### Table 31. PLL Specifications for Stratix V Devices (Part 3 of 3)

Symbol	Parameter	Min	Тур	Max	Unit
f <sub>RES</sub>	Resolution of VCO frequency ( $f_{INPFD} = 100 \text{ MHz}$ )	390625	5.96	0.023	Hz

#### Notes to Table 31:

(1) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(2) This specification is limited by the lower of the two: I/O  $f_{MAX}$  or  $f_{OUT}$  of the PLL.

- (3) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.
- (4)  $f_{REF}$  is fIN/N when N = 1.
- (5) Peak-to-peak jitter with a probability level of 10<sup>-12</sup> (14 sigma, 99.9999999974404% confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 44 on page 52.
- (6) The cascaded PLL specification is only applicable with the following condition: a. Upstream PLL: 0.59Mhz ≤ Upstream PLL BW < 1 MHz b. Downstream PLL: Downstream PLL BW > 2 MHz
- (7) High bandwidth PLL settings are not supported in external feedback mode.
- (8) The external memory interface clock output jitter specifications use a different measurement method, which is available in Table 42 on page 50.
- (9) The VCO frequency reported by the Quartus II software in the PLL Usage Summary section of the compilation report takes into consideration the VCO post-scale counter K value. Therefore, if the counter K has a value of 2, the frequency reported can be lower than the f<sub>VCO</sub> specification.
- (10) This specification only covers fractional PLL for low bandwidth. The  $f_{VCO}$  for fractional value range 0.05 0.95 must be  $\geq$  1000 MHz, while  $f_{VCO}$  for fractional value range 0.20 0.80 must be  $\geq$  1200 MHz.
- (11) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.05-0.95 must be  $\geq$  1000 MHz.
- (12) This specification only covered fractional PLL for low bandwidth. The  $f_{VC0}$  for fractional value range 0.20-0.80 must be  $\geq$  1200 MHz.

# **DSP Block Specifications**

Table 32 lists the Stratix V DSP block performance specifications.

			F	Peformanc	e			
Mode	C1	C2, C2L	12, 12L	C3	13, 13L, 13YY	C4	14	Unit
		Modes ı	using one	DSP				
Three 9 x 9	600	600	600	480	480	420	420	MHz
One 18 x 18	600	600	600	480	480	420	400	MHz
Two partial 18 x 18 (or 16 x 16)	600	600	600	480	480	420	400	MHz
One 27 x 27	500	500	500	400	400	350	350	MHz
One 36 x 18	500	500	500	400	400	350	350	MHz
One sum of two 18 x 18(One sum of 2 16 x 16)	500	500	500	400	400	350	350	MHz
One sum of square	500	500	500	400	400	350	350	MHz
One 18 x 18 plus 36 (a x b) + c	500	500	500	400	400	350	350	MHz
		Modes u	sing two l	DSPs				
Three 18 x 18	500	500	500	400	400	350	350	MHz
One sum of four 18 x 18	475	475	475	380	380	300	300	MHz
One sum of two 27 x 27	465	465	450	380	380	300	290	MHz
One sum of two 36 x 18	475	475	475	380	380	300	300	MHz
One complex 18 x 18	500	500	500	400	400	350	350	MHz
One 36 x 36	475	475	475	380	380	300	300	MHz

### Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 1 of 2)

		<b>Resources Used</b>				Ρε	erforman	ce			
Memory	Mode	ALUTS	Memory	C1	C2, C2L	C3	C4	12, 12L	13, 13L, 13YY	14	Unit
	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to <b>Old Data</b> , all supported widths	0	1	525	525	455	400	525	455	400	MHz
M20K Block	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

# Table 33. Memory Block Performance Specifications for Stratix V Devices <sup>(1), (2)</sup> (Part 2 of 2)

### Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50**% output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F<sub>MAX</sub>.

(3) The F<sub>MAX</sub> specification is only achievable with Fitter options, MLAB Implementation In 16-Bit Deep Mode enabled.

# **Temperature Sensing Diode Specifications**

Table 34 lists the internal TSD specification.

#### **Table 34. Internal Temperature Sensing Diode Specification**

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
-40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35.	External	Temperature	Sensing Dic	de Specifica	ations for Stratix	V Devices
-----------	----------	-------------	-------------	--------------	--------------------	-----------

Description	Min	Тур	Max	Unit
I <sub>bias</sub> , diode source current	8	—	200	μA
V <sub>bias,</sub> voltage across diode	0.3	—	0.9	V
Series resistance	—	_	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	_

# **Periphery Performance**

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

# **High-Speed I/O Specification**

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 1 of 4)

	Sumbol	Conditions		C1		C2,	C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,14		
Symbol		Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UNIT
	f <sub>HSCLK_in</sub> (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	800	5		800	5		625	5		525	MHz
	f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards <sup>(3)</sup>	Clock boost factor W = 1 to 40 $^{(4)}$	5		800	5		800	5		625	5		525	MHz
	f <sub>HSCLK_in</sub> (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 $^{(4)}$	5	_	520	5		520	5	_	420	5	_	420	MHz
f <sub>HSCLK_OUT</sub> (output clock — frequency)		5	_	800	5	_	800	5	_	625 (5)	5	_	525 (5)	MHz	

Symbol	Conditiono		C1		C2,	C2L, I	2, I2L	C3,	13, 131	., I <b>3</b> YY	C4,14			Unit
əynnuu	Conditions	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	UIIIL
Transmitter														
	SERDES factor J = 3 to 10 <sup>(9)</sup> , <sup>(11)</sup> , <sup>(12)</sup> , <sup>(13)</sup> , <sup>(14)</sup> , <sup>(15)</sup> , <sup>(16)</sup>	(6)	_	1600	(6)	_	1434	(6)	_	1250	(6)	_	1050	Mbps
True Differential I/O Standards	SERDES factor J $\geq 4$ LVDS TX with DPA (12), (14), (15), (16)	(6)		1600	(6)		1600	(6)		1600	(6)	_	1250	Mbps
- f <sub>HSDR</sub> (data rate)	SERDES factor J = 2, uses DDR Registers	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
	SERDES factor J = 1, uses SDR Register	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	(6)	_	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f <sub>HSDR</sub> (data rate) <sup>(10)</sup>	SERDES factor J = 4 to 10 $(^{17})$	(6)		1100	(6)		1100	(6)		840	(6)		840	Mbps
t <sub>x Jitter</sub> - True Differential	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps		_	160		_	160		_	160			160	ps
I/O Standards	Total Jitter for Data Rate < 600 Mbps		_	0.1			0.1			0.1		_	0.1	UI
t <sub>x Jitter</sub> - Emulated Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	_	_	300	_	_	300	_	_	300	_		325	ps
with Three External Output Resistor Network	Total Jitter for Data Rate < 600 Mbps	_	_	0.2	_	_	0.2	_	_	0.2	_	_	0.25	UI

# Table 36. High-Speed I/O Specifications for Stratix V Devices (1), (2) (Part 2 of 4)

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled

rx_reset			
rx_dpa_locked			
-			

Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions <sup>(4)</sup>	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Missellansous	10101010	8	32	640 data transitions
Wiscenareous	01010101	8	32	640 data transitions

#### Notes to Table 37:

(1) The DPA lock time is for one channel.

(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.

(3) The DPA lock time stated in this table applies to both commercial and industrial grade.

(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the **LVDS** soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps. Table 38 lists the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate  $\geq$  1.25 Gbps.





# **Remote System Upgrades**

Table 56 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 56. Remote System Upgrade Circuitry Timing Specificatio
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Parameter	Minimum	Maximum	Unit
t <sub>RU_nCONFIG</sub> <sup>(1)</sup>	250	—	ns
t <sub>RU_nRSTIMER</sub> <sup>(2)</sup>	250	_	ns

#### Notes to Table 56:

- (1) This is equivalent to strobing the reconfiguration input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the Remote System Upgrade State Machine section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (2) This is equivalent to strobing the reset\_timer input of the ALTREMOTE\_UPDATE megafunction high for the minimum timing specification. For more information, refer to the User Watchdog Timer section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

# **User Watchdog Internal Circuitry Timing Specification**

Table 57 lists the operating range of the 12.5-MHz internal oscillator.

#### Table 57. 12.5-MHz Internal Oscillator Specifications

Minimum	Typical	Maximum	Units
5.3	7.9	12.5	MHz

# I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

 You can download the Excel-based I/O Timing spreadsheet from the Stratix V Devices Documentation web page.

# **Programmable IOE Delay**

Table 58 lists the Stratix V IOE programmable delay settings.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 1 of 2)

Deremeter	Available Min Fast Model Slow							Slow N	lodel			
(1)	Available Settings	0ffset (2)	Industrial	Commercial	C1	C2	C3	C4	12	13, 13YY	14	Unit
D1	64	0	0.464	0.493	0.838	0.838	0.924	1.011	0.844	0.921	1.006	ns
D2	32	0	0.230	0.244	0.415	0.415	0.459	0.503	0.417	0.456	0.500	ns

# Table 60. Glossary (Part 2 of 4)

Letter	Subject	Definitions
G H I	JTAG Timing Specifications	High-speed I/O block—Deserialization factor (width of parallel data bus). JTAG Timing Specifications: TMS
K L M N O		
Ρ	PLL Specifications	Diagram of PLL Specifications (1)
Q	_	—
R	RL	Receiver differential input discrete resistor (external to the Stratix V device).

# **Document Revision History**

Table 61 lists the revision history for this chapter.

 Table 61. Document Revision History (Part 1 of 3)

Date	Version	Changes				
June 2018	3.9	<ul> <li>Added the "Stratix V Device Overshoot Duration" figure.</li> </ul>				
		Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.				
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "PS Timing Parameters for Stratix V Devices" table.</li> </ul>				
	3.8					<ul> <li>Changed the condition for 100-Ω R<sub>D</sub> in the "OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices" table.</li> </ul>
April 2017		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table</li> </ul>				
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>				
		<ul> <li>Changed the minimum value for t<sub>CD2UMC</sub> in the "FPP Timing Parameters for Stratix V Devices When the DCLK-to-DATA[] Ratio is &gt;1" table.</li> </ul>				
		<ul> <li>Changed the minimum number of clock cycles value in the "Initialization Clock Source Option and the Maximum Frequency" table.</li> </ul>				
June 2016	2.7	<ul> <li>Added the V<sub>ID</sub> minimum specification for LVPECL in the "Differential I/O Standard Specifications for Stratix V Devices" table</li> </ul>				
	0.7	<ul> <li>Added the I<sub>OUT</sub> specification to the "Absolute Maximum Ratings for Stratix V Devices" table.</li> </ul>				
December 2015	3.6	Added a footnote to the "High-Speed I/O Specifications for Stratix V Devices" table.				
December 2015	3.5	<ul> <li>Changed the transmitter, receiver, and ATX PLL data rate specifications in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>				
	5.5	<ul> <li>Changed the configuration .rbf sizes in the "Uncompressed .rbf Sizes for Stratix V Devices" table.</li> </ul>				
		• Changed the data rate specification for transceiver speed grade 3 in the following tables:				
		<ul> <li>"Transceiver Specifications for Stratix V GX and GS Devices"</li> </ul>				
		<ul> <li>"Stratix V Standard PCS Approximate Maximum Date Rate"</li> </ul>				
		<ul> <li>"Stratix V 10G PCS Approximate Maximum Data Rate"</li> </ul>				
July 2015	3.4	<ul> <li>Changed the conditions for reference clock rise and fall time, and added a note to the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>				
		<ul> <li>Added a note to the "Minimum differential eye opening at receiver serial input pins" specification in the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>				
		<ul> <li>Changed the t<sub>c0</sub> maximum value in the "AS Timing Parameters for AS '1 and AS '4 Configurations in Stratix V Devices" table.</li> </ul>				
		<ul> <li>Removed the CDR ppm tolerance specification from the "Transceiver Specifications for Stratix V GX and GS Devices" table.</li> </ul>				

 Table 61. Document Revision History (Part 3 of 3)

Date	Version	Changes	
		■ Updated Table 2, Table 6, Table 7, Table 20, Table 23, Table 27, Table 47, Table 60	
May 2013	2.7	Added Table 24, Table 48	
		<ul> <li>Updated Figure 9, Figure 10, Figure 11, Figure 12</li> </ul>	
February 2013	2.6	<ul> <li>Updated Table 7, Table 9, Table 20, Table 23, Table 27, Table 30, Table 31, Table 35, Table 46</li> </ul>	
		Updated "Maximum Allowed Overshoot and Undershoot Voltage"	
		<ul> <li>Updated Table 3, Table 6, Table 7, Table 8, Table 23, Table 24, Table 25, Table 27, Table 30, Table 32, Table 35</li> </ul>	
		Added Table 33	
		<ul> <li>Added "Fast Passive Parallel Configuration Timing"</li> </ul>	
		<ul> <li>Added "Active Serial Configuration Timing"</li> </ul>	
December 2012	2.5	<ul> <li>Added "Passive Serial Configuration Timing"</li> </ul>	
		<ul> <li>Added "Remote System Upgrades"</li> </ul>	
		<ul> <li>Added "User Watchdog Internal Circuitry Timing Specification"</li> </ul>	
		Added "Initialization"	
		Added "Raw Binary File Size"	
	2.4	<ul> <li>Added Figure 1, Figure 2, and Figure 3.</li> </ul>	
June 2012		2.4	<ul> <li>Updated Table 1, Table 2, Table 3, Table 6, Table 11, Table 22, Table 23, Table 27, Table 29, Table 30, Table 31, Table 32, Table 35, Table 38, Table 39, Table 40, Table 41, Table 43, Table 56, and Table 59.</li> </ul>
			<ul> <li>Various edits throughout to fix bugs.</li> </ul>
			Changed title of document to <i>Stratix V Device Datasheet</i> .
		<ul> <li>Removed document from the Stratix V handbook and made it a separate document.</li> </ul>	
February 2012	2.3	■ Updated Table 1–22, Table 1–29, Table 1–31, and Table 1–31.	
December 2011	22	■ Added Table 2–31.	
December 2011	2.2	■ Updated Table 2–28 and Table 2–34.	
	0.1	<ul> <li>Added Table 2–2 and Table 2–21 and updated Table 2–5 with information about Stratix V GT devices.</li> </ul>	
November 2011	2.1	<ul> <li>Updated Table 2–11, Table 2–13, Table 2–20, and Table 2–25.</li> </ul>	
		<ul> <li>Various edits throughout to fix SPRs.</li> </ul>	
		■ Updated Table 2–4, Table 2–18, Table 2–19, Table 2–21, Table 2–22, Table 2–23, and Table 2–24.	
May 2011	2.0	<ul> <li>Updated the "DQ Logic Block and Memory Output Clock Jitter Specifications" title.</li> </ul>	
		Chapter moved to Volume 1.	
		<ul> <li>Minor text edits.</li> </ul>	
		■ Updated Table 1–2, Table 1–4, Table 1–19, and Table 1–23.	
December 2010	1.1	<ul> <li>Converted chapter to the new template.</li> </ul>	
		<ul> <li>Minor text edits.</li> </ul>	
July 2010	1.0	Initial release.	