



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 359200 |
| Number of Logic Elements/Cells | 952000 |
| Total RAM Bits | 53248000 |
| Number of I/O | 696 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 1517-BBGA, FCBGA |
| Supplier Device Package | 1517-HBGA (45x45) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxmabk3h40i4n |

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Condition | Min ⁽⁴⁾ | Typ | Max ⁽⁴⁾ | Unit |
|-----------------------------------|---|------------|--------------------|------|--------------------|------|
| V _{CC} | Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades) | — | 0.87 | 0.9 | 0.93 | V |
| | Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) ⁽³⁾ | — | 0.82 | 0.85 | 0.88 | V |
| V _{CCPT} | Power supply for programmable power technology | — | 1.45 | 1.50 | 1.55 | V |
| V _{CC_AUX} | Auxiliary supply for the programmable power technology | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCPD} ⁽¹⁾ | I/O pre-driver (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O pre-driver (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCIO} | I/O buffers (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | I/O buffers (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | I/O buffers (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| | I/O buffers (1.5 V) power supply | — | 1.425 | 1.5 | 1.575 | V |
| | I/O buffers (1.35 V) power supply | — | 1.283 | 1.35 | 1.45 | V |
| | I/O buffers (1.25 V) power supply | — | 1.19 | 1.25 | 1.31 | V |
| | I/O buffers (1.2 V) power supply | — | 1.14 | 1.2 | 1.26 | V |
| V _{CCPGM} | Configuration pins (3.0 V) power supply | — | 2.85 | 3.0 | 3.15 | V |
| | Configuration pins (2.5 V) power supply | — | 2.375 | 2.5 | 2.625 | V |
| | Configuration pins (1.8 V) power supply | — | 1.71 | 1.8 | 1.89 | V |
| V _{CCA_FPLL} | PLL analog voltage regulator power supply | — | 2.375 | 2.5 | 2.625 | V |
| V _{CCD_FPLL} | PLL digital voltage regulator power supply | — | 1.45 | 1.5 | 1.55 | V |
| V _{CCBAT} ⁽²⁾ | Battery back-up power supply (For design security volatile key register) | — | 1.2 | — | 3.0 | V |
| V _I | DC input voltage | — | −0.5 | — | 3.6 | V |
| V _O | Output voltage | — | 0 | — | V _{CCIO} | V |
| T _J | Operating junction temperature | Commercial | 0 | — | 85 | °C |
| | | Industrial | −40 | — | 100 | °C |

Internal Weak Pull-Up Resistor

Table 16 lists the weak pull-up resistor values for Stratix V devices.

Table 16. Internal Weak Pull-Up Resistor for Stratix V Devices ^{(1), (2)}

| Symbol | Description | V _{CCIO} Conditions (V) ⁽³⁾ | Value ⁽⁴⁾ | Unit |
|-----------------|---|---|----------------------|------|
| R _{PU} | Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you enable the programmable pull-up resistor option. | 3.0 ±5% | 25 | kΩ |
| | | 2.5 ±5% | 25 | kΩ |
| | | 1.8 ±5% | 25 | kΩ |
| | | 1.5 ±5% | 25 | kΩ |
| | | 1.35 ±5% | 25 | kΩ |
| | | 1.25 ±5% | 25 | kΩ |
| | | 1.2 ±5% | 25 | kΩ |

Notes to Table 16:

- (1) All I/O pins have an option to enable the weak pull-up resistor except the configuration, test, and JTAG pins.
- (2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.
- (3) The pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.
- (4) These specifications are valid with a ±10% tolerance to cover changes over PVT.

I/O Standard Specifications

Table 17 through Table 22 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Stratix V devices. These tables also show the Stratix V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of the terms used in Table 17 through Table 22, refer to “Glossary” on page 65. For tolerance calculations across all SSTL and HSTL I/O standards, refer to Altera knowledge base solution rd07262012_486.

Table 17. Single-Ended I/O Standards for Stratix V Devices

| I/O Standard | V _{CCIO} (V) | | | V _{IL} (V) | | V _{IH} (V) | | V _{OL} (V) | V _{OH} (V) | I _{OL} (mA) | I _{OH} (mA) |
|--------------|-----------------------|-----|-------|---------------------|-----------------------------|-----------------------------|-------------------------|-----------------------------|-----------------------------|----------------------|----------------------|
| | Min | Typ | Max | Min | Max | Min | Max | Max | Min | | |
| LVTTTL | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.4 | 2.4 | 2 | −2 |
| LVC MOS | 2.85 | 3 | 3.15 | −0.3 | 0.8 | 1.7 | 3.6 | 0.2 | V _{CCIO} − 0.2 | 0.1 | −0.1 |
| 2.5 V | 2.375 | 2.5 | 2.625 | −0.3 | 0.7 | 1.7 | 3.6 | 0.4 | 2 | 1 | −1 |
| 1.8 V | 1.71 | 1.8 | 1.89 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.45 | V _{CCIO} − 0.45 | 2 | −2 |
| 1.5 V | 1.425 | 1.5 | 1.575 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.25 * V _{CCIO} | 0.75 * V _{CCIO} | 2 | −2 |
| 1.2 V | 1.14 | 1.2 | 1.26 | −0.3 | 0.35 * V _{CCIO} | 0.65 * V _{CCIO} | V _{CCIO} + 0.3 | 0.25 * V _{CCIO} | 0.75 * V _{CCIO} | 2 | −2 |

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

| I/O Standard | $V_{IL(DC)}$ (V) | | $V_{IH(DC)}$ (V) | | $V_{IL(AC)}$ (V) | $V_{IH(AC)}$ (V) | V_{OL} (V) | V_{OH} (V) | I_{ol} (mA) | I_{oh} (mA) |
|------------------|------------------|------------------|------------------|-------------------|------------------|------------------|-------------------|-------------------|---------------|---------------|
| | Min | Max | Min | Max | Max | Min | Max | Min | | |
| HSTL-18 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-18 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-15 Class I | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 8 | -8 |
| HSTL-15 Class II | — | $V_{REF} - 0.1$ | $V_{REF} + 0.1$ | — | $V_{REF} - 0.2$ | $V_{REF} + 0.2$ | 0.4 | $V_{CCIO} - 0.4$ | 16 | -16 |
| HSTL-12 Class I | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 8 | -8 |
| HSTL-12 Class II | -0.15 | $V_{REF} - 0.08$ | $V_{REF} + 0.08$ | $V_{CCIO} + 0.15$ | $V_{REF} - 0.15$ | $V_{REF} + 0.15$ | $0.25^* V_{CCIO}$ | $0.75^* V_{CCIO}$ | 16 | -16 |
| HSUL-12 | — | $V_{REF} - 0.13$ | $V_{REF} + 0.13$ | — | $V_{REF} - 0.22$ | $V_{REF} + 0.22$ | $0.1^* V_{CCIO}$ | $0.9^* V_{CCIO}$ | — | — |

Table 20. Differential SSTL I/O Standards for Stratix V Devices



| I/O Standard | V_{CCIO} (V) | | | $V_{SWING(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{SWING(AC)}$ (V) | |
|----------------------|----------------|------|-------|---------------------|------------------|----------------------|--------------|----------------------|---------------------------|---------------------------|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Max |
| SSTL-2 Class I, II | 2.375 | 2.5 | 2.625 | 0.3 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.2$ | — | $V_{CCIO}/2 + 0.2$ | 0.62 | $V_{CCIO} + 0.6$ |
| SSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.25 | $V_{CCIO} + 0.6$ | $V_{CCIO}/2 - 0.175$ | — | $V_{CCIO}/2 + 0.175$ | 0.5 | $V_{CCIO} + 0.6$ |
| SSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | (1) | $V_{CCIO}/2 - 0.15$ | — | $V_{CCIO}/2 + 0.15$ | 0.35 | — |
| SSTL-135 Class I, II | 1.283 | 1.35 | 1.45 | 0.2 | (1) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | $2(V_{IL(AC)} - V_{REF})$ |
| SSTL-125 Class I, II | 1.19 | 1.25 | 1.31 | 0.18 | (1) | $V_{CCIO}/2 - 0.15$ | $V_{CCIO}/2$ | $V_{CCIO}/2 + 0.15$ | $2(V_{IH(AC)} - V_{REF})$ | — |
| SSTL-12 Class I, II | 1.14 | 1.2 | 1.26 | 0.18 | — | $V_{REF} - 0.15$ | $V_{CCIO}/2$ | $V_{REF} + 0.15$ | -0.30 | 0.30 |

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)

| I/O Standard | V_{CCIO} (V) | | | $V_{DIF(DC)}$ (V) | | $V_{X(AC)}$ (V) | | | $V_{CM(DC)}$ (V) | | | $V_{DIF(AC)}$ (V) | |
|---------------------|----------------|-----|-------|-------------------|-----|-----------------|-----|------|------------------|-----|------|-------------------|-----|
| | Min | Typ | Max | Min | Max | Min | Typ | Max | Min | Typ | Max | Min | Max |
| HSTL-18 Class I, II | 1.71 | 1.8 | 1.89 | 0.2 | — | 0.78 | — | 1.12 | 0.78 | — | 1.12 | 0.4 | — |
| HSTL-15 Class I, II | 1.425 | 1.5 | 1.575 | 0.2 | — | 0.68 | — | 0.9 | 0.68 | — | 0.9 | 0.4 | — |

-
-  You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
-  For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as “Preliminary.”
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 1 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|---|---|-----|-----|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Input Reference Clock Frequency (CMU PLL) ⁽⁸⁾ | — | 40 | — | 710 | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) ⁽⁸⁾ | — | 100 | — | 710 | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | Measure at ±60 mV of differential signal ⁽²⁶⁾ | — | — | 400 | — | — | 400 | — | — | 400 | ps |
| Fall time | Measure at ±60 mV of differential signal ⁽²⁶⁾ | — | — | 400 | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express® (PCIe®) | 30 | — | 33 | 30 | — | 33 | 30 | — | 33 | kHz |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 3 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|--|-----|-------|------------------------------|-----|-------|------------------------------|-----|-------------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Reconfiguration clock (<code>mgmt_clk_clk</code>) frequency | — | 100 | — | 125 | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | | | | |
| Data rate (Standard PCS) ^{(9), (23)} | — | 600 | — | 12200 | 600 | — | 12200 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| Data rate (10G PCS) ^{(9), (23)} | — | 600 | — | 14100 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| Absolute V_{MAX} for a receiver pin ⁽⁵⁾ | — | — | — | 1.2 | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V_{MIN} for a receiver pin | — | −0.4 | — | — | −0.4 | — | — | −0.4 | — | — | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) before device configuration ⁽²²⁾ | — | — | — | 1.6 | — | — | 1.6 | — | — | 1.6 | V |
| Maximum peak- to-peak differential input voltage V_{ID} (diff p- p) after device configuration ^{(18), (22)} | $V_{CCR_GXB} = 1.0\text{ V}/1.05\text{ V}$ ($V_{ICM} = 0.70\text{ V}$) | — | — | 2.0 | — | — | 2.0 | — | — | 2.0 | V |
| | $V_{CCR_GXB} = 0.90\text{ V}$ ($V_{ICM} = 0.6\text{ V}$) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| | $V_{CCR_GXB} = 0.85\text{ V}$ ($V_{ICM} = 0.6\text{ V}$) | — | — | 2.4 | — | — | 2.4 | — | — | 2.4 | V |
| Minimum differential eye opening at receiver serial input pins ^{(6), (22), (27)} | — | 85 | — | — | 85 | — | — | 85 | — | — | mV |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 6 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|--|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------|------------------------------|-----|-------------------------------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Inter-transceiver block transmitter channel-to- channel skew | xN PMA bonded mode | — | — | 500 | — | — | 500 | — | — | 500 | ps |
| CMU PLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 12500 | 600 | — | 12500 | 600 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| ATX PLL | | | | | | | | | | | |
| Supported Data Rate Range | VCO post-divider L=2 | 8000 | — | 14100 | 8000 | — | 12500 | 8000 | — | 8500/ 10312.5 ⁽²⁴⁾ | Mbps |
| | L=4 | 4000 | — | 7050 | 4000 | — | 6600 | 4000 | — | 6600 | Mbps |
| | L=8 | 2000 | — | 3525 | 2000 | — | 3300 | 2000 | — | 3300 | Mbps |
| | L=8, Local/Central Clock Divider =2 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | 1000 | — | 1762.5 | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |
| t _{pll_lock} ⁽¹⁶⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| fPLL | | | | | | | | | | | |
| Supported Data Range | — | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | 600 | — | 3250/ 3125 ⁽²⁵⁾ | Mbps |
| t _{pll_powerdown} ⁽¹⁵⁾ | — | 1 | — | — | 1 | — | — | 1 | — | — | μs |

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 7 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $t_{pll_lock}^{(16)}$ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |

Notes to Table 23:

- (1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.
- (3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.
- (4) This supply follows $VCCR_GXB$.
- (5) The device cannot tolerate prolonged operation at this absolute maximum.
- (6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.
- (8) The input reference clock frequency options depend on the data rate and the device speed grade.
- (9) The line data rate may be limited by PCS-FPGA interface speed grade.
- (10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.
- (13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.
- (14) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.
- (15) $t_{pll_powerdown}$ is the PLL powerdown minimum pulse width.
- (16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz \times 100/f.
- (18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (19) For ES devices, R_{REF} is $2000 \Omega \pm 1\%$.
- (20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + $20 \times \log(f/622)$.
- (21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100Ω . The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (22) Refer to Figure 2.
- (23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (24) I3YY devices can achieve data rates up to 10.3125 Gbps.
- (25) When you use fPLL as a TXPLL of the transceiver.
- (26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.
- (27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 1 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|--|--|-----------|------|------------------------------|-----------|------|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Reference Clock | | | | | | | | |
| Supported I/O Standards | Dedicated reference clock pin | 1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL | | | | | | |
| | RX reference clock pin | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Input Reference Clock Frequency (CMU PLL) ⁽⁶⁾ | — | 40 | — | 710 | 40 | — | 710 | MHz |
| Input Reference Clock Frequency (ATX PLL) ⁽⁶⁾ | — | 100 | — | 710 | 100 | — | 710 | MHz |
| Rise time | 20% to 80% | — | — | 400 | — | — | 400 | ps |
| Fall time | 80% to 20% | — | — | 400 | — | — | 400 | |
| Duty cycle | — | 45 | — | 55 | 45 | — | 55 | % |
| Spread-spectrum modulating clock frequency | PCI Express (PCIe) | 30 | — | 33 | 30 | — | 33 | kHz |
| Spread-spectrum downspread | PCIe | — | 0 to −0.5 | — | — | 0 to −0.5 | — | % |
| On-chip termination resistors ⁽¹⁹⁾ | — | — | 100 | — | — | 100 | — | Ω |
| Absolute V _{MAX} ⁽³⁾ | Dedicated reference clock pin | — | — | 1.6 | — | — | 1.6 | V |
| | RX reference clock pin | — | — | 1.2 | — | — | 1.2 | |
| Absolute V _{MIN} | — | -0.4 | — | — | -0.4 | — | — | V |
| Peak-to-peak differential input voltage | — | 200 | — | 1600 | 200 | — | 1600 | mV |
| V _{ICM} (AC coupled) | Dedicated reference clock pin | 1050/1000 ⁽²⁾ | | | 1050/1000 ⁽²⁾ | | | mV |
| | RX reference clock pin | 1.0/0.9/0.85 ⁽²²⁾ | | | 1.0/0.9/0.85 ⁽²²⁾ | | | V |
| V _{ICM} (DC coupled) | HCSL I/O standard for PCIe reference clock | 250 | — | 550 | 250 | — | 550 | mV |

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---|---|--|---------------|--------|------------------------------|---------------|--------|----------|
| | | Min | Typ | Max | Min | Typ | Max | |
| Transmitter REFCLK Phase Noise (622 MHz) ⁽¹⁸⁾ | 100 Hz | — | — | -70 | — | — | -70 | dBc/Hz |
| | 1 kHz | — | — | -90 | — | — | -90 | |
| | 10 kHz | — | — | -100 | — | — | -100 | |
| | 100 kHz | — | — | -110 | — | — | -110 | |
| | ≥ 1 MHz | — | — | -120 | — | — | -120 | |
| Transmitter REFCLK Phase Jitter (100 MHz) ⁽¹⁵⁾ | 10 kHz to 1.5 MHz (PCIe) | — | — | 3 | — | — | 3 | ps (rms) |
| RREF ⁽¹⁷⁾ | — | — | 1800 ± 1% | — | — | 1800 ± 1% | — | Ω |
| Transceiver Clocks | | | | | | | | |
| fixedclk clock frequency | PCIe Receiver Detect | — | 100 or 125 | — | — | 100 or 125 | — | MHz |
| Reconfiguration clock (mgmt_clk_clk) frequency | — | 100 | — | 125 | 100 | — | 125 | MHz |
| Receiver | | | | | | | | |
| Supported I/O Standards | — | 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS | | | | | | |
| Data rate (Standard PCS) ⁽²¹⁾ | GX channels | 600 | — | 8500 | 600 | — | 8500 | Mbps |
| Data rate (10G PCS) ⁽²¹⁾ | GX channels | 600 | — | 12,500 | 600 | — | 12,500 | Mbps |
| Data rate | GT channels | 19,600 | — | 28,050 | 19,600 | — | 25,780 | Mbps |
| Absolute V _{MAX} for a receiver pin ⁽³⁾ | GT channels | — | — | 1.2 | — | — | 1.2 | V |
| Absolute V _{MIN} for a receiver pin | GT channels | -0.4 | — | — | -0.4 | — | — | V |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) before device configuration ⁽²⁰⁾ | GT channels | — | — | 1.6 | — | — | 1.6 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Maximum peak-to-peak differential input voltage V _{ID} (diff p-p) after device configuration ⁽¹⁶⁾ , ⁽²⁰⁾ | GT channels V _{CCR_GTB} = 1.05 V (V _{ICM} = 0.65 V) | — | — | 2.2 | — | — | 2.2 | V |
| | GX channels | ⁽⁸⁾ | | | | | | |
| Minimum differential eye opening at receiver serial input pins ⁽⁴⁾ , ⁽²⁰⁾ | GT channels | 200 | — | — | 200 | — | — | mV |
| | GX channels | ⁽⁸⁾ | | | | | | |

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---------------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedtodata$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedtodata$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedtoref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Table 29 shows the V_{OD} settings for the GT channel.

Table 29. Typical V_{OD} Setting for GT Channel, TX Termination = 100 Ω

| Symbol | V_{OD} Setting | V_{OD} Value (mV) |
|---|------------------|---------------------|
| V_{OD} differential peak to peak typical ⁽¹⁾ | 0 | 0 |
| | 1 | 200 |
| | 2 | 400 |
| | 3 | 600 |
| | 4 | 800 |
| | 5 | 1000 |

Note:

(1) Refer to Figure 4.

Table 31. PLL Specifications for Stratix V Devices (Part 2 of 3)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--|--|------|---------|--|-----------|
| t_{INCCJ} ^{(3), (4)} | Input clock cycle-to-cycle jitter ($f_{\text{REF}} \geq 100$ MHz) | — | — | 0.15 | UI (p-p) |
| | Input clock cycle-to-cycle jitter ($f_{\text{REF}} < 100$ MHz) | −750 | — | +750 | ps (p-p) |
| $t_{\text{OUTPJ_DC}}$ ⁽⁵⁾ | Period Jitter for dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 ⁽¹⁾ | ps (p-p) |
| | Period Jitter for dedicated clock output ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 ⁽¹⁾ | mUI (p-p) |
| $t_{\text{FOUTPJ_DC}}$ ⁽⁵⁾ | Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 250 ⁽¹¹⁾ , 175 ⁽¹²⁾ | ps (p-p) |
| | Period Jitter for dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾ | mUI (p-p) |
| $t_{\text{OUTCCJ_DC}}$ ⁽⁵⁾ | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Cycle-to-Cycle Jitter for a dedicated clock output ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| $t_{\text{FOUTCCJ_DC}}$ ⁽⁵⁾ | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 250 ⁽¹¹⁾ , 175 ⁽¹²⁾ | ps (p-p) |
| | Cycle-to-cycle Jitter for a dedicated clock output in fractional PLL ($f_{\text{OUT}} < 100$ MHz)+ | — | — | 25 ⁽¹¹⁾ , 17.5 ⁽¹²⁾ | mUI (p-p) |
| $t_{\text{OUTPJ_IO}}$ ^{(5), (8)} | Period Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{FOUTPJ_IO}}$ ^{(5), (8), (11)} | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 ⁽¹⁰⁾ | ps (p-p) |
| | Period Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 ⁽¹⁰⁾ | mUI (p-p) |
| $t_{\text{OUTCCJ_IO}}$ ^{(5), (8)} | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in integer PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 ⁽¹⁰⁾ | mUI (p-p) |
| $t_{\text{FOUTCCJ_IO}}$ ^{(5), (8), (11)} | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 600 ⁽¹⁰⁾ | ps (p-p) |
| | Cycle-to-cycle Jitter for a clock output on a regular I/O in fractional PLL ($f_{\text{OUT}} < 100$ MHz) | — | — | 60 | mUI (p-p) |
| $t_{\text{CASC_OUTPJ_DC}}$ ^{(5), (6)} | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} \geq 100$ MHz) | — | — | 175 | ps (p-p) |
| | Period Jitter for a dedicated clock output in cascaded PLLs ($f_{\text{OUT}} < 100$ MHz) | — | — | 17.5 | mUI (p-p) |
| f_{DRIFT} | Frequency drift after PFDENA is disabled for a duration of 100 μ s | — | — | ± 10 | % |
| dK_{BIT} | Bit number of Delta Sigma Modulator (DSM) | 8 | 24 | 32 | Bits |
| K_{VALUE} | Numerator of Fraction | 128 | 8388608 | 2147483648 | — |

Table 32. Block Performance Specifications for Stratix V DSP Devices (Part 2 of 2)

| Mode | Peformance | | | | | | | Unit |
|------------------------|------------|---------|---------|-----|---------------|-----|-----|------|
| | C1 | C2, C2L | I2, I2L | C3 | I3, I3L, I3YY | C4 | I4 | |
| Modes using Three DSPs | | | | | | | | |
| One complex 18 x 25 | 425 | 425 | 415 | 340 | 340 | 275 | 265 | MHz |
| Modes using Four DSPs | | | | | | | | |
| One complex 27 x 27 | 465 | 465 | 465 | 380 | 380 | 300 | 290 | MHz |

Memory Block Specifications

Table 33 lists the Stratix V memory block specifications.

Table 33. Memory Block Performance Specifications for Stratix V Devices ⁽¹⁾, ⁽²⁾ (Part 1 of 2)

| Memory | Mode | Resources Used | | Performance | | | | | | | Unit |
|--------|--|----------------|--------|-------------|---------|-----|-----|---------|---------------|-----|------|
| | | ALUTs | Memory | C1 | C2, C2L | C3 | C4 | I2, I2L | I3, I3L, I3YY | I4 | |
| MLAB | Single port, all supported widths | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x32/x64 depth | 0 | 1 | 450 | 450 | 400 | 315 | 450 | 400 | 315 | MHz |
| | Simple dual-port, x16 depth ⁽³⁾ | 0 | 1 | 675 | 675 | 533 | 400 | 675 | 533 | 400 | MHz |
| | ROM, all supported widths | 0 | 1 | 600 | 600 | 500 | 450 | 600 | 500 | 450 | MHz |

Table 36. High-Speed I/O Specifications for Stratix V Devices ⁽¹⁾, ⁽²⁾ (Part 2 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|--|---|-----|-----|------|------------------|-----|------|-------------------|-----|------|-------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Transmitter | | | | | | | | | | | | | | |
| True Differential I/O Standards - f _{HSDR} (data rate) | SERDES factor J = 3 to 10 ^{(9), (11), (12), (13), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1434 | (6) | — | 1250 | (6) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA ^{(12), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾ | SERDES factor J = 4 to 10 ⁽¹⁷⁾ | (6) | — | 1100 | (6) | — | 1100 | (6) | — | 840 | (6) | — | 840 | Mbps |
| t _{x Jitter} - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| t _{x Jitter} - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

Table 36. High-Speed I/O Specifications for Stratix V Devices ⁽¹⁾, ⁽²⁾ (Part 3 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4, I4 | | | Unit |
|--|---|----------------|-----|----------------|------------------|-----|----------------|-------------------|-----|----------------|----------------|-----|----------------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| t_{DUTY} | Transmitter output clock duty cycle for both True and Emulated Differential I/O Standards | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | 45 | 50 | 55 | % |
| t_{RISE} & t_{FALL} | True Differential I/O Standards | — | — | 160 | — | — | 160 | — | — | 200 | — | — | 200 | ps |
| | Emulated Differential I/O Standards with three external output resistor networks | — | — | 250 | — | — | 250 | — | — | 250 | — | — | 300 | ps |
| TCCS | True Differential I/O Standards | — | — | 150 | — | — | 150 | — | — | 150 | — | — | 150 | ps |
| | Emulated Differential I/O Standards | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |
| Receiver | | | | | | | | | | | | | | |
| True Differential I/O Standards - f_{HSDRDP} (data rate) | SERDES factor J = 3 to 10 ⁽¹¹⁾ , ⁽¹²⁾ , ⁽¹³⁾ , ⁽¹⁴⁾ , ⁽¹⁵⁾ , ⁽¹⁶⁾ | 150 | — | 1434 | 150 | — | 1434 | 150 | — | 1250 | 150 | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | LVDS RX with DPA ⁽¹²⁾ , ⁽¹⁴⁾ , ⁽¹⁵⁾ , ⁽¹⁶⁾ | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1600 | 150 | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | Mbps |
| | SERDES factor J = 1, uses SDR Register | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | ⁽⁶⁾ | — | ⁽⁷⁾ | Mbps |

Table 49. DCLK-to-DATA[] Ratio ⁽¹⁾ (Part 2 of 2)

| Configuration Scheme | Decompression | Design Security | DCLK-to-DATA[] Ratio |
|----------------------|---------------|-----------------|----------------------|
| FPP ×32 | Disabled | Disabled | 1 |
| | Disabled | Enabled | 4 |
| | Enabled | Disabled | 8 |
| | Enabled | Enabled | 8 |

Note to Table 49:

- (1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the DCLK-to-DATA[] ratio is 2, the DCLK frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.



If the DCLK-to-DATA[] ratio is greater than 1, at the end of configuration, you can only stop the DCLK (DCLK-to-DATA[] ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

Figure 11. Single Device FPP Configuration Using an External Host**Notes to Figure 11:**

- (1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with V_{CCPGM} .
- (2) You can leave the nCEO pin unconnected or use it as a user I/O pin when it does not feed another device's nCE pin.
- (3) The MSEL pin settings vary for different data width, configuration voltage standards, and POR delay. To connect MSEL, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.
- (4) If you use FPP ×8, use DATA [7..0]. If you use FPP ×16, use DATA [15..0].

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 2 of 2)

| Symbol | Parameter | Minimum | Maximum | Units |
|--------------|---|--|---------|-------|
| t_{CD2UM} | CONF_DONE high to user mode ⁽³⁾ | 175 | 437 | μs |
| t_{CD2CU} | CONF_DONE high to CLKUSR enabled | 4 × maximum DCLK period | — | — |
| t_{CD2UMC} | CONF_DONE high to user mode with CLKUSR option on | $t_{CD2CU} + (8576 \times \text{CLKUSR period})$ | — | — |

Notes to Table 53:

- (1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.
- (2) t_{CF2CD} , t_{CF2ST0} , t_{CFG} , t_{STATUS} , and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.
- (3) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices” chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform ⁽¹⁾**Notes to Figure 15:**

- (1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (2) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (3) After power-up, before and during configuration, CONF_DONE is low.
- (4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.
- (5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.
- (6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high after the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 58. IOE Programmable Delay for Stratix V Devices (Part 2 of 2)

| Parameter (1) | Available Settings | Min Offset (2) | Fast Model | | Slow Model | | | | | | | |
|------------------|-----------------------|----------------------|------------|------------|------------|-------|-------|-------|-------|-------------|-------|------|
| | | | Industrial | Commercial | C1 | C2 | C3 | C4 | I2 | I3, I3YY | I4 | Unit |
| D3 | 8 | 0 | 1.587 | 1.699 | 2.793 | 2.793 | 2.992 | 3.192 | 2.811 | 3.047 | 3.257 | ns |
| D4 | 64 | 0 | 0.464 | 0.492 | 0.838 | 0.838 | 0.924 | 1.011 | 0.843 | 0.920 | 1.006 | ns |
| D5 | 64 | 0 | 0.464 | 0.493 | 0.838 | 0.838 | 0.924 | 1.011 | 0.844 | 0.921 | 1.006 | ns |
| D6 | 32 | 0 | 0.229 | 0.244 | 0.415 | 0.415 | 0.458 | 0.503 | 0.418 | 0.456 | 0.499 | ns |

Notes to Table 58:

- (1) You can set this value in the Quartus II software by selecting **D1**, **D2**, **D3**, **D5**, and **D6** in the **Assignment Name** column of **Assignment Editor**.
- (2) Minimum offset does not include the intrinsic delay.

Programmable Output Buffer Delay

Table 59 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 59. Programmable Output Buffer Delay for Stratix V Devices (1)

| Symbol | Parameter | Typical | Unit |
|---------------------|----------------------------------|-------------|------|
| D _{OUTBUF} | Rising and/or falling edge delay | 0 (default) | ps |
| | | 25 | ps |
| | | 50 | ps |
| | | 75 | ps |

Note to Table 59:

- (1) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 60 lists the glossary for this chapter.

Table 60. Glossary (Part 1 of 4)

| Letter | Subject | Definitions |
|--------|----------------------|---|
| A | — | — |
| B | | |
| C | | |
| D | — | — |
| E | — | — |
| F | f _{HCLK} | Left and right PLL input clock frequency. |
| | f _{HSDR} | High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDR} = 1/TUI), non-DPA. |
| | f _{HSDRDPA} | High-speed I/O block—Maximum and minimum LVDS data transfer rate (f _{HSDRDPA} = 1/TUI), DPA. |

Table 61. Document Revision History (Part 2 of 3)

| Date | Version | Changes |
|---------------|---------|--|
| November 2014 | 3.3 | <ul style="list-style-type: none"> ■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. ■ Added the I3YY speed grade to the V_{CC} description in Table 6. ■ Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. ■ Added 240-Ω to Table 11. ■ Changed CDR PPM tolerance in Table 23. ■ Added additional max data rate for fPLL in Table 23. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. ■ Changed CDR PPM tolerance in Table 28. ■ Added additional max data rate for fPLL in Table 28. ■ Changed the mode descriptions for MLAB and M20K in Table 33. ■ Changed the Max value of f_{HCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. ■ Changed the frequency ranges for C1 and C2 in Table 39. ■ Changed the .rbf file sizes for 5SGSD6 and 5SGSD8 in Table 47. ■ Added note about nSTATUS to Table 50, Table 51, Table 54. ■ Changed the available settings in Table 58. ■ Changed the note in “Periphery Performance”. ■ Updated the “I/O Standard Specifications” section. ■ Updated the “Raw Binary File Size” section. ■ Updated the receiver voltage input range in Table 22. ■ Updated the max frequency for the LVDS clock network in Table 36. ■ Updated the DCLK note to Figure 11. ■ Updated Table 23 VO_{CM} (DC Coupled) condition. ■ Updated Table 6 and Table 7. ■ Added the DCLK specification to Table 55. ■ Updated the notes for Table 47. ■ Updated the list of parameters for Table 56. |
| November 2013 | 3.2 | ■ Updated Table 28 |
| November 2013 | 3.1 | ■ Updated Table 33 |
| November 2013 | 3.0 | ■ Updated Table 23 and Table 28 |
| October 2013 | 2.9 | ■ Updated the “Transceiver Characterization” section |
| October 2013 | 2.8 | <ul style="list-style-type: none"> ■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 ■ Added Figure 1 and Figure 3 ■ Added the “Transceiver Characterization” section ■ Removed all “Preliminary” designations. |