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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

| | |
|--------------------------------|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 225400 |
| Number of Logic Elements/Cells | 597000 |
| Total RAM Bits | 53248000 |
| Number of I/O | 600 |
| Number of Gates | - |
| Voltage - Supply | 0.82V ~ 0.88V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 1760-BBGA, FCBGA |
| Supplier Device Package | 1760-FCBGA (42.5x42.5) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/5sgxmb6r2f43c3n |

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

| Symbol | Description | Minimum | Maximum | Unit |
|-----------------------|--------------------------------|---------|---------|------|
| V _{CCD_FPLL} | PLL digital power supply | −0.5 | 1.8 | V |
| V _{CCA_FPLL} | PLL analog power supply | −0.5 | 3.4 | V |
| V _I | DC input voltage | −0.5 | 3.8 | V |
| T _J | Operating junction temperature | −55 | 125 | °C |
| T _{STG} | Storage temperature (No bias) | −65 | 150 | °C |
| I _{OUT} | DC output current per pin | −25 | 40 | mA |

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

| Symbol | Description | Devices | Minimum | Maximum | Unit |
|-----------------------|--|------------|---------|---------|------|
| V _{CCA_GXBL} | Transceiver channel PLL power supply (left side) | GX, GS, GT | −0.5 | 3.75 | V |
| V _{CCA_GXBR} | Transceiver channel PLL power supply (right side) | GX, GS | −0.5 | 3.75 | V |
| V _{CCA_GTBR} | Transceiver channel PLL power supply (right side) | GT | −0.5 | 3.75 | V |
| V _{CCHIP_L} | Transceiver hard IP power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCHIP_R} | Transceiver hard IP power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCHSSI_L} | Transceiver PCS power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCHSSI_R} | Transceiver PCS power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCR_GXBL} | Receiver analog power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCR_GXBR} | Receiver analog power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCR_GTBR} | Receiver analog power supply for GT channels (right side) | GT | −0.5 | 1.35 | V |
| V _{CCT_GXBL} | Transmitter analog power supply (left side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCT_GXBR} | Transmitter analog power supply (right side) | GX, GS, GT | −0.5 | 1.35 | V |
| V _{CCT_GTBR} | Transmitter analog power supply for GT channels (right side) | GT | −0.5 | 1.35 | V |
| V _{CCL_GTBR} | Transmitter clock network power supply (right side) | GT | −0.5 | 1.35 | V |
| V _{CCH_GXBL} | Transmitter output buffer power supply (left side) | GX, GS, GT | −0.5 | 1.8 | V |
| V _{CCH_GXBR} | Transmitter output buffer power supply (right side) | GX, GS, GT | −0.5 | 1.8 | V |

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to −2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 7. Recommended Transceiver Power Supply Operating Conditions for Stratix V GX, GS, and GT Devices (Part 2 of 2)

| Symbol | Description | Devices | Minimum ⁽⁴⁾ | Typical | Maximum ⁽⁴⁾ | Unit |
|------------------------|--|------------|------------------------|---------|------------------------|------|
| V_{CCR_GXBR} (2) | Receiver analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCR_GTBR} | Receiver analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCT_GXBL} (2) | Transmitter analog power supply (left side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GXBR} (2) | Transmitter analog power supply (right side) | GX, GS, GT | 0.82 | 0.85 | 0.88 | V |
| | | | 0.87 | 0.90 | 0.93 | |
| | | | 0.97 | 1.0 | 1.03 | |
| | | | 1.03 | 1.05 | 1.07 | |
| V_{CCT_GTBR} | Transmitter analog power supply for GT channels (right side) | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCL_GTBR} | Transmitter clock network power supply | GT | 1.02 | 1.05 | 1.08 | V |
| V_{CCH_GXBL} | Transmitter output buffer power supply (left side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |
| V_{CCH_GXBR} | Transmitter output buffer power supply (right side) | GX, GS, GT | 1.425 | 1.5 | 1.575 | V |

Notes to Table 7:

- (1) This supply must be connected to 3.0 V if the CMU PLL, receiver CDR, or both, are configured at a base data rate > 6.5 Gbps. Up to 6.5 Gbps, you can connect this supply to either 3.0 V or 2.5 V.
- (2) Refer to Table 8 to select the correct power supply level for your design.
- (3) When using ATX PLLs, the supply must be 3.0 V.
- (4) This value describes the budget for the DC (static) power supply tolerance and does not include the dynamic tolerance requirements. Refer to the PDN tool for the additional budget for the dynamic tolerance requirements.

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

| Conditions | Core Speed Grade | VCCR_GXB & VCCT_GXB ⁽²⁾ | VCCA_GXB | VCCH_GXB | Unit |
|---|-----------------------------------|------------------------------------|----------|----------|------|
| If BOTH of the following conditions are true: <ul style="list-style-type: none"> ■ Data rate > 10.3 Gbps. ■ DFE is used. | All | 1.05 | 3.0 | 1.5 | V |
| If ANY of the following conditions are true ⁽¹⁾ : <ul style="list-style-type: none"> ■ ATX PLL is used. ■ Data rate > 6.5Gbps. ■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used. | All | 1.0 | | | |
| If ALL of the following conditions are true: <ul style="list-style-type: none"> ■ ATX PLL is not used. ■ Data rate ≤ 6.5Gbps. ■ DFE, AEQ, and EyeQ are not used. | C1, C2, I2, and I3YY | 0.90 | 2.5 | | |
| | C2L, C3, C4, I2L, I3, I3L, and I4 | 0.85 | 2.5 | | |

Notes to Table 8:

- (1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.
- (2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.



For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices ⁽¹⁾ (Part 2 of 2)

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
|--|--|---|----------------------|------------|----------------|------------|------|
| | | | C1 | C2,I2 | C3,I3, I3YY | C4,I4 | |
| 50-Ω R _S | Internal series termination with calibration (50-Ω setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 34-Ω and 40-Ω R _S | Internal series termination with calibration (34-Ω and 40-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 48-Ω, 60-Ω, 80-Ω, and 240-Ω R _S | Internal series termination with calibration (48-Ω, 60-Ω, 80-Ω, and 240-Ω setting) | V _{CCIO} = 1.2 V | ±15 | ±15 | ±15 | ±15 | % |
| 50-Ω R _T | Internal parallel termination with calibration (50-Ω setting) | V _{CCIO} = 2.5, 1.8, 1.5, 1.2 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω R _T | Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting) | V _{CCIO} = 1.5, 1.35, 1.25 V | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 60-Ω and 120-Ω R _T | Internal parallel termination with calibration (60-Ω and 120-Ω setting) | V _{CCIO} = 1.2 | -10 to +40 | -10 to +40 | -10 to +40 | -10 to +40 | % |
| 25-Ω R _{S_left_shift} | Internal left shift series termination with calibration (25-Ω R _{S_left_shift} setting) | V _{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V | ±15 | ±15 | ±15 | ±15 | % |

Note to Table 11:

(1) OCT calibration accuracy is valid at the time of calibration only.

Table 12 lists the Stratix V OCT without calibration resistance tolerance to PVT changes.

Table 12. OCT Without Calibration Resistance Tolerance Specifications for Stratix V Devices (Part 1 of 2)

| Symbol | Description | Conditions | Resistance Tolerance | | | | Unit |
|-----------------------------|--|-----------------------------------|----------------------|-------|-----------------|--------|------|
| | | | C1 | C2,I2 | C3, I3, I3YY | C4, I4 | |
| 25-Ω R, 50-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 3.0 and 2.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.8 and 1.5 V | ±30 | ±30 | ±40 | ±40 | % |
| 25-Ω R _S | Internal series termination without calibration (25-Ω setting) | V _{CCIO} = 1.2 V | ±35 | ±35 | ±50 | ±50 | % |

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) ⁽¹⁾

| Symbol | Description | V _{CCIO} (V) | Typical | Unit |
|--------|--|-----------------------|---------|-------------------|
| dR/dT | OCT variation with temperature without recalibration | 3.0 | 0.189 | %/ ^o C |
| | | 2.5 | 0.208 | |
| | | 1.8 | 0.266 | |
| | | 1.5 | 0.273 | |
| | | 1.2 | 0.317 | |

Note to Table 13:

(1) Valid for a V_{CCIO} range of $\pm 5\%$ and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

| Symbol | Description | Value | Unit |
|--------------------|--|-------|------|
| C _{IOTB} | Input capacitance on the top and bottom I/O pins | 6 | pF |
| C _{IOLR} | Input capacitance on the left and right I/O pins | 6 | pF |
| C _{OUTFB} | Input capacitance on dual-purpose clock output and feedback pins | 6 | pF |

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Table 15. Hot Socketing Specifications for Stratix V Devices

| Symbol | Description | Maximum |
|---------------------------|--|---------------------|
| I _{IOPIN} (DC) | DC current per I/O pin | 300 μ A |
| I _{IOPIN} (AC) | AC current per I/O pin | 8 mA ⁽¹⁾ |
| I _{XCVR-TX} (DC) | DC current per transceiver transmitter pin | 100 mA |
| I _{XCVR-RX} (DC) | DC current per transceiver receiver pin | 50 mA |

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C \, dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

-  You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.
-  For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices ⁽¹⁾ (Part 4 of 7)

| Symbol/ Description | Conditions | Transceiver Speed Grade 1 | | | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|--|---|------------------------------|-----------|-----|------------------------------|-----------|-----|------------------------------|-----------|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Differential on-chip termination resistors ⁽²¹⁾ | 85-Ω setting | — | 85 ± 30% | — | — | 85 ± 30% | — | — | 85 ± 30% | — | Ω |
| | 100-Ω setting | — | 100 ± 30% | — | — | 100 ± 30% | — | — | 100 ± 30% | — | Ω |
| | 120-Ω setting | — | 120 ± 30% | — | — | 120 ± 30% | — | — | 120 ± 30% | — | Ω |
| | 150-Ω setting | — | 150 ± 30% | — | — | 150 ± 30% | — | — | 150 ± 30% | — | Ω |
| V _{ICM} (AC and DC coupled) | V _{CCR_GXB} = 0.85 V or 0.9 V full bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | V _{CCR_GXB} = 0.85 V or 0.9 V half bandwidth | — | 600 | — | — | 600 | — | — | 600 | — | mV |
| | V _{CCR_GXB} = 1.0 V/1.05 V full bandwidth | — | 700 | — | — | 700 | — | — | 700 | — | mV |
| | V _{CCR_GXB} = 1.0 V half bandwidth | — | 750 | — | — | 750 | — | — | 750 | — | mV |
| t _{LTR} ⁽¹¹⁾ | — | — | — | 10 | — | — | 10 | — | — | 10 | μs |
| t _{LTD} ⁽¹²⁾ | — | 4 | — | — | 4 | — | — | 4 | — | — | μs |
| t _{LTD_manual} ⁽¹³⁾ | — | 4 | — | — | 4 | — | — | 4 | — | — | μs |
| t _{LTR_LTD_manual} ⁽¹⁴⁾ | — | 15 | — | — | 15 | — | — | 15 | — | — | μs |
| Run Length | — | — | — | 200 | — | — | 200 | — | — | 200 | UI |
| Programmable equalization (AC Gain) ⁽¹⁰⁾ | Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz) | — | — | 16 | — | — | 16 | — | — | 16 | dB |

Table 24 shows the maximum transmitter data rate for the clock network.

Table 24. Clock Network Maximum Data Rate Transmitter Specifications ⁽¹⁾

| Clock Network | ATX PLL | | | CMU PLL ⁽²⁾ | | | fPLL | | |
|--------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|------------------------|--------------------|---------------------------------------|
| | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span | Non-bonded Mode (Gbps) | Bonded Mode (Gbps) | Channel Span |
| x1 ⁽³⁾ | 14.1 | — | 6 | 12.5 | — | 6 | 3.125 | — | 3 |
| x6 ⁽³⁾ | — | 14.1 | 6 | — | 12.5 | 6 | — | 3.125 | 6 |
| x6 PLL Feedback ⁽⁴⁾ | — | 14.1 | Side-wide | — | 12.5 | Side-wide | — | — | — |
| xN (PCIe) | — | 8.0 | 8 | — | 5.0 | 8 | — | — | — |
| xN (Native PHY IP) | 8.0 | 8.0 | Up to 13 channels above and below PLL | 7.99 | 7.99 | Up to 13 channels above and below PLL | 3.125 | 3.125 | Up to 13 channels above and below PLL |
| | — | 8.01 to 9.8304 | Up to 7 channels above and below PLL | | | | | | |

Notes to Table 24:

- (1) Valid data rates below the maximum specified in this table depend on the reference clock frequency and the PLL counter settings. Check the MegaWizard message during the PHY IP instantiation.
- (2) ATX PLL is recommended at 8 Gbps and above data rates for improved jitter performance.
- (3) Channel span is within a transceiver bank.
- (4) Side-wide channel bonding is allowed up to the maximum supported by the PHY IP.

Table 25 shows the approximate maximum data rate using the standard PCS.

Table 25. Stratix V Standard PCS Approximate Maximum Date Rate ⁽¹⁾, ⁽³⁾

| Mode ⁽²⁾ | Transceiver Speed Grade | PMA Width | 20 | 20 | 16 | 16 | 10 | 10 | 8 | 8 |
|---------------------|-------------------------|---------------------------------------|---------|---------|---------|---------|-----|-----|------|------|
| | | PCS/Core Width | 40 | 20 | 32 | 16 | 20 | 10 | 16 | 8 |
| FIFO | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 8.5 | 8.5 | 8.5 | 8.5 | 6.5 | 5.8 | 5.2 | 4.72 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.84 | 7.2 | 5.3 | 4.7 | 4.24 | 3.76 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.8 | 4.2 | 3.84 | 3.44 |
| Register | 1 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | 2 | C1, C2, C2L, I2, I2L core speed grade | 12.2 | 11.4 | 9.76 | 9.12 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | C3, I3, I3L core speed grade | 9.8 | 9.0 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | 3 | C1, C2, C2L, I2, I2L core speed grade | 10.3125 | 10.3125 | 10.3125 | 10.3125 | 6.1 | 5.7 | 4.88 | 4.56 |
| | | I3YY core speed grade | 10.3125 | 10.3125 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C3, I3, I3L core speed grade | 8.5 | 8.5 | 7.92 | 7.2 | 4.9 | 4.5 | 3.96 | 3.6 |
| | | C4, I4 core speed grade | 8.5 | 8.2 | 7.04 | 6.56 | 4.4 | 4.1 | 3.52 | 3.28 |

Notes to Table 25:

- (1) The maximum data rate is in Gbps.
- (2) The Phase Compensation FIFO can be configured in FIFO mode or register mode. In the FIFO mode, the pointers are not fixed, and the latency can vary. In the register mode the pointers are fixed for low latency.
- (3) The maximum data rate is also constrained by the transceiver speed grade. Refer to Table 1 for the transceiver speed grade.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) ⁽¹⁾

| Symbol/ Description | Conditions | Transceiver Speed Grade 2 | | | Transceiver Speed Grade 3 | | | Unit |
|---------------------------------|------------|------------------------------|-----|-----|------------------------------|-----|-----|------|
| | | Min | Typ | Max | Min | Typ | Max | |
| t_{pll_lock} ⁽¹⁴⁾ | — | — | — | 10 | — | — | 10 | μs |

Notes to Table 28:

- (1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.
- (2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.
- (3) The device cannot tolerate prolonged operation at this absolute maximum.
- (4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.
- (5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.
- (6) Refer to Figure 6 for the GT channel DC gain curves.
- (7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.
- (9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.
- (10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high.
- (11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the $rx_is_lockedto\ data$ signal goes high when the CDR is functioning in the manual mode.
- (12) $t_{LTR_LTD_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the $rx_is_lockedto\ ref$ signal goes high when the CDR is functioning in the manual mode.
- (13) $tp11_powerdown$ is the PLL powerdown minimum pulse width.
- (14) $tp11_lock$ is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.
- (15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula:
REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.
- (16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to $4 \times (\text{absolute } V_{MAX} \text{ for receiver pin} - V_{ICM})$.
- (17) For ES devices, RREF is 2000 Ω ±1%.
- (18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).
- (19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.
- (20) Refer to Figure 4.
- (21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.
- (22) This supply follows VCCR_GXB for both GX and GT channels.
- (23) When you use fPLL as a TXPLL of the transceiver.

Table 29 shows the V_{OD} settings for the GT channel.

Table 29. Typical V_{OD} Setting for GT Channel, TX Termination = 100 Ω

| Symbol | V_{OD} Setting | V_{OD} Value (mV) |
|---|------------------|---------------------|
| V_{OD} differential peak to peak typical ⁽¹⁾ | 0 | 0 |
| | 1 | 200 |
| | 2 | 400 |
| | 3 | 600 |
| | 4 | 800 |
| | 5 | 1000 |

Note:

(1) Refer to Figure 4.

PLL Specifications

Table 31 lists the Stratix V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

Table 31. PLL Specifications for Stratix V Devices (Part 1 of 3)

| Symbol | Parameter | Min | Typ | Max | Unit |
|--------------------------|--|-----|-----|--------------------|------|
| f_{IN} | Input clock frequency (C1, C2, C2L, I2, and I2L speed grades) | 5 | — | 800 ⁽¹⁾ | MHz |
| | Input clock frequency (C3, I3, I3L, and I3YY speed grades) | 5 | — | 800 ⁽¹⁾ | MHz |
| | Input clock frequency (C4, I4 speed grades) | 5 | — | 650 ⁽¹⁾ | MHz |
| f_{INPFD} | Input frequency to the PFD | 5 | — | 325 | MHz |
| f_{FINPFD} | Fractional Input clock frequency to the PFD | 50 | — | 160 | MHz |
| f_{VCO} ⁽⁹⁾ | PLL VCO operating range (C1, C2, C2L, I2, I2L speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C3, I3, I3L, I3YY speed grades) | 600 | — | 1600 | MHz |
| | PLL VCO operating range (C4, I4 speed grades) | 600 | — | 1300 | MHz |
| $t_{EINDUTY}$ | Input clock or external feedback clock input duty cycle | 40 | — | 60 | % |
| f_{OUT} | Output frequency for an internal global or regional clock (C1, C2, C2L, I2, I2L speed grades) | — | — | 717 ⁽²⁾ | MHz |
| | Output frequency for an internal global or regional clock (C3, I3, I3L speed grades) | — | — | 650 ⁽²⁾ | MHz |
| | Output frequency for an internal global or regional clock (C4, I4 speed grades) | — | — | 580 ⁽²⁾ | MHz |
| f_{OUT_EXT} | Output frequency for an external clock output (C1, C2, C2L, I2, I2L speed grades) | — | — | 800 ⁽²⁾ | MHz |
| | Output frequency for an external clock output (C3, I3, I3L speed grades) | — | — | 667 ⁽²⁾ | MHz |
| | Output frequency for an external clock output (C4, I4 speed grades) | — | — | 553 ⁽²⁾ | MHz |
| $t_{OUTDUTY}$ | Duty cycle for a dedicated external clock output (when set to 50%) | 45 | 50 | 55 | % |
| t_{FCOMP} | External feedback clock compensation time | — | — | 10 | ns |
| $f_{DYCONFIGCLK}$ | Dynamic Configuration Clock used for <code>mgmt_clk</code> and <code>scanclk</code> | — | — | 100 | MHz |
| t_{LOCK} | Time required to lock from the end-of-device configuration or deassertion of <code>areset</code> | — | — | 1 | ms |
| t_{DLOCK} | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) | — | — | 1 | ms |
| f_{CLBW} | PLL closed-loop low bandwidth | — | 0.3 | — | MHz |
| | PLL closed-loop medium bandwidth | — | 1.5 | — | MHz |
| | PLL closed-loop high bandwidth ⁽⁷⁾ | — | 4 | — | MHz |
| t_{PLL_PSERR} | Accuracy of PLL phase shift | — | — | ±50 | ps |
| t_{ARESET} | Minimum pulse width on the <code>areset</code> signal | 10 | — | — | ns |

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 2 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4,I4 | | | Unit |
|--|---|-----|-----|------|------------------|-----|------|-------------------|-----|------|-------|-----|------|------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Transmitter | | | | | | | | | | | | | | |
| True Differential I/O Standards - f _{HSDR} (data rate) | SERDES factor J = 3 to 10 ^{(9), (11), (12), (13), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1434 | (6) | — | 1250 | (6) | — | 1050 | Mbps |
| | SERDES factor J ≥ 4 LVDS TX with DPA ^{(12), (14), (15), (16)} | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1600 | (6) | — | 1250 | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| Emulated Differential I/O Standards with Three External Output Resistor Networks - f _{HSDR} (data rate) ⁽¹⁰⁾ | SERDES factor J = 4 to 10 ⁽¹⁷⁾ | (6) | — | 1100 | (6) | — | 1100 | (6) | — | 840 | (6) | — | 840 | Mbps |
| t _{x Jitter} - True Differential I/O Standards | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 160 | — | — | 160 | — | — | 160 | — | — | 160 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | — | — | 0.1 | UI |
| t _{x Jitter} - Emulated Differential I/O Standards with Three External Output Resistor Network | Total Jitter for Data Rate 600 Mbps - 1.25 Gbps | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 325 | ps |
| | Total Jitter for Data Rate < 600 Mbps | — | — | 0.2 | — | — | 0.2 | — | — | 0.2 | — | — | 0.25 | UI |

Table 36. High-Speed I/O Specifications for Stratix V Devices ^{(1), (2)} (Part 4 of 4)

| Symbol | Conditions | C1 | | | C2, C2L, I2, I2L | | | C3, I3, I3L, I3YY | | | C4, I4 | | | Unit |
|-------------------------------|---|-----|-----|-----------|------------------|-----|-----------|-------------------|-----|-----------|--------|-----|-----------|----------|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| f _{HSDR} (data rate) | SERDES factor J = 3 to 10 | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | (6) | — | (8) | Mbps |
| | SERDES factor J = 2, uses DDR Registers | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| | SERDES factor J = 1, uses SDR Register | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | (6) | — | (7) | Mbps |
| DPA Mode | | | | | | | | | | | | | | |
| DPA run length | — | — | — | 1000 0 | — | — | 1000 0 | — | — | 1000 0 | — | — | 1000 0 | UI |
| Soft CDR mode | | | | | | | | | | | | | | |
| Soft-CDR PPM tolerance | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ± PPM |
| Non DPA Mode | | | | | | | | | | | | | | |
| Sampling Window | — | — | — | 300 | — | — | 300 | — | — | 300 | — | — | 300 | ps |

Notes to Table 36:

- (1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.
- (2) When J = 1 or 2, bypass the SERDES block.
- (3) This only applies to DPA and soft-CDR modes.
- (4) Clock Boost Factor (W) is the ratio between the input data rate to the input clock rate.
- (5) This is achieved by using the **LVDS** clock network.
- (6) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
- (7) The maximum ideal frequency is the SERDES factor (J) x the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity simulation is clean.
- (8) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.
- (9) If the receiver with DPA enabled and transmitter are using shared PLLs, the minimum data rate is 150 Mbps.
- (10) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine leftover timing margin.
- (11) The F_{MAX} specification is based on the fast clock used for serial data. The interface F_{MAX} is also dependent on the parallel clock domain which is design-dependent and requires timing analysis.
- (12) Stratix V RX LVDS will need DPA. For Stratix V TX LVDS, the receiver side component must have DPA.
- (13) Stratix V LVDS serialization and de-serialization factor needs to be x4 and above.
- (14) Requires package skew compensation with PCB trace length.
- (15) Do not mix single-ended I/O buffer within LVDS I/O bank.
- (16) Chip-to-chip communication only with a maximum load of 5 pF.
- (17) When using True LVDS RX channels for emulated LVDS TX channel, only serialization factors 1 and 2 are supported.

Figure 7 shows the dynamic phase alignment (DPA) lock time specifications with the DPA PLL calibration option enabled.

Figure 7. DPA Lock Time Specification with DPA PLL Calibration Enabled



Table 37 lists the DPA lock time specifications for Stratix V devices.

Table 37. DPA Lock Time Specifications for Stratix V GX Devices Only ^{(1), (2), (3)}

| Standard | Training Pattern | Number of Data Transitions in One Repetition of the Training Pattern | Number of Repetitions per 256 Data Transitions ⁽⁴⁾ | Maximum |
|--------------------|----------------------|--|---|----------------------|
| SPI-4 | 00000000001111111111 | 2 | 128 | 640 data transitions |
| Parallel Rapid I/O | 00001111 | 2 | 128 | 640 data transitions |
| | 10010000 | 4 | 64 | 640 data transitions |
| Miscellaneous | 10101010 | 8 | 32 | 640 data transitions |
| | 01010101 | 8 | 32 | 640 data transitions |

Notes to Table 37:

- (1) The DPA lock time is for one channel.
- (2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
- (3) The DPA lock time stated in this table applies to both commercial and industrial grade.
- (4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 8 shows the LVDS soft-clock data recovery (CDR)/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps. Table 38 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate ≥ 1.25 Gbps.

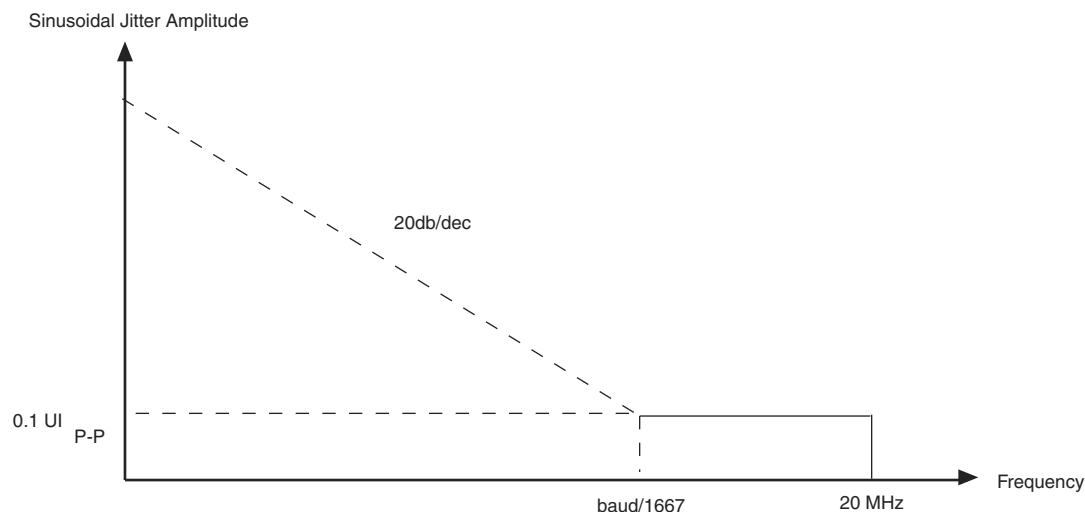
Figure 8. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate ≥ 1.25 Gbps



Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

| Jitter Frequency (Hz) | | Sinusoidal Jitter (UI) |
|-----------------------|------------|------------------------|
| F1 | 10,000 | 25.000 |
| F2 | 17,565 | 25.000 |
| F3 | 1,493,000 | 0.350 |
| F4 | 50,000,000 | 0.350 |

Figure 9 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps

DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices ⁽¹⁾

| C1 | C2, C2L, I2, I2L | C3, I3, I3L, I3YY | C4,I4 | Unit |
|---------|------------------|-------------------|---------|------|
| 300-933 | 300-933 | 300-890 | 300-890 | MHz |

Note to Table 39:

- (1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices ^{(1), (2)} (Part 1 of 2)

| Speed Grade | Min | Max | Unit |
|------------------|-----|-----|------|
| C1 | 8 | 14 | ps |
| C2, C2L, I2, I2L | 8 | 14 | ps |
| C3,I3, I3L, I3YY | 8 | 15 | ps |

FPP Configuration Timing when DCLK-to-DATA [] = 1

Figure 12 shows the timing waveform for FPP configuration when using a MAX II or MAX V device as an external host. This waveform shows timing when the DCLK-to-DATA [] ratio is 1.

Figure 12. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is 1 ^{(1), (2)}



Notes to Figure 12:

- (1) Use this timing waveform when the DCLK-to-DATA [] ratio is 1.
- (2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.
- (3) After power-up, the Stratix V device holds nSTATUS low for the time of the POR delay.
- (4) After power-up, before and during configuration, CONF_DONE is low.
- (5) Do not leave DCLK floating after configuration. DCLK is ignored after configuration is complete. It can toggle high or low if required.
- (6) For FPP $\times 16$, use DATA [15..0]. For FPP $\times 8$, use DATA [7..0]. DATA [31..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.
- (7) To ensure a successful configuration, send the entire configuration data to the Stratix V device. CONF_DONE is released high when the Stratix V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.
- (8) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme ^{(1), (2)}

| Minimum | Typical | Maximum | Unit |
|---------|---------|---------|------|
| 5.3 | 7.9 | 12.5 | MHz |
| 10.6 | 15.7 | 25.0 | MHz |
| 21.3 | 31.4 | 50.0 | MHz |
| 42.6 | 62.9 | 100.0 | MHz |

Notes to Table 52:

- (1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.
- (2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing



Notes to Figure 14:

- (1) If you are using AS ×4 mode, this signal represents the AS_DATA [3 : 0] and EPCQ sends in 4-bits of data for each DCLK cycle.
- (2) The initialization clock can be from internal oscillator or CLKUSR pin.
- (3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices ^{(1), (2)} (Part 1 of 2)

| Symbol | Parameter | Minimum | Maximum | Units |
|----------|---|---------|---------|-------|
| t_{CO} | DCLK falling edge to AS_DATA0/ASDO output | — | 2 | ns |
| t_{SU} | Data setup time before falling edge on DCLK | 1.5 | — | ns |
| t_H | Data hold time after falling edge on DCLK | 0 | — | ns |

Table 60. Glossary (Part 3 of 4)

| Letter | Subject | Definitions |
|--------|--|--|
| S | SW (sampling window) | <p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position within the sampling window, as shown:</p>  |
| | Single-ended voltage referenced I/O standard | <p>The JEDEC standard for SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing:</p> <p><i>Single-Ended Voltage Referenced I/O Standard</i></p>  |
| T | t_c | High-speed receiver and transmitter input and output clock period. |
| | TCCS (channel-to-channel-skew) | The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the <i>Timing Diagram</i> figure under SW in this table). |
| | t_{DUTY} | <p>High-speed I/O block—Duty cycle on the high-speed transmitter output clock.</p> <p>Timing Unit Interval (TUI)</p> <p>The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{receiver input clock frequency multiplication factor}) = t_c/w$)</p> |
| | t_{FALL} | Signal high-to-low transition time (80-20%) |
| | t_{INCCJ} | Cycle-to-cycle jitter tolerance on the PLL clock input. |
| | t_{OUTPJ_IO} | Period jitter on the general purpose I/O driven by a PLL. |
| | t_{OUTPJ_DC} | Period jitter on the dedicated clock output driven by a PLL. |
| | t_{RISE} | Signal low-to-high transition time (20-80%) |
| U | — | — |

