Intel - 5SGXMB6R3F40C2N Datasheet

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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	225400
Number of Logic Elements/Cells	597000
Total RAM Bits	53248000
Number of I/O	432
Number of Gates	-
Voltage - Supply	0.87V ~ 0.93V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	1517-FBGA (40x40)
Supplier Device Package	1517-FBGA (40x40)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxmb6r3f40c2n

Table 3. Absolute Maximum Ratings for Stratix V Devices (Part 2 of 2)

Symbol	Description	Minimum	Maximum	Unit
V_{CCD_FPLL}	PLL digital power supply	–0.5	1.8	V
V_{CCA_FPLL}	PLL analog power supply	–0.5	3.4	V
V_I	DC input voltage	–0.5	3.8	V
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C
I_{OUT}	DC output current per pin	–25	40	mA

Table 4 lists the absolute conditions for the transceiver power supply for Stratix V GX, GS, and GT devices.

Table 4. Transceiver Power Supply Absolute Conditions for Stratix V GX, GS, and GT Devices

Symbol	Description	Devices	Minimum	Maximum	Unit
V_{CCA_GXBL}	Transceiver channel PLL power supply (left side)	GX, GS, GT	–0.5	3.75	V
V_{CCA_GXBR}	Transceiver channel PLL power supply (right side)	GX, GS	–0.5	3.75	V
V_{CCA_GTBR}	Transceiver channel PLL power supply (right side)	GT	–0.5	3.75	V
V_{CCHIP_L}	Transceiver hard IP power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCHIP_R}	Transceiver hard IP power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCHSSI_L}	Transceiver PCS power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCHSSI_R}	Transceiver PCS power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GXBL}	Receiver analog power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GXBR}	Receiver analog power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCR_GTBR}	Receiver analog power supply for GT channels (right side)	GT	–0.5	1.35	V
V_{CCT_GXBL}	Transmitter analog power supply (left side)	GX, GS, GT	–0.5	1.35	V
V_{CCT_GXBR}	Transmitter analog power supply (right side)	GX, GS, GT	–0.5	1.35	V
V_{CCT_GTBR}	Transmitter analog power supply for GT channels (right side)	GT	–0.5	1.35	V
V_{CCL_GTBR}	Transmitter clock network power supply (right side)	GT	–0.5	1.35	V
V_{CCH_GXBL}	Transmitter output buffer power supply (left side)	GX, GS, GT	–0.5	1.8	V
V_{CCH_GXBR}	Transmitter output buffer power supply (right side)	GX, GS, GT	–0.5	1.8	V

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage shown in Table 5 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Recommended Operating Conditions

This section lists the functional operating limits for the AC and DC parameters for Stratix V devices. Table 6 lists the steady-state voltage and current values expected from Stratix V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 6. Recommended Operating Conditions for Stratix V Devices (Part 1 of 2)

Symbol	Description	Condition	Min (4)	Typ	Max (4)	Unit
V_{CC}	Core voltage and periphery circuitry power supply (C1, C2, I2, and I3YY speed grades)	—	0.87	0.9	0.93	V
	Core voltage and periphery circuitry power supply (C2L, C3, C4, I2L, I3, I3L, and I4 speed grades) (3)	—	0.82	0.85	0.88	V
V_{CCPT}	Power supply for programmable power technology	—	1.45	1.50	1.55	V
V_{CC_AUX}	Auxiliary supply for the programmable power technology	—	2.375	2.5	2.625	V
V_{CCPD} (1)	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V
V_{CCIO}	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.45	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.45	1.5	1.55	V
V_{CCBAT} (2)	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C

Table 13. OCT Variation after Power-Up Calibration for Stratix V Devices (Part 2 of 2) (1)

Symbol	Description	V_{CCIO} (V)	Typical	Unit
dR/dT	OCT variation with temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 13:

(1) Valid for a V_{CCIO} range of ±5% and a temperature range of 0° to 85°C.

Pin Capacitance

Table 14 lists the Stratix V device family pin capacitance.

Table 14. Pin Capacitance for Stratix V Devices

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on the top and bottom I/O pins	6	pF
C_{IOLR}	Input capacitance on the left and right I/O pins	6	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output and feedback pins	6	pF

Hot Socketing

Table 15 lists the hot socketing specifications for Stratix V devices.

Table 15. Hot Socketing Specifications for Stratix V Devices

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 μA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver pin	50 mA

Note to Table 15:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}|$ = C dv/dt, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Table 19. Single-Ended SSTL, HSTL, and HSUL I/O Standards Signal Specifications for Stratix V Devices (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
HSTL-18 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25* V_{CCIO}	0.75* V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1* V_{CCIO}	0.9* V_{CCIO}	—	—

Table 20. Differential SSTL I/O Standards for Stratix V Devices

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.62	V_{CCIO} + 0.6
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	*(1)*	V_{CCIO}/2 – 0.15	—	V_{CCIO}/2 + 0.15	0.35	—
SSTL-135 Class I, II	1.283	1.35	1.45	0.2	*(1)*	V_{CCIO}/2 – 0.15	V_{CCIO}/2	V_{CCIO}/2 + 0.15	2($V_{IH(AC)}$ - V_{REF})	2($V_{IL(AC)}$ - V_{REF})
SSTL-125 Class I, II	1.19	1.25	1.31	0.18	*(1)*	V_{CCIO}/2 – 0.15	V_{CCIO}/2	V_{CCIO}/2 + 0.15	2($V_{IH(AC)}$ - V_{REF})	—
SSTL-12 Class I, II	1.14	1.2	1.26	0.18	—	V_{REF} –0.15	V_{CCIO}/2	V_{REF} + 0.15	–0.30	0.30

Note to Table 20:

(1) The maximum value for $V_{SWING(DC)}$ is not defined. However, each single-ended signal needs to be within the respective single-ended limits ($V_{IH(DC)}$ and $V_{IL(DC)}$).

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—

Table 21. Differential HSTL and HSUL I/O Standards for Stratix V Devices (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5* V_{CCIO}	—	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5*V_{CCIO} – 0.12	0.5* V_{CCIO}	0.5*V_{CCIO} + 0.12	0.4* V_{CCIO}	0.5* V_{CCIO}	0.6* V_{CCIO}	0.44	0.44

Table 22. Differential I/O Standard Specifications for Stratix V Devices *(7)*

I/O Standard	V_{CCIO} (V) *(10)*			V_{ID} (mV) *(8)*			$V_{ICM(DC)}$ (V)			V_{OD} (V) *(6)*			V_{OCM} (V) *(6)*		
	Min	Typ	Max	Min	Condition	Max	Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
PCML	Transmitter, receiver, and input reference clock pins of the high-speed transceivers use the PCML I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 23 on page 18.														
2.5 V LVDS *(1)*	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	$D_{MAX} \leq$ 700 Mbps	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	$D_{MAX} >$ 700 Mbps	1.55	0.247	—	0.6	1.125	1.25	1.375
BLVDS *(5)*	2.375	2.5	2.625	100	—	—	—	—	—	—	—	—	—	—	—
RSDS (HIO) *(2)*	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	—	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO) *(3)*	2.375	2.5	2.625	200	—	600	0.4	—	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL *(4), (9)*	—	—	—	300	—	—	0.6	$D_{MAX} \leq$ 700 Mbps	1.8	—	—	—	—	—	—
	—	—	—	300	—	—	1	$D_{MAX} >$ 700 Mbps	1.6	—	—	—	—	—	—

Notes to Table 22*:*

(1) For optimized LVDS receiver performance, the receiver voltage input range must be between 1.0 V to 1.6 V for data rates above 700 Mbps, and 0 V to 1.85 V for data rates below 700 Mbps.

(2) For optimized RSDS receiver performance, the receiver voltage input range must be between 0.25 V to 1.45 V.

(3) For optimized Mini-LVDS receiver performance, the receiver voltage input range must be between 0.3 V to 1.425 V.

(4) For optimized LVPECL receiver performance, the receiver voltage input range must be between 0.85 V to 1.75 V for data rate above 700 Mbps and 0.45 V to 1.95 V for data rate below 700 Mbps.

(5) There are no fixed V_{ICM}, V_{OD}, and V_{OCM} specifications for BLVDS. They depend on the system topology.

(6) RL range: $90 \leq RL \leq 110\ \Omega$.

(7) The 1.4-V and 1.5-V PCML transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 18.

(8) The minimum VID value is applicable over the entire common mode range, VCM.

(9) LVPECL is only supported on dedicated clock input pins.

(10) Differential inputs are powered by VCCPD which requires 2.5 V.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator and the Quartus® II PowerPlay Power Analyzer feature.

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices (1) (Part 1 of 7)

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) (8)	—	40	—	710	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) (8)	—	100	—	710	100	—	710	100	—	710	MHz
Rise time	Measure at ±60 mV of differential signal (26)	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal (26)	—	—	400	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices *(1)* **(Part 4 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors *(21)*	85–Ω setting	—	85 ± 30%	—	—	85 ± 30%	—	—	85 ± 30%	—	Ω
	100–Ω setting	—	100 ± 30%	—	—	100 ± 30%	—	—	100 ± 30%	—	Ω
	120–Ω setting	—	120 ± 30%	—	—	120 ± 30%	—	—	120 ± 30%	—	Ω
	150-Ω setting	—	150 ± 30%	—	—	150 ± 30%	—	—	150 ± 30%	—	Ω
V_{ICM} (AC and DC coupled)	V_{CCR_GXB} = 0.85 V or 0.9 V full bandwidth	—	600	—	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 0.85 V or 0.9 V half bandwidth	—	600	—	—	600	—	—	600	—	mV
	V_{CCR_GXB} = 1.0 V/1.05 V full bandwidth	—	700	—	—	700	—	—	700	—	mV
	V_{CCR_GXB} = 1.0 V half bandwidth	—	750	—	—	750	—	—	750	—	mV
t_{LTR} *(11)*	—	—	—	10	—	—	10	—	—	10	µs
t_{LTD} *(12)*	—	4	—	—	4	—	—	4	—	—	µs
t_{LTD_manual} *(13)*	—	4	—	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ *(14)*	—	15	—	—	15	—	—	15	—	—	µs
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization (AC Gain) *(10)*	Full bandwidth (6.25 GHz) Half bandwidth (3.125 GHz)	—	—	16	—	—	16	—	—	16	dB

Table 23. Transceiver Specifications for Stratix V GX and GS Devices *(1)* **(Part 7 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} *(16)*	—	—	—	10	—	—	10	—	—	10	µs

Notes to Table 23:

(1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

(4) This supply follows VCCR_GXB.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(8) The input reference clock frequency options depend on the data rate and the device speed grade.

(9) The line data rate may be limited by PCS-FPGA interface speed grade.

(10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(14) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(15) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(19) For ES devices, R_{REF} is 2000 Ω ±1%.

(20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(22) Refer to Figure 2.

(23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(24) I3YY devices can achieve data rates up to 10.3125 Gbps.

(25) When you use fPLL as a TXPLL of the transceiver.

(26) `REFCLK` performance requires to meet transmitter `REFCLK` phase noise specification.

(27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 2 of 5) (1)

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Transmitter REFCLK Phase Noise (622 MHz) (18)	100 Hz	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	
	10 kHz	—	—	-100	—	—	-100	
	100 kHz	—	—	-110	—	—	-110	
	≥ 1 MHz	—	—	-120	—	—	-120	
Transmitter REFCLK Phase Jitter (100 MHz) (15)	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	ps (rms)
RREF (17)	—	—	1800 ± 1%	—	—	1800 ± 1%	—	Ω
Transceiver Clocks								
`fixedclk` clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	MHz
Reconfiguration clock (`mgmt_clk_clk`) frequency	—	100	—	125	100	—	125	MHz
Receiver								
Supported I/O Standards	—	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS						
Data rate (Standard PCS) (21)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS) (21)	GX channels	600	—	12,500	600	—	12,500	Mbps
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Absolute V_{MAX} for a receiver pin (3)	GT channels	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	GT channels	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration (20)	GT channels	—	—	1.6	—	—	1.6	V
	GX channels	(8)						
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration (16), (20)	GT channels V_{CCR_GTB} = 1.05 V (V_{ICM} = 0.65 V)	—	—	2.2	—	—	2.2	V
	GX channels	(8)						
Minimum differential eye opening at receiver serial input pins (4), (20)	GT channels	200	—	—	200	—	—	mV
	GX channels	(8)						

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) *(1)*

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	**Typ**	**Max**	**Min**	**Typ**	**Max**	
Differential on-chip termination resistors *(7)*	GT channels	—	100	—	—	100	—	Ω
Differential on-chip termination resistors for GX channels *(19)*	85-Ω setting	—	85 ± 30%	—	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	—	100 ± 30%	—	Ω
	120-Ω setting	—	120 ± 30%	—	—	120 ± 30%	—	Ω
	150-Ω setting	—	150 ± 30%	—	—	150 ± 30%	—	Ω
V_{ICM} (AC coupled)	GT channels	—	650	—	—	650	—	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 0.85 V or 0.9 V	—	600	—	—	600	—	mV
	VCCR_GXB = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	VCCR_GXB = 1.0 V half bandwidth	—	750	—	—	750	—	mV
t_{LTR} *(9)*	—	—	—	10	—	—	10	µs
t_{LTD} *(10)*	—	4	—	—	4	—	—	µs
t_{LTD_manual} *(11)*	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ *(12)*	—	15	—	—	15	—	—	µs
Run Length	GT channels	—	—	72	—	—	72	CID
	GX channels	*(8)*						
CDR PPM	GT channels	—	—	1000	—	—	1000	± PPM
	GX channels	*(8)*						
Programmable equalization (AC Gain) *(5)*	GT channels	—	—	14	—	—	14	dB
	GX channels	*(8)*						
Programmable DC gain *(6)*	GT channels	—	—	7.5	—	—	7.5	dB
	GX channels	*(8)*						
Differential on-chip termination resistors *(7)*	GT channels	—	100	—	—	100	—	Ω
Transmitter								
Supported I/O Standards	—	1.4-V and 1.5-V PCML						
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps

Table 33. Memory Block Performance Specifications for Stratix V Devices (1), (2) (Part 2 of 2)

Memory	Mode	Resources Used		Performance							Unit
		ALUTs	Memory	C1	C2, C2L	C3	C4	I2, I2L	I3, I3L, I3YY	I4	
M20K Block	Single-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	525	525	455	400	525	455	400	MHz
	Simple dual-port with ECC enabled, 512 × 32	0	1	450	450	400	350	450	400	350	MHz
	Simple dual-port with ECC and optional pipeline registers enabled, 512 × 32	0	1	600	600	500	450	600	500	450	MHz
	True dual port, all supported widths	0	1	700	700	650	550	700	500	450	MHz
	ROM, all supported widths	0	1	700	700	650	550	700	500	450	MHz

Notes to Table 33:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in F_{MAX}.

(3) The F_{MAX} specification is only achievable with Fitter options, **MLAB Implementation In 16-Bit Deep Mode** enabled.

Temperature Sensing Diode Specifications

Table 34 lists the internal TSD specification.

Table 34. Internal Temperature Sensing Diode Specification

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimum Resolution with no Missing Codes
–40°C to 100°C	±8°C	No	1 MHz, 500 KHz	< 100 ms	8 bits	8 bits

Table 35 lists the specifications for the Stratix V external temperature sensing diode.

Table 35. External Temperature Sensing Diode Specifications for Stratix V Devices

Description	Min	Typ	Max	Unit
I_{bias}, diode source current	8	—	200	μA
$V_{bias,}$ voltage across diode	0.3	—	0.9	V
Series resistance	—	—	< 1	Ω
Diode ideality factor	1.006	1.008	1.010	—

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

☞ The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices *(1), (2)* **(Part 1 of 4)**

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 *(4)*	5	—	800	5	—	800	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards *(3)*	Clock boost factor W = 1 to 40 *(4)*	5	—	800	5	—	800	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 *(4)*	5	—	520	5	—	520	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	800	5	—	800	5	—	625 *(5)*	5	—	525 *(5)*	MHz

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices (1), (2) (Part 2 of 2)

Speed Grade	Min	Max	Unit
C4,I4	8	16	ps

Notes to Table 40:

(1) The typical value equals the average of the minimum and maximum values.

(2) The delay settings are linear with a cumulative delay variation of 40 ps for all speed grades. For example, when using a –2 speed grade and applying a 10-phase offset setting to a 90° phase shift at 400 MHz, the expected average cumulative delay is [625 ps + (10 × 10 ps) ± 20 ps] = 725 ps ± 20 ps.

Table 41 lists the DQS phase shift error for Stratix V devices.

Table 41. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Stratix V Devices (1)

Number of DQS Delay Buffers	C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
1	28	28	30	32	ps
2	56	56	60	64	ps
3	84	84	90	96	ps
4	112	112	120	128	ps

Notes to Table 41:

(1) This error specification is the absolute maximum and minimum error. For example, skew on three DQS delay buffers in a –2 speed grade is ±78 ps or ±39 ps.

Table 42 lists the memory output clock jitter specifications for Stratix V devices.

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices (1), (Part 1 of 2) (2), (3)

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Regional	Clock period jitter	$t_{JIT(per)}$	–50	50	–50	50	–55	55	–55	55	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–100	100	–100	100	–110	110	–110	110	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–50	50	–50	50	–82.5	82.5	–82.5	82.5	ps
Global	Clock period jitter	$t_{JIT(per)}$	–75	75	–75	75	–82.5	82.5	–82.5	82.5	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	–150	150	–150	150	–165	165	–165	165	ps
	Duty cycle jitter	$t_{JIT(duty)}$	–75	75	–75	75	–90	90	–90	90	ps

Duty Cycle Distortion (DCD) Specifications

Table 44 lists the worst-case DCD for Stratix V devices.

Table 44. Worst-Case DCD on Stratix V I/O Pins (1)

Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4,I4		Unit
	Min	Max	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	45	55	%

Note to Table 44:

(1) The DCD numbers do not cover the core clock network.

Configuration Specification

POR Delay Specification

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the `nSTATUS` is released high and your device is ready to begin configuration.

For more information about the POR delay, refer to the *Hot Socketing and Power-On Reset in Stratix V Devices* chapter.

Table 45 lists the fast and standard POR delay specification.

Table 45. Fast and Standard POR Delay Specification (1)

POR Delay	Minimum	Maximum
Fast	4 ms	12 ms
Standard	100 ms	300 ms

Note to Table 45:

(1) You can select the POR delay based on the `MSEL` settings as described in the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

JTAG Configuration Specifications

Table 46 lists the JTAG timing parameters and values for Stratix V devices.

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period (2)	30	—	ns
t_{JCP}	TCK clock period (2)	167	—	ns
t_{JCH}	TCK clock high time (2)	14	—	ns
t_{JCL}	TCK clock low time (2)	14	—	ns
$t_{JPSU (TDI)}$	TDI JTAG port setup time	2	—	ns
$t_{JPSU (TMS)}$	TMS JTAG port setup time	3	—	ns

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the “POR Delay Specification” section of the “Configuration, Design Security, and Remote System Upgrades in Stratix V Devices”.

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) (4), (5)
Stratix V GX	5SGXA3	H35, F40, F35 (2)	213,798,880	562,392
		H29, F35 (3)	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Table 48. Minimum Configuration Time Estimation for Stratix V Devices

Variant	Member Code	Active Serial (1)			Fast Passive Parallel (2)		
		Width	DCLK (MHz)	Min Config Time (s)	Width	DCLK (MHz)	Min Config Time (s)
GS	D3	4	100	0.344	32	100	0.043
	D4	4	100	0.534	32	100	0.067
		4	100	0.344	32	100	0.043
	D5	4	100	0.534	32	100	0.067
	D6	4	100	0.741	32	100	0.093
	D8	4	100	0.741	32	100	0.093
E	E9	4	100	0.857	32	100	0.107
	EB	4	100	0.857	32	100	0.107

Notes to Table 48:

(1) DCLK frequency of 100 MHz using external CLKUSR.

(2) Max FPGA FPP bandwidth may exceed bandwidth available from some external storage or control logic.

Fast Passive Parallel Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Stratix V devices.

DCLK-to-DATA[] Ratio for FPP Configuration

FPP configuration requires a different `DCLK`-to-`DATA[]` ratio when you enable the design security, decompression, or both features. Table 49 lists the `DCLK`-to-`DATA[]` ratio for each combination.

Table 49. DCLK-to-DATA[] Ratio (1) (Part 1 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×8	Disabled	Disabled	1
	Disabled	Enabled	1
	Enabled	Disabled	2
	Enabled	Enabled	2
FPP ×16	Disabled	Disabled	1
	Disabled	Enabled	2
	Enabled	Disabled	4
	Enabled	Enabled	4

Table 49. DCLK-to-DATA[] Ratio (1) (Part 2 of 2)

Configuration Scheme	Decompression	Design Security	DCLK-to-DATA[] Ratio
FPP ×32	Disabled	Disabled	1
	Disabled	Enabled	4
	Enabled	Disabled	8
	Enabled	Enabled	8

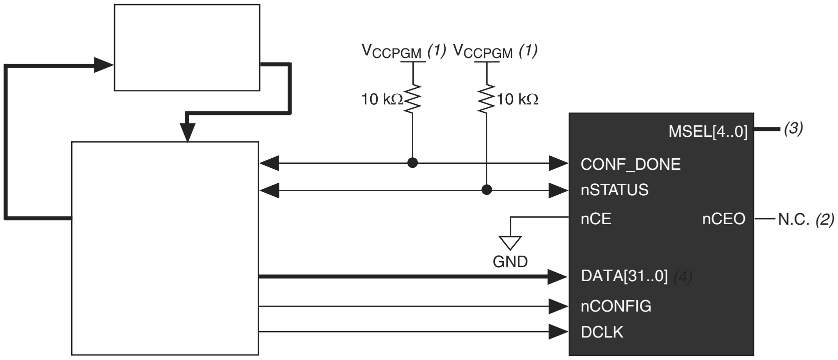
Note to Table 49:

(1) Depending on the `DCLK`-to-`DATA[]` ratio, the host must send a `DCLK` frequency that is r times the data rate in bytes per second (Bps), or words per second (Wps). For example, in FPP ×16 when the `DCLK`-to-`DATA[]` ratio is 2, the `DCLK` frequency must be 2 times the data rate in Wps. Stratix V devices use the additional clock cycles to decrypt and decompress the configuration data.

☞ If the `DCLK`-to-`DATA[]` ratio is greater than 1, at the end of configuration, you can only stop the `DCLK` (`DCLK`-to-`DATA[]` ratio – 1) clock cycles after the last data is latched into the Stratix V device.

Figure 11 shows the configuration interface connections between the Stratix V device and a MAX II or MAX V device for single device configuration.

Figure 11. Single Device FPP Configuration Using an External Host



Notes to Figure 11:

(1) Connect the resistor to a supply that provides an acceptable input signal for the Stratix V device. V_{CCPGM} must be high enough to meet the V_{IH} specification of the I/O on the device and the external host. Altera recommends powering up all configuration system I/Os with V_{CCPGM}.

(2) You can leave the `nCEO` pin unconnected or use it as a user I/O pin when it does not feed another device's `nCE` pin.

(3) The `MSEL` pin settings vary for different data width, configuration voltage standards, and POR delay. To connect `MSEL`, refer to the MSEL Pin Settings section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

(4) If you use FPP ×8, use `DATA[7..0]`. If you use FPP ×16, use `DATA[15..0]`.

Active Serial Configuration Timing

Table 52 lists the `DCLK` frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme (1), (2)

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

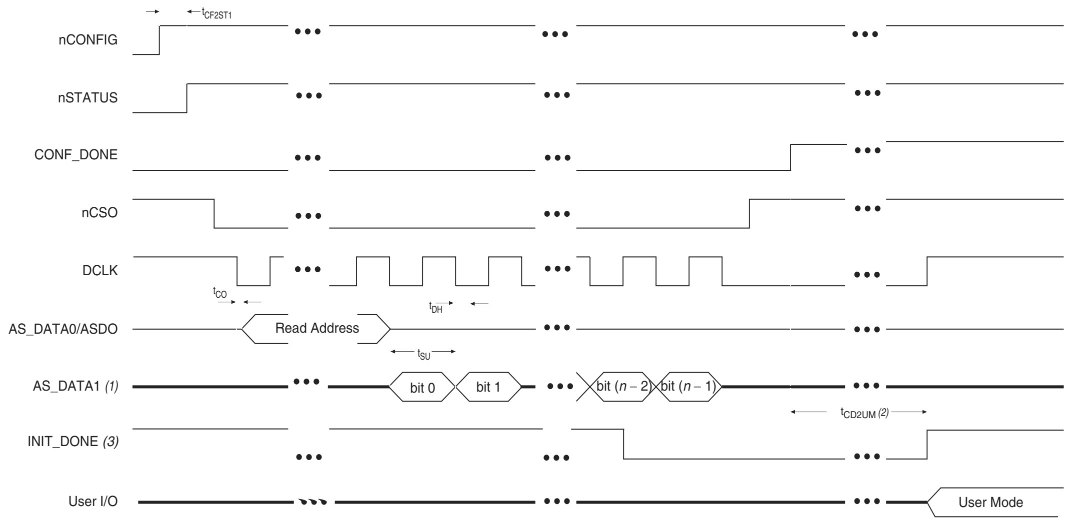
Notes to Table 52:

(1) This applies to the `DCLK` frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support `DCLK` frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing



Notes to Figure 14:

(1) If you are using AS ×4 mode, this signal represents the `AS_DATA[3..0]` and EPCQ sends in 4-bits of data for each `DCLK` cycle.

(2) The initialization clock can be from internal oscillator or `CLKUSR` pin.

(3) After the option bit to enable the `INIT_DONE` pin is configured into the device, the `INIT_DONE` goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices (1), (2) (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Units
t_{CO}	`DCLK` falling edge to `AS_DATA0/ASDO` output	—	2	ns
t_{SU}	Data setup time before falling edge on `DCLK`	1.5	—	ns
t_{H}	Data hold time after falling edge on `DCLK`	0	—	ns

Table 60. Glossary (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC common mode input voltage.
	V_{ICM}	Input common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—clock boost factor
X Y Z	—	—

Table 61. Document Revision History (Part 2 of 3)

Date	Version	Changes
November 2014	3.3	■ Added the I3YY speed grade and changed the data rates for the GX channel in Table 1. ■ Added the I3YY speed grade to the V_{CC} description in Table 6. ■ Added the I3YY speed grade to V_{CCHIP_L}, V_{CCHIP_R}, V_{CCHSSI_L}, and V_{CCHSSI_R} descriptions in Table 7. ■ Added 240-Ω to Table 11. ■ Changed CDR PPM tolerance in Table 23. ■ Added additional max data rate for fPLL in Table 23. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 25. ■ Added the I3YY speed grade and changed the data rates for transceiver speed grade 3 in Table 26. ■ Changed CDR PPM tolerance in Table 28. ■ Added additional max data rate for fPLL in Table 28. ■ Changed the mode descriptions for MLAB and M20K in Table 33. ■ Changed the Max value of f_{HSCLK_OUT} for the C2, C2L, I2, I2L speed grades in Table 36. ■ Changed the frequency ranges for C1 and C2 in Table 39. ■ Changed the **.rbf** file sizes for 5SGSD6 and 5SGSD8 in Table 47. ■ Added note about `nSTATUS` to Table 50, Table 51, Table 54. ■ Changed the available settings in Table 58. ■ Changed the note in “Periphery Performance”. ■ Updated the “I/O Standard Specifications” section. ■ Updated the “Raw Binary File Size” section. ■ Updated the receiver voltage input range in Table 22. ■ Updated the max frequency for the LVDS clock network in Table 36. ■ Updated the `DCLK` note to Figure 11. ■ Updated Table 23 VO_{CM} (DC Coupled) condition. ■ Updated Table 6 and Table 7. ■ Added the `DCLK` specification to Table 55. ■ Updated the notes for Table 47. ■ Updated the list of parameters for Table 56.
November 2013	3.2	■ Updated Table 28
November 2013	3.1	■ Updated Table 33
November 2013	3.0	■ Updated Table 23 and Table 28
October 2013	2.9	■ Updated the “Transceiver Characterization” section
October 2013	2.8	■ Updated Table 3, Table 12, Table 14, Table 19, Table 20, Table 23, Table 24, Table 28, Table 30, Table 31, Table 32, Table 33, Table 36, Table 39, Table 40, Table 41, Table 42, Table 47, Table 53, Table 58, and Table 59 ■ Added Figure 1 and Figure 3 ■ Added the “Transceiver Characterization” section ■ Removed all “Preliminary” designations.