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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Obsolete
Number of LABs/CLBs	317000
Number of Logic Elements/Cells	840000
Total RAM Bits	53248000
Number of I/O	600
Number of Gates	-
Voltage - Supply	0.82V ~ 0.88V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	1760-BBGA, FCBGA
Supplier Device Package	1760-HBGA (45x45)
Purchase URL	https://www.e-xfl.com/product-detail/intel/5sgxmb9r2h43i3ln

Table 8 shows the transceiver power supply voltage requirements for various conditions.

Table 8. Transceiver Power Supply Voltage Requirements

Conditions	Core Speed Grade	VCCR_GXB & VCCT_GXB [2]	VCCA_GXB	VCCH_GXB	Unit
If BOTH of the following conditions are true: ■ Data rate > 10.3 Gbps. ■ DFE is used.	All	1.05	3.0	1.5	V
If ANY of the following conditions are true [1]: ■ ATX PLL is used. ■ Data rate > 6.5Gbps. ■ DFE (data rate ≤ 10.3 Gbps), AEQ, or EyeQ feature is used.	All	1.0			
If ALL of the following conditions are true: ■ ATX PLL is not used. ■ Data rate ≤ 6.5Gbps. ■ DFE, AEQ, and EyeQ are not used.	C1, C2, I2, and I3YY	0.90	2.5		
	C2L, C3, C4, I2L, I3, I3L, and I4	0.85	2.5		

Notes to Table 8:

(1) Choose this power supply voltage requirement option if you plan to upgrade your design later with any of the listed conditions.

(2) If the VCCR_GXB and VCCT_GXB supplies are set to 1.0 V or 1.05 V, they cannot be shared with the VCC core supply. If the VCCR_GXB and VCCT_GXB are set to either 0.90 V or 0.85 V, they can be shared with the VCC core supply.

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Supply current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to get supply current estimates for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 9 lists the Stratix V I/O pin leakage current specifications.

Table 9. I/O Pin Leakage Current for Stratix V Devices [1]

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	−30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	−30	—	30	µA

Note to Table 9:

(1) If V_O = V_{CCIO} to $V_{CCIOMax}$, 100 µA of leakage current per I/O is expected.

Bus Hold Specifications

Table 10 lists the Stratix V device family bus hold specifications.

Table 10. Bus Hold Parameters for Stratix V Devices

| Parameter | Symbol | Conditions | V_{CCIO} | | | | | | | | | | Unit |
| | | | 1.2 V | | 1.5 V | | 1.8 V | | 2.5 V | | 3.0 V | | |
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	I_{SUSL}	V_{IN} > V_{IL} (maximum)	22.5	—	25.0	—	30.0	—	50.0	—	70.0	—	µA
High sustaining current	I_{SUSH}	V_{IN} < V_{IH} (minimum)	−22.5	—	−25.0	—	−30.0	—	−50.0	—	−70.0	—	µA
Low overdrive current	I_{ODL}	0V < V_{IN} < V_{CCIO}	—	120	—	160	—	200	—	300	—	500	µA
High overdrive current	I_{ODH}	0V < V_{IN} < V_{CCIO}	—	−120	—	−160	—	−200	—	−300	—	−500	µA
Bus-hold trip point	V_{TRIP}	—	0.45	0.95	0.50	1.00	0.68	1.07	0.70	1.70	0.80	2.00	V

On-Chip Termination (OCT) Specifications

If you enable OCT calibration, calibration is automatically performed at power-up for I/Os connected to the calibration block. Table 11 lists the Stratix V OCT termination calibration accuracy specifications.

Table 11. OCT Calibration Accuracy Specifications for Stratix V Devices [1] **(Part 1 of 2)**

| Symbol | Description | Conditions | Calibration Accuracy | | | | Unit |
			C1	C2,I2	C3,I3, I3YY	C4,I4	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2 V	±15	±15	±15	±15	%

☞ You typically use the interactive Excel-based Early Power Estimator before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of the Stratix V core and periphery blocks.

These characteristics can be designated as Preliminary or Final.

■ Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."

■ Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 23 lists the Stratix V GX and GS transceiver specifications.

Table 23. Transceiver Specifications for Stratix V GX and GS Devices [1] **(Part 1 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	Dedicated reference clock pin	1.2-V PCML, 1.4-V PCML, 1.5-V PCML, 2.5-V PCML, Differential LVPECL, LVDS, and HCSL									
	RX reference clock pin	1.4-V PCML, 1.5-V PCML, 2.5-V PCML, LVPECL, and LVDS									
Input Reference Clock Frequency (CMU PLL) [8]	—	40	—	710	40	—	710	40	—	710	MHz
Input Reference Clock Frequency (ATX PLL) [8]	—	100	—	710	100	—	710	100	—	710	MHz
Rise time	Measure at ±60 mV of differential signal [26]	—	—	400	—	—	400	—	—	400	ps
Fall time	Measure at ±60 mV of differential signal [26]	—	—	400	—	—	400	—	—	400	
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices [1] **(Part 2 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Spread-spectrum downspread	PCIe	—	0 to −0.5	—	—	0 to −0.5	—	—	0 to −0.5	—	%
On-chip termination resistors [21]	—	—	100	—	—	100	—	—	100	—	Ω
Absolute V_{MAX} [5]	Dedicated reference clock pin	—	—	1.6	—	—	1.6	—	—	1.6	V
	RX reference clock pin	—	—	1.2	—	—	1.2	—	—	1.2	
Absolute V_{MIN}	—	−0.4	—	—	−0.4	—	—	−0.4	—	—	V
Peak-to-peak differential input voltage	—	200	—	1600	200	—	1600	200	—	1600	mV
V_{ICM} (AC coupled) [3]	Dedicated reference clock pin	1050/1000/900/850 [2]			1050/1000/900/850 [2]			1050/1000/900/850 [2]			mV
	RX reference clock pin	1.0/0.9/0.85 [4]			1.0/0.9/0.85 [4]			1.0/0.9/0.85 [4]			V
V_{ICM} (DC coupled)	HCSL I/O standard for PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
Transmitter REFCLK Phase Noise (622 MHz) [20]	100 Hz	—	—	-70	—	—	-70	—	—	-70	dBc/Hz
	1 kHz	—	—	-90	—	—	-90	—	—	-90	dBc/Hz
	10 kHz	—	—	-100	—	—	-100	—	—	-100	dBc/Hz
	100 kHz	—	—	-110	—	—	-110	—	—	-110	dBc/Hz
	≥1 MHz	—	—	-120	—	—	-120	—	—	-120	dBc/Hz
Transmitter REFCLK Phase Jitter (100 MHz) [17]	10 kHz to 1.5 MHz (PCIe)	—	—	3	—	—	3	—	—	3	ps (rms)
R_{REF} [19]	—	—	1800 ±1%	—	—	1800 ±1%	—	—	1800 ±1%	—	Ω
Transceiver Clocks											
`fixedclk` clock frequency	PCIe Receiver Detect	—	100 or 125	—	—	100 or 125	—	—	100 or 125	—	MHz

Table 23. Transceiver Specifications for Stratix V GX and GS Devices [1] **(Part 6 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Inter-transceiver block transmitter channel-to-channel skew	xN PMA bonded mode	—	—	500	—	—	500	—	—	500	ps
CMU PLL											
Supported Data Range	—	600	—	12500	600	—	12500	600	—	8500/ 10312.5 [24]	Mbps
$t_{pll\_powerdown}$ [15]	—	1	—	—	1	—	—	1	—	—	µs
t_{pll_lock} [16]	—	—	—	10	—	—	10	—	—	10	µs
ATX PLL											
Supported Data Rate Range	VCO post-divider L=2	8000	—	14100	8000	—	12500	8000	—	8500/ 10312.5 [24]	Mbps
	L=4	4000	—	7050	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3525	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	1000	—	1762.5	Mbps
$t_{pll\_powerdown}$ [15]	—	1	—	—	1	—	—	1	—	—	µs
t_{pll_lock} [16]	—	—	—	10	—	—	10	—	—	10	µs
fPLL											
Supported Data Range	—	600	—	3250/ 3125 [25]	600	—	3250/ 3125 [25]	600	—	3250/ 3125 [25]	Mbps
$t_{pll\_powerdown}$ [15]	—	1	—	—	1	—	—	1	—	—	µs

Table 23. Transceiver Specifications for Stratix V GX and GS Devices [(1)] **(Part 7 of 7)**

Symbol/ Description	Conditions	Transceiver Speed Grade 1			Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} [(16)]	—	—	—	10	—	—	10	—	—	10	µs

Notes to Table 23:

(1) Speed grades shown in Table 23 refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(3) This supply must be connected to 1.0 V if the transceiver is configured at a data rate > 6.5 Gbps, and to 1.05 V if configured at a data rate > 10.3 Gbps when DFE is used. For data rates up to 6.5 Gbps, you can connect this supply to 0.85 V.

(4) This supply follows VCCR_GXB.

(5) The device cannot tolerate prolonged operation at this absolute maximum.

(6) The differential eye opening specification at the receiver input pins assumes that **Receiver Equalization** is disabled. If you enable **Receiver Equalization**, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

(8) The input reference clock frequency options depend on the data rate and the device speed grade.

(9) The line data rate may be limited by PCS-FPGA interface speed grade.

(10) Refer to Figure 1 for the GX channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(11) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(12) t_{LTD} is time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high.

(13) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the rx_is_lockedtodata signal goes high when the CDR is functioning in the manual mode.

(14) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the rx_is_lockedtoref signal goes high when the CDR is functioning in the manual mode.

(15) $t_{pll\_powerdown}$ is the PLL powerdown minimum pulse width.

(16) t_{pll_lock} is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(17) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(18) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(19) For ES devices, R_{REF} is 2000 Ω ±1%.

(20) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(21) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(22) Refer to Figure 2.

(23) For oversampling designs to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(24) I3YY devices can achieve data rates up to 10.3125 Gbps.

(25) When you use fPLL as a TXPLL of the transceiver.

(26) REFCLK performance requires to meet transmitter REFCLK phase noise specification.

(27) Minimum eye opening of 85 mV is only for the unstressed input eye condition.

Figure 2 shows the differential transmitter output waveform.

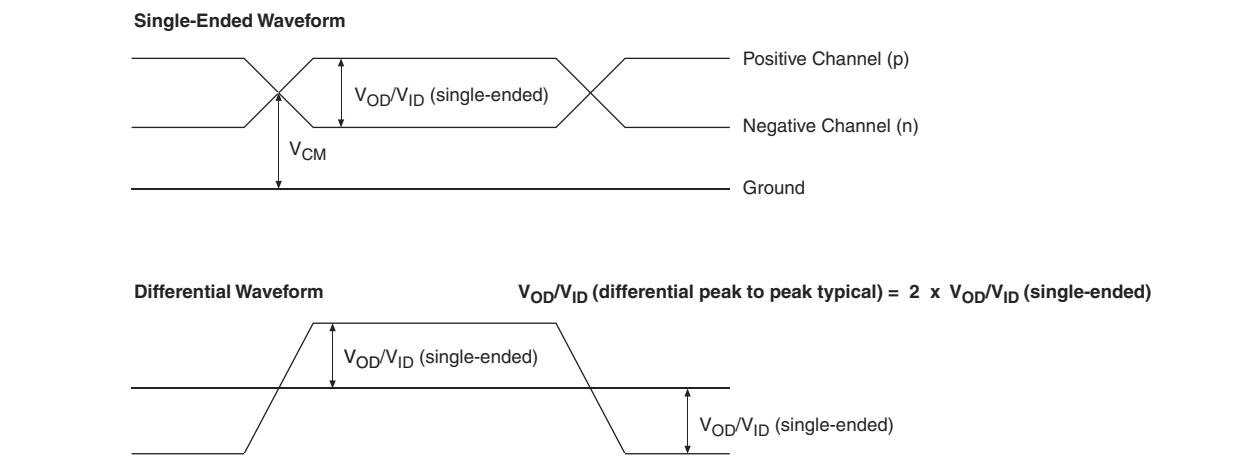**Figure 2. Differential Transmitter Output Waveform**

Single-Ended Waveform

Positive Channel (p)

V_{OD}/V_{ID} (single-ended)

Negative Channel (n)

V_{CM}

Ground

Differential Waveform   **V_{OD}/V_{ID} (differential peak to peak typical) = 2 x V_{OD}/V_{ID} (single-ended)**

V_{OD}/V_{ID} (single-ended)

V_{OD}/V_{ID} (single-ended)

Figure 3 shows the Stratix V AC gain curves for GX channels.

Figure 3. AC Gain Curves for GX Channels (full bandwidth)

☞ Stratix V GT devices contain both GX and GT channels. All transceiver specifications for the GX channels not listed in Table 28 are the same as those listed in Table 23.

Table 28 lists the Stratix V GT transceiver specifications.

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 3 of 5) [1]

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Differential on-chip termination resistors [7]	GT channels	—	100	—	—	100	—	Ω
Differential on-chip termination resistors for GX channels [19]	85-Ω setting	—	85 ± 30%	—	—	85 ± 30%	—	Ω
	100-Ω setting	—	100 ± 30%	—	—	100 ± 30%	—	Ω
	120-Ω setting	—	120 ± 30%	—	—	120 ± 30%	—	Ω
	150-Ω setting	—	150 ± 30%	—	—	150 ± 30%	—	Ω
V_{ICM} (AC coupled)	GT channels	—	650	—	—	650	—	mV
VICM (AC and DC coupled) for GX Channels	VCCR_GXB = 0.85 V or 0.9 V	—	600	—	—	600	—	mV
	VCCR_GXB = 1.0 V full bandwidth	—	700	—	—	700	—	mV
	VCCR_GXB = 1.0 V half bandwidth	—	750	—	—	750	—	mV
t_{LTR} [9]	—	—	—	10	—	—	10	µs
t_{LTD} [10]	—	4	—	—	4	—	—	µs
t_{LTD_manual} [11]	—	4	—	—	4	—	—	µs
$t_{LTR\_LTD\_manual}$ [12]	—	15	—	—	15	—	—	µs
Run Length	GT channels	—	—	72	—	—	72	CID
	GX channels				[8]			
CDR PPM	GT channels	—	—	1000	—	—	1000	± PPM
	GX channels				[8]			
Programmable equalization (AC Gain) [5]	GT channels	—	—	14	—	—	14	dB
	GX channels				[8]			
Programmable DC gain [6]	GT channels	—	—	7.5	—	—	7.5	dB
	GX channels				[8]			
Differential on-chip termination resistors [7]	GT channels	—	100	—	—	100	—	Ω
Transmitter								
Supported I/O Standards	—			1.4-V and 1.5-V PCML				
Data rate (Standard PCS)	GX channels	600	—	8500	600	—	8500	Mbps
Data rate (10G PCS)	GX channels	600	—	12,500	600	—	12,500	Mbps

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 4 of 5) [1]

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
Data rate	GT channels	19,600	—	28,050	19,600	—	25,780	Mbps
Differential on-chip termination resistors	GT channels	—	100	—	—	100	—	Ω
	GX channels				[8]			
V$_{OCM}$ (AC coupled)	GT channels	—	500	—	—	500	—	mV
	GX channels				[8]			
Rise/Fall time	GT channels	—	15	—	—	15	—	ps
	GX channels				[8]			
Intra-differential pair skew	GX channels				[8]			
Intra-transceiver block transmitter channel-to-channel skew	GX channels				[8]			
Inter-transceiver block transmitter channel-to-channel skew	GX channels				[8]			
CMU PLL								
Supported Data Range	—	600	—	12500	600	—	8500	Mbps
t$_{pll\_powerdown}$ [13]	—	1	—	—	1	—	—	µs
t$_{pll\_lock}$ [14]	—	—	—	10	—	—	10	µs
ATX PLL								
Supported Data Rate Range for GX Channels	VCO post-divider L=2	8000	—	12500	8000	—	8500	Mbps
	L=4	4000	—	6600	4000	—	6600	Mbps
	L=8	2000	—	3300	2000	—	3300	Mbps
	L=8, Local/Central Clock Divider =2	1000	—	1762.5	1000	—	1762.5	Mbps
Supported Data Rate Range for GT Channels	VCO post-divider L=2	9800	—	14025	9800	—	12890	Mbps
t$_{pll\_powerdown}$ [13]	—	1	—	—	1	—	—	µs
t$_{pll\_lock}$ [14]	—	—	—	10	—	—	10	µs
fPLL								
Supported Data Range	—	600	—	3250/ 3.125 [23]	600	—	3250/ 3.125 [23]	Mbps
t$_{pll\_powerdown}$ [13]	—	1	—	—	1	—	—	µs

Table 28. Transceiver Specifications for Stratix V GT Devices (Part 5 of 5) [1]

Symbol/ Description	Conditions	Transceiver Speed Grade 2			Transceiver Speed Grade 3			Unit
		Min	Typ	Max	Min	Typ	Max	
t_{pll_lock} [14]	—	—	—	10	—	—	10	μs

Notes to Table 28:

(1) Speed grades shown refer to the PMA Speed Grade in the device ordering code. The maximum data rate could be restricted by the Core/PCS speed grade. Contact your Altera Sales Representative for the maximum data rate specifications in each speed grade combination offered. For more information about device ordering codes, refer to the *Stratix V Device Overview*.

(2) The reference clock common mode voltage is equal to the VCCR_GXB power supply level.

(3) The device cannot tolerate prolonged operation at this absolute maximum.

(4) The differential eye opening specification at the receiver input pins assumes that receiver equalization is disabled. If you enable receiver equalization, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(5) Refer to Figure 5 for the GT channel AC gain curves. The total effective AC gain is the AC gain minus the DC gain.

(6) Refer to Figure 6 for the GT channel DC gain curves.

(7) CFP2 optical modules require the host interface to have the receiver data pins differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(8) Specifications for this parameter are the same as for Stratix V GX and GS devices. See Table 23 for specifications.

(9) t_{LTR} is the time required for the receive CDR to lock to the input reference clock frequency after coming out of reset.

(10) t_{LTD} is time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high.

(11) t_{LTD_manual} is the time required for the receiver CDR to start recovering valid data after the `rx_is_lockedtodata` signal goes high when the CDR is functioning in the manual mode.

(12) $t_{LTR\_LTD\_manual}$ is the time the receiver CDR must be kept in lock to reference (LTR) mode after the `rx_is_lockedtoref` signal goes high when the CDR is functioning in the manual mode.

(13) `tpll_powerdown` is the PLL powerdown minimum pulse width.

(14) `tpll_lock` is the time required for the transmitter CMU/ATX PLL to lock to the input reference clock frequency after coming out of reset.

(15) To calculate the REFCLK rms phase jitter requirement for PCIe at reference clock frequencies other than 100 MHz, use the following formula: REFCLK rms phase jitter at f(MHz) = REFCLK rms phase jitter at 100 MHz × 100/f.

(16) The maximum peak to peak differential input voltage V_{ID} after device configuration is equal to 4 × (absolute V_{MAX} for receiver pin - V_{ICM}).

(17) For ES devices, RREF is 2000 Ω ±1%.

(18) To calculate the REFCLK phase noise requirement at frequencies other than 622 MHz, use the following formula: REFCLK phase noise at f(MHz) = REFCLK phase noise at 622 MHz + 20*log(f/622).

(19) SFP/+ optical modules require the host interface to have RD+/- differentially terminated with 100 Ω. The internal OCT feature is available after the Stratix V FPGA configuration is completed. Altera recommends that FPGA configuration is completed before inserting the optical module. Otherwise, minimize unnecessary removal and insertion with unconfigured devices.

(20) Refer to Figure 4.

(21) For oversampling design to support data rates less than the minimum specification, the CDR needs to be in LTR mode only.

(22) This supply follows VCCR_GXB for both GX and GT channels.

(23) When you use fPLL as a TXPLL of the transceiver.

- ■ XFI

- ■ ASI

- ■ HiGig/HiGig+

- ■ HiGig2/HiGig2+

- ■ Serial Data Converter (SDC)

- ■ GPON

- ■ SDI

- ■ SONET

- ■ Fibre Channel (FC)

- ■ PCIe

- ■ QPI

- ■ SFF-8431

Download the Stratix V Characterization Report Tool to view the characterization report summary for these protocols.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks, configuration, and JTAG specifications.

Clock Tree Specifications

Table 30 lists the clock tree specifications for Stratix V devices.

Table 30. Clock Tree Performance for Stratix V Devices [1]

Symbol	Performance			Unit
	C1, C2, C2L, I2, and I2L	C3, I3, I3L, and I3YY	C4, I4	
Global and Regional Clock	717	650	580	MHz
Periphery Clock	550	500	500	MHz

Note to Table 30:

(1) The Stratix V ES devices are limited to 600 MHz core clock tree performance.

Periphery Performance

This section describes periphery performance, including high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the **LVDS** high-speed I/O interface, external memory interface, and the **PCI/PCI-X** bus interface. General-purpose I/O standards such as 3.3-, 2.5-, 1.8-, and 1.5-**LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2-**LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

☞ The actual achievable frequency depends on design- and system-specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 36 lists high-speed I/O timing for Stratix V devices.

Table 36. High-Speed I/O Specifications for Stratix V Devices [(1), (2)] **(Part 1 of 4)**

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4,I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 [(4)]	5	—	800	5	—	800	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards [(3)]	Clock boost factor W = 1 to 40 [(4)]	5	—	800	5	—	800	5	—	625	5	—	525	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards	Clock boost factor W = 1 to 40 [(4)]	5	—	520	5	—	520	5	—	420	5	—	420	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	800	5	—	800	5	—	625 [(5)]	5	—	525 [(5)]	MHz

Table 36. High-Speed I/O Specifications for Stratix V Devices [1], [2] **(Part 2 of 4)**

Symbol	Conditions	C1			C2, C2L, I2, I2L			C3, I3, I3L, I3YY			C4, I4			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transmitter														
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10 [9], [11], [12], [13], [14], [15], [16]	[6]	—	1600	[6]	—	1434	[6]	—	1250	[6]	—	1050	Mbps
	SERDES factor J ≥ 4 LVDS TX with DPA [12], [14], [15], [16]	[6]	—	1600	[6]	—	1600	[6]	—	1600	[6]	—	1250	Mbps
	SERDES factor J = 2, uses DDR Registers	[6]	—	[7]	[6]	—	[7]	[6]	—	[7]	[6]	—	[7]	Mbps
	SERDES factor J = 1, uses SDR Register	[6]	—	[7]	[6]	—	[7]	[6]	—	[7]	[6]	—	[7]	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) [10]	SERDES factor J = 4 to 10 [17]	[6]	—	1100	[6]	—	1100	[6]	—	840	[6]	—	840	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	—	—	0.1	UI
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate 600 Mbps - 1.25 Gbps	—	—	300	—	—	300	—	—	300	—	—	325	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	0.2	—	—	0.2	—	—	0.2	—	—	0.25	UI

Table 38. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate ≥ 1.25 Gbps

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 9 shows the **LVDS** soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate < 1.25 Gbps.

Figure 9. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate < 1.25 Gbps

DLL Range, DQS Logic Block, and Memory Output Clock Jitter Specifications

Table 39 lists the DLL range specification for Stratix V devices. The DLL is always in 8-tap mode in Stratix V devices.

Table 39. DLL Range Specifications for Stratix V Devices [(1)]

C1	C2, C2L, I2, I2L	C3, I3, I3L, I3YY	C4,I4	Unit
300-933	300-933	300-890	300-890	MHz

Note to Table 39:

(1) Stratix V devices support memory interface frequencies lower than 300 MHz, although the reference clock that feeds the DLL must be at least 300 MHz. To support interfaces below 300 MHz, multiply the reference clock feeding the DLL to ensure the frequency is within the supported range of the DLL.

Table 40 lists the DQS phase offset delay per stage for Stratix V devices.

Table 40. DQS Phase Offset Delay Per Setting for Stratix V Devices [(1), (2)] **(Part 1 of 2)**

Speed Grade	Min	Max	Unit
C1	8	14	ps
C2, C2L, I2, I2L	8	14	ps
C3,I3, I3L, I3YY	8	15	ps

Table 42. Memory Output Clock Jitter Specification for Stratix V Devices [1], **(Part 2 of 2)** [2], [3]

Clock Network	Parameter	Symbol	C1		C2, C2L, I2, I2L		C3, I3, I3L, I3YY		C4, I4		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
PHY Clock	Clock period jitter	$t_{JIT(per)}$	−25	25	−25	25	−30	30	−35	35	ps
	Cycle-to-cycle period jitter	$t_{JIT(cc)}$	−50	50	−50	50	−60	60	−70	70	ps
	Duty cycle jitter	$t_{JIT(duty)}$	−37.5	37.5	−37.5	37.5	−45	45	−56	56	ps

Notes to Table 42:

(1) The clock jitter specification applies to the memory output clock pins generated using differential signal-splitter and DDIO circuits clocked by a PLL output routed on a PHY, regional, or global clock network as specified. Altera recommends using PHY clock networks whenever possible.

(2) The clock jitter specification applies to the memory output clock pins clocked by an integer PLL.

(3) The memory output clock jitter is applicable when an input jitter of 30 ps peak-to-peak is applied with bit error rate (BER) -12, equivalent to 14 sigma.

OCT Calibration Block Specifications

Table 43 lists the OCT calibration block specifications for Stratix V devices.

Table 43. OCT Calibration Block Specifications for Stratix V Devices

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by the OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for OCT R_S/R_T calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for the OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the dyn_term_ctrl and oe signal transitions in a bidirectional I/O buffer to dynamically switch between OCT R_S and R_T (Figure 10)	—	2.5	—	ns

Figure 10 shows the timing diagram for the oe and dyn_term_ctrl signals.

Figure 10. Timing Diagram for oe and dyn_term_ctrl Signals

Table 46. JTAG Timing Parameters and Values for Stratix V Devices

Symbol	Description	Min	Max	Unit
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 [1]	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 [1]	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 [1]	ns

Notes to Table 46:

(1) A 1 ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

(2) The minimum TCK clock period is 167 ns if VCCBAT is within the range 1.2V-1.5V when you perform the volatile key programming.

Raw Binary File Size

For the POR delay specification, refer to the "POR Delay Specification" section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices".

Table 47 lists the uncompressed raw binary file (**.rbf**) sizes for Stratix V devices.

Table 47. Uncompressed .rbf Sizes for Stratix V Devices

Family	Device	Package	Configuration .rbf Size (bits)	IOCSR .rbf Size (bits) [4], [5]
Stratix V GX	5SGXA3	H35, F40, F35 [2]	213,798,880	562,392
		H29, F35 [3]	137,598,880	564,504
	5SGXA4	—	213,798,880	563,672
	5SGXA5	—	269,979,008	562,392
	5SGXA7	—	269,979,008	562,392
	5SGXA9	—	342,742,976	700,888
	5SGXAB	—	342,742,976	700,888
	5SGXB5	—	270,528,640	584,344
	5SGXB6	—	270,528,640	584,344
	5SGXB9	—	342,742,976	700,888
	5SGXBB	—	342,742,976	700,888
Stratix V GT	5SGTC5	—	269,979,008	562,392
	5SGTC7	—	269,979,008	562,392
Stratix V GS	5SGSD3	—	137,598,880	564,504
	5SGSD4	F1517	213,798,880	563,672
		—	137,598,880	564,504
	5SGSD5	—	213,798,880	563,672
	5SGSD6	—	293,441,888	565,528
	5SGSD8	—	293,441,888	565,528

Active Serial Configuration Timing

Table 52 lists the DCLK frequency specification in the AS configuration scheme.

Table 52. DCLK Frequency Specification in the AS Configuration Scheme *(1), (2)*

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 52:

(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

Figure 14 shows the single-device configuration setup for an AS ×1 mode.

Figure 14. AS Configuration Timing

Notes to Figure 14:

(1) If you are using AS ×4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.

(2) The initialization clock can be from internal oscillator or CLKUSR pin.

(3) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 53 lists the timing parameters for AS ×1 and AS ×4 configurations in Stratix V devices.

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices *(1), (2)* **(Part 1 of 2)**

Symbol	Parameter	Minimum	Maximum	Units
t_{CO}	DCLK falling edge to AS_DATA0/ASDO output	—	2	ns
t_{SU}	Data setup time before falling edge on DCLK	1.5	—	ns
t_H	Data hold time after falling edge on DCLK	0	—	ns

Table 53. AS Timing Parameters for AS ×1 and AS ×4 Configurations in Stratix V Devices [1], [2] **(Part 2 of 2)**

Symbol	Parameter	Minimum	Maximum	Units
t_{CD2UM}	`CONF_DONE` high to user mode [3]	175	437	μs
t_{CD2CU}	`CONF_DONE` high to `CLKUSR` enabled	4 × maximum `DCLK` period	—	—
t_{CD2UMC}	`CONF_DONE` high to user mode with `CLKUSR` option on	t_{CD2CU} + (8576 × `CLKUSR` period)	—	—

Notes to Table 53:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 54 on page 63.

(3) To enable the `CLKUSR` pin as the initialization clock source and to obtain the maximum frequency specification on this pin, refer to the Initialization section of the "Configuration, Design Security, and Remote System Upgrades in Stratix V Devices" chapter.

Passive Serial Configuration Timing

Figure 15 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device, MAX V device, or microprocessor as an external host.

Figure 15. PS Configuration Timing Waveform [1]

Notes to Figure 15:

(1) The beginning of this waveform shows the device in user mode. In user mode, `nCONFIG`, `nSTATUS`, and `CONF_DONE` are at logic high levels. When `nCONFIG` is pulled low, a reconfiguration cycle begins.

(2) After power-up, the Stratix V device holds `nSTATUS` low for the time of the POR delay.

(3) After power-up, before and during configuration, `CONF_DONE` is low.

(4) Do not leave `DCLK` floating after configuration. You can drive it high or low, whichever is more convenient.

(5) `DATA0` is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

(6) To ensure a successful configuration, send the entire configuration data to the Stratix V device. `CONF_DONE` is released high after the Stratix V device receives all the configuration data successfully. After `CONF_DONE` goes high, send two additional falling edges on `DCLK` to begin initialization and enter user mode.

(7) After the option bit to enable the `INIT_DONE` pin is configured into the device, the `INIT_DONE` goes low.

Table 54 lists the PS configuration timing parameters for Stratix V devices.

Table 54. PS Timing Parameters for Stratix V Devices

Symbol	Parameter	Minimum	Maximum	Units
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1,506 [1]	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1,506 [2]	µs
t_{CF2CK} [5]	nCONFIG high to first rising edge on DCLK	1,506	—	µs
t_{ST2CK} [5]	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	$0.45 \times 1/f_{MAX}$	—	s
t_{CL}	DCLK low time	$0.45 \times 1/f_{MAX}$	—	s
t_{CLK}	DCLK period	$1/f_{MAX}$	—	s
f_{MAX}	DCLK frequency	—	125	MHz
t_{CD2UM}	CONF_DONE high to user mode [3]	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	$4 \times$ maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (8576 × CLKUSR period) [4]	—	—

Notes to Table 54:

(1) This value is applicable if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) This value is applicable if you do not delay configuration by externally holding the nSTATUS low.

(3) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(4) To enable the CLKUSR pin as the initialization clock source and to obtain the maximum frequency specification on these pins, refer to the "Initialization" section.

(5) If nSTATUS is monitored, follow the t_{ST2CK} specification. If nSTATUS is not monitored, follow the t_{CF2CK} specification.

Initialization

Table 55 lists the initialization clock source option, the applicable configuration schemes, and the maximum frequency.

Table 55. Initialization Clock Source Option and the Maximum Frequency

Initialization Clock Source	Configuration Schemes	Maximum Frequency	Minimum Number of Clock Cycles [1]
Internal Oscillator	AS, PS, FPP	12.5 MHz	
CLKUSR	AS, PS, FPP [2]	125 MHz	8576
DCLK	PS, FPP	125 MHz	

Notes to Table 55:

(1) The minimum number of clock cycles required for device initialization.

(2) To enable CLKUSR as the initialization clock source, turn on the **Enable user-supplied start-up clock (CLKUSR)** option in the Quartus II software from the **General** panel of the **Device and Pin Options** dialog box.