2 &) ' ! > &$" ! $41?@<A , B C

2 (/ "$0=$D4 > E&FF&F1C0 ' - ! ' ! #"- !))&-=DG

8 . .)0 ' / "0 ! #=$! H$D4 > E&FF&F$1
C0 ' - ! ' ! #"- !))&-=D

; &" / 0)=	
- ,	.
$ -	%0 &
$, #	%1
,	2/ 3#
$	1 , -
-	- . 4 5 6
7 .	( )
- , #	' 281 9 28 * %
-	; <! , 3
- 4 . , #	
4! , #	&8 * %
= , 9= = :	2 0= > 0 0=
6 $	
.	
.	/ ?$ > @ ?$ 9 ! :
	3
- $	2/ 6 -
, 6 -	
- A4< B *	@@ 0&' 2/

5. FUNCTIONAL DESCRIPTION

The W77E516 is 8052 pin compatible and instruction set compatible. It includes the resources of the standard 8052 such as four 8-bit I/O Ports, three 16-bit timer/counters, and full duplex serial port and interrupt sources.

The W77E516 features a faster running and better performance 8-bit CPU with a redesigned core processor without wasted clock and memory cycles. It improves the performance not just by running at high frequency but also by reducing the machine cycle duration from the standard 8052 period of twelve clocks to four clock cycles for the majority of instructions. This improves performance by an average of 1.5 to 3 times. The W77E516 also provides dual Data Pointers (DPTRs) to speed up block data memory transfers. It can also adjust the duration of the MOVX instruction (access to off-chip data memory) between two machine cycles and nine machine cycles. This flexibility allows the W77E516 to work efficiently with both fast and slow RAMs and peripheral devices. In addition, the W77E516 contains on-chip 1KB MOVX SRAM, the address of which is between 0000H and 03FFH. It only can be accessed by MOVX instruction; this on-chip SRAM is optional under software control.

The W77E516 is an 8052 compatible device that gives the user the features of the original 8052 device, but with improved speed and power consumption characteristics. It has the same instruction set as the 8051 family, with one addition: DEC DPTR (op-code A5H, the DPTR is decreased by 1). While the original 8051 family was designed to operate at 12 clock periods per machine cycle, the W77E516 operates at a much reduced clock rate of only 4 clock periods per machine cycle. This naturally speeds up the execution of instructions. Consequently, the W77E516 can run at a higher speed as compared to the original 8052, even if the same crystal is used. Since the W77E516 is a fully static CMOS design, it can also be operated at a lower crystal clock, giving the same throughput in terms of instruction execution, yet reducing the power consumption.

The 4 clocks per machine cycle feature in the W77E516 is responsible for a three-fold increase in execution speed. The W77E516 has all the standard features of the 8052, and has a few extra peripherals and features as well.

5.1 I/O Ports

The W77E516 has four 8-bit ports and one extra 4-bit port. Port 0 can be used as an Address/Data bus when external program is running or external memory/device is accessed by MOVC or MOVX instruction. In these cases, it has strong pull-ups and pull-downs, and does not need any external pull-ups. Otherwise it can be used as a general I/O port with open-drain circuit. Port 2 is used chiefly as the upper 8-bits of the Address bus when port 0 is used as an address/data bus. It also has strong pull-ups and pull-downs when it serves as an address bus. Port 1 and 3 act as I/O ports with alternate functions. Port 4 is only available on 44-pin PLCC/QFP package type. It serves as a general purpose I/O port as Port 1 and Port 3. The P4.0 has an alternate function $\overline{\text{WAIT}}$ that is the wait state control signal. When wait state control signal is enabled, P4.0 is input only.

5.2 Serial I/O

The W77E516 has two enhanced serial ports that are functionally similar to the serial port of the original 8052 family. However the serial ports on the W77E516 can operate in different modes in order to obtain timing similarity as well. Note that the serial port 0 can use Timer 1 or 2 as baud rate generator, but the serial port 1 can only use Timer 1 as baud rate generator . The serial ports have the enhanced features of Automatic Address recognition and Frame Error detection.

5.3 Timers

The W77E516 has three 16-bit timers that are functionally similar to the timers of the 8052 family. When used as timers, they can be set to run at either 4 clocks or 12 clocks per count, thus providing the user with the option of operating in a mode that emulates the timing of the original 8052. The W77E516 has an additional feature, the watchdog timer. This timer is used as a System Monitor or as a very long time period timer.

5.4 Interrupts

The Interrupt structure in the W77E516 is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W77E516 provides 12 interrupt resources with two-priority level, including six external interrupt sources, timer interrupts, serial I/O interrupts and power-fail interrupt.

5.5 Data Pointers

The original 8052 had only one 16-bit Data Pointer (DPL, DPH). In the W77E516, there is an additional 16-bit Data Pointer (DPL1, DPH1). This new Data Pointer uses two SFR locations that were unused in the original 8052. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

5.6 Power Management

Like the standard 80C52, the W77E516 also has IDLE and POWER DOWN modes of operation. The W77E516 provides a new Economy mode that allow user to switch the internal clock rate divided by 4, 64 or 1024. In the IDLE mode, the clock to the CPU core is stopped while the timers; serial ports and interrupts clock continue to operate. In the POWER DOWN mode, the entire clock is stopped and the chip operation is completely stopped. This is the lowest power consumption state.

5.7 On-chip Data SRAM

The W77E516 has 1K Bytes of data space SRAM which is read/write accessible and is memory mapped. This on-chip MOVX SRAM is reached by the MOVX instruction. It is not used for executable program memory. There is no conflict or overlap among the 256 bytes Scratchpad RAM and the 1K Bytes MOVX SRAM as they use different addressing modes and separate instructions. Setting the DME0 bit in the PMR register enables the on-chip MOVX SRAM. After a reset, the DME0 bit is cleared such that the on-chip MOVX SRAM is disabled, and all data memory spaces 0000H 4 FFFFH access to the external memory.

SM1_1: Serial port 1 Mode bit 1:

SM0_1	SM1_1	Mode	Description	Length	Baud rate
0	0	0	Synchronous	8	4/12 Tclk
0	1	1	Asynchronous	10	variable
1	0	2	Asynchronous	11	64/32 Tclk
1	1	3	Asynchronous	11	variable

SM2_1: Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2_1 is set to 1, then RI_1 will not be activated if the received 9th data bit (RB8_1) is 0. In mode 1, if SM2_1 = 1, then RI_1 will not be activated if a valid stop bit was not received. In mode 0, the SM2_1 bit controls the serial port 1 clock. If set to 0, then the serial port 1 runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become divide by 4 of the oscillator clock. This results in faster synchronous serial communication.

REN_1: Receive enable: When set to 1 serial reception is enabled, otherwise reception is disabled.

TB8_1: This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.

RB8_1: In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2_1 = 0, RB8_1 is the stop bit that was received. In mode 0 it has no function.

TI_1: Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

RI_1: Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2_1 apply to this bit. This bit can be cleared only by software.

Serial Data Buffer 1

Bit:	7	6	5	4	3	2	1	0
	SBUF1.7	SBUF1.6	SBUF1.5	SBUF1.4	SBUF1.3	SBUF1.2	SBUF1.1	SBUF1.0

Mnemonic: SBUF1 Address: C1h

SBUF1.7 4 0: Serial data of the serial port 1 is read from or written to this location. It actually consists of two separate 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write accesses are to the transmit data buffer.

WSCON

Bit:	7	6	5	4	3	2	1	0
	WS	-	-	-	-	-	-	-

Mnemonic: WSCON Address: C2h

WS: Wait State Signal Enable. Setting this bit enables the $\overline{WAIT}$ signal on P4.0. The device will sample the wait state control signal $\overline{WAIT}$ via P4.0 during MOVX instruction. This bit is time access protected.

```
TA          REG   C7H
WSCON REG   C2H
CKCON       REG   8EH
MOV         TA, #AAH
MOV         TA, #55H
ORL         WSCON, #10000000B; Set WS bit and stretch value = 0 to enable wait signal.
```

Power Management Register

Bit:	7	6	5	4	3	2	1	0
	CD1	CD0	SWB	-	-	ALE-OFF	-	DME0

Mnemonic: PMR Address: C4h

CD1, CD0: Clock Divide Control. These bit selects the number of clocks required to generate one machine cycle. There are three modes including divide by 4, 64 or 1024. Switching between modes must first go back divide by 4 mode. For instance, to go from 64 to 1024 clocks/machine cycle the device must first go from 64 to 4 clocks/machine cycle, and then from 4 to 1024 clocks/machine cycle.

CD1,	CD0	Clocks/machine Cycle
0	0	Reserved
0	1	4
1	0	64
1	1	1024

SWB: Switchback Enable. Setting this bit allows an enabled external interrupt or serial port activity to force the CD1, CD0 to divide by 4 state (0,1). The device will switch modes at the start of the jump to interrupt service routine while a external interrupt is enabled and actually recognized by micro controller. While a serial port reception, the switchback occurs at the start of the instruction following the falling edge of the start bit.

ALE0FF: This bit disables the expression of the ALE signal on the device pin during all on-board program and data memory accesses. External memory accesses will automatically enable ALE independent of ALEOFF.

0 = ALE expression is enable; 1 = ALE expression is disable

DME0: This bit determines the on-chip MOVX SRAM to be enabled or disabled. Set this bit to 1 will enable the on-chip 1KB MOVX SRAM.

Status Register

Bit:	7	6	5	4	3	2	1	0
	-	HIP	LIP	XTUP	SPTA1	SPRA1	SPTA0	SPRA0

Mnemonic: STATUS Address: C5h

HIP: High Priority Interrupt Status. When set, it indicates that software is servicing a high priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.

LIP: Low Priority Interrupt Status. When set, it indicates that software is servicing a low priority interrupt. This bit will be cleared when the program executes the corresponding RETI instruction.

XTUP: Crystal Oscillator Warm-up Status. When set, this bit indicates CPU has detected clock to be ready. Each time the crystal oscillator is restarted by exit from power down mode, hardware will clear this bit. This bit is set to 1 after a power-on reset.

SPTA1: Serial Port 1 Transmit Activity. This bit is set during serial port 1 is currently transmitting data. It is cleared when TI_1 bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

SPRA1: Serial Port 1 Receive Activity. This bit is set during serial port 1 is currently receiving a data. It is cleared when RI_1 bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

SPTA0: Serial Port 0 Transmit Activity. This bit is set during serial port 0 is currently transmitting data. It is cleared when TI bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

SPRA0: Serial Port 0 Receive Activity. This bit is set during serial port 0 is currently receiving a data. It is cleared when RI bit is set by hardware. Changing the Clock Divide Control bits CD0, CD1 will be ignored when this bit is set to 1 and SWB = 1.

Timed Access

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TfA.0

Mnemonic: TA Address: C7h

TA: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

Timer 2 Control

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	C / $\overline{T2}$	CP / $\overline{RL2}$

Mnemonic: T2CON Address: C8h

CP / $\overline{RL2}$: Capture/Reload Select. This bit determines whether the capture or reload function will be used for timer 2. If either RCLK or TCLK is set, this bit will be ignored and the timer will function in an auto-reload mode following each overflow. If the bit is 0 then auto-reload will occur when timer 2 overflows or a falling edge is detected on T2EX pin if EXEN2 = 1. If this bit is 1, then timer 2 captures will occur when a falling edge is detected on T2EX pin if EXEN2 = 1.

Timer 2 Mode Control

Bit:	7	6	5	4	3	2	1	0
	HC5	HC4	HC3	HC2	T2CR	-	T2OE	DCEN

Mnemonic: T2MOD Address: C9h

HC5: Hardware Clear $\overline{INT5}$ flag. Setting this bit allows the flag of external interrupt 5 to be automatically cleared by hardware while entering the interrupt service routine.

HC4: Hardware Clear INT4 flag. Setting this bit allows the flag of external interrupt 4 to be automatically cleared by hardware while entering the interrupt service routine.

HC3: Hardware Clear $\overline{INT3}$ flag. Setting this bit allows the flag of external interrupt 3 to be automatically cleared by hardware while entering the interrupt service routine.

HC3: Hardware Clear INT2 flag. Setting this bit allows the flag of external interrupt 3 to be automatically cleared by hardware while entering the interrupt service routine.

T2CR: Timer 2 Capture Reset. In the Timer 2 Capture Mode this bit enables/disables hardware automatically reset Timer 2 while the value in TL2 and TH2 have been transferred into the capture register.

T2OE: Timer 2 Output Enable. This bit enables/disables the Timer 2 clock out function.

DCEN: Down Count Enable: This bit, in conjunction with the T2EX pin, controls the direction that timer 2 counts in 16-bit auto-reload mode.

Timer 2 Capture LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: Cah

RCAP2L: This register is used to capture the TL2 value when a timer 2 is configured in capture mode. RCAP2L is also used as the LSB of a 16-bit reload value when timer 2 is configured in auto-reload mode.

Timer 2 Capture MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

6.4 Instruction

The W77E516 executes all the instructions of the standard 8032 family. The operation of these instructions, their effect on the flag bits and the status bits is exactly the same. However, timing of these instructions is different. The reason for this is two fold. Firstly, in the W77E516, each machine cycle consists of 4 clock periods, while in the standard 8032 it consists of 12 clock periods. Also, in the W77E516 there is only one fetch per machine cycle i.e. 4 clocks per fetch, while in the standard 8032 there can be two fetches per machine cycle, which works out to 6 clocks per fetch.

The advantage the W77E516 has is that since there is only one fetch per machine cycle, the number of machine cycles in most cases is equal to the number of operands that the instruction has. In case of jumps and calls there will be an additional cycle that will be needed to calculate the new address. But overall the W77E516 reduces the number of dummy fetches and wasted cycles, thereby improving efficiency as compared to the standard 8032.

Table 2. Instructions that affect Flag settings

INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY	INSTRUCTION	CARRY	OVERFLOW	AUXILIARY CARRY
ADD	X	X	X	CLR C	0		
ADDC	X	X	X	CPL C	X		
SUBB	X	X	X	ANL C, bit	X		
MUL	0	X		ANL C, bit	X		
DIV	0	X		ORL C, bit	X		
DA A	X			ORL C, bit	X		
RRC A	X			MOV C, bit	X		
RLC A	X			CJNE	X		
SETB C	1						

A “X” indicates that the modification is as per the result of instruction.

Table 3. Instruction Timing for W77E516

INSTRUCTION	HEX OP-CODE	BYTES	W77E516 MACHINE CYCLES	W77E516 CLOCK CYCLES	8032 CLOCK CYCLES	W77E516 VS. 8032 SPEED RATIO
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3

Table 3. Instruction Timing for W77E516, continued

INSTRUCTION	HEX OP-CODE	BYTES	W77E516 MACHINE CYCLES	W77E516 CLOCK CYCLES	8032 CLOCK CYCLES	W77E516 VS. 8032 SPEED RATIO
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
JMP @A+DPTR	73	1	2	8	24	3
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
LCALL addr16	12	3	4	16	24	1.5
LJMP addr16	02	3	4	16	24	1.5
MUL AB	A4	1	5	20	48	2.4
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3

stretching of the instruction only results in the elongation of the MOVX instruction, as if the state of the CPU was held for the desired period. There is no effect on any other instruction or its timing. By default, the Stretch value is set at 1, giving a MOVX instruction of 3 machine cycles. If desired by the user the stretch value can be set to 0 to give the fastest MOVX instruction of only 2 machine cycles.

Table 4. Data Memory Cycle Stretch Values

M2	M1	M0	MACHINE CYCLES	/RD OR /WR STROBE WIDTH IN CLOCKS	/RD OR /WR STROBE WIDTH @25 MHZ	/RD OR /WR STROBE WIDTH @40 MHZ
0	0	0	2	2	80 nS	50 nS
0	0	1	3(default)	4	160 nS	100 nS
0	1	0	4	8	320 nS	200 nS
0	1	1	5	12	480 nS	300 nS
1	0	0	6	16	640 nS	400 nS
1	0	1	7	20	800 nS	500 nS
1	1	0	8	24	960 nS	600 nS
1	1	1	9	28	1120 nS	700 nS

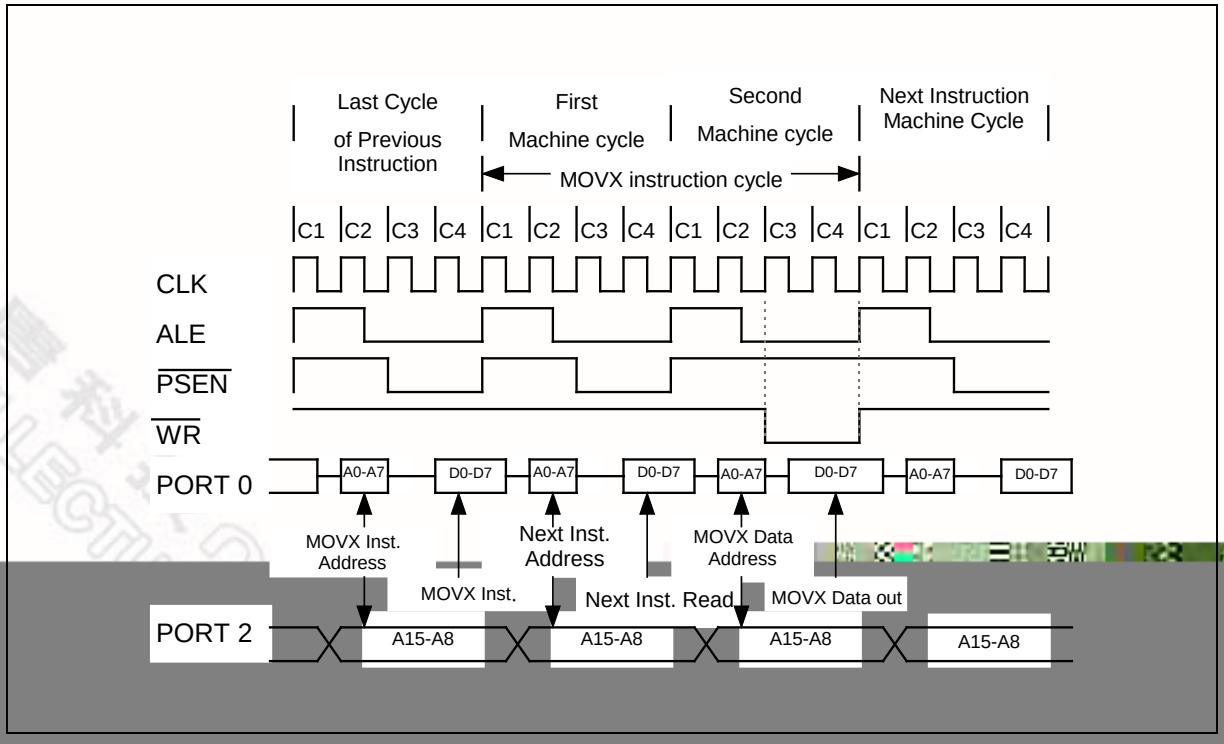


Figure 8: Data Memory Write with Stretch Value = 0

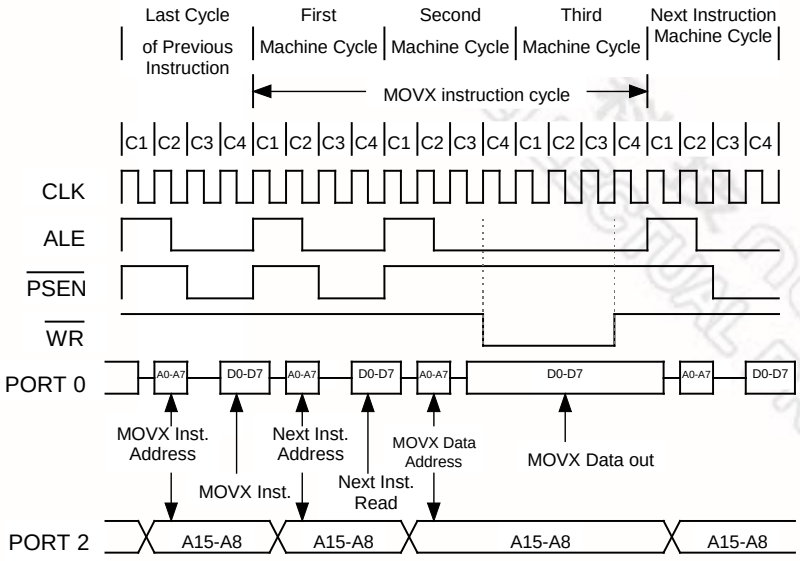


Figure 9: Dada Memory Write with Stretch Value = 1

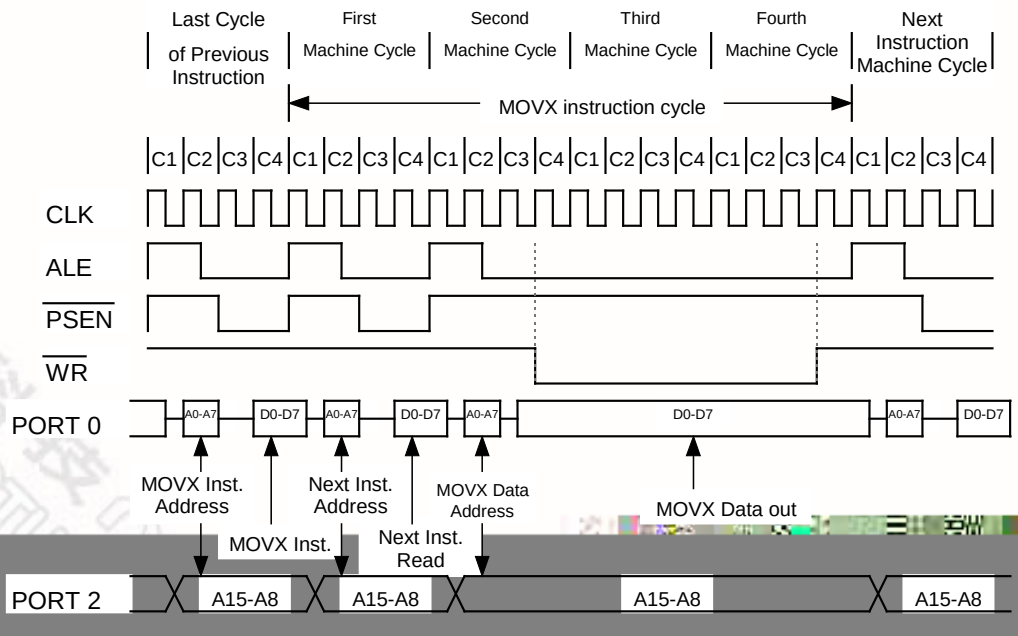


Figure 10: Dada Memory Write with Stretch Value = 2

6.6 Power Management

The W77E516 has several features that help the user to modify the power consumption of the device. The power saving features are basically the POWER DOWN mode, ECONOMY mode and the IDLE mode of operation.

6.6.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The ALE and $\overline{PSEN}$ pins are held high during the Idle state. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle mode.

The Idle mode can also be exited by activating the reset. The device can be put into reset either by applying a high on the external RST pin, a Power on/fail reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles I.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W77E516 is exiting from an Idle mode with a reset, the instruction following the one which put the device into Idle mode is not executed. So there is no danger of unexpected writes.

6.6.2 Economy Mode

The power consumption of microcontroller relates to operating frequency. The W77E516 offers a Economy mode to reduce the internal clock rate dynamically without external components. By default, one machine cycle needs 4 clocks. In Economy mode, software can select 4, 64 or 1024 clocks per machine cycle. It keeps the CPU operating at a acceptable speed but eliminates the power consumption. In the Idle mode, the clock of the core logic is stopped, but all clocked peripherals such as watchdog timer are still running at a rate of clock/4. In the Economy mode, all clocked peripherals run at the same reduced clocks rate as in core logic. So the Economy mode may provide a lower power consumption than idle mode.

Software invokes the Economy mode by setting the appropriate bits in the SFRs. Setting the bits CD0(PMR.6),CD1(PMR.7) decides the instruction cycle rate as below:

CD1	CD0	Clocks/Machine Cycle
0	0	Reserved
0	1	4 (default)
1	0	64
1	1	1024

6.8 Reset State

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the V_{DD} falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost. Hence it should be assumed that after a power on/fail reset, POR = 1, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have FFh written into them which puts the port pins in a high state. Port 0 floats as it does not have on-chip pull-ups.

Table 6. SFR Reset Value

SFR NAME	RESET VALUE	SFR NAME	RESET VALUE
P0	11111111b	IE	00000000b
SP	00000111b	SADDR	00000000b
DPL	00000000b	P3	11111111b
DPH	00000000b	IP	x0000000b
DPL1	00000000b	SADEN	00000000b
DPH1	00000000b	T2CON	00000000b
DPS	00000000b	T2MOD	00000x00b
PCON	00xx0000b	RCAP2L	00000000b
TCON	00000000b	RCAP2H	00000000b
TMOD	00000000b	TL2	00000000b
TL0	00000000b	TH2	00000000b
TL1	00000000b	TA	11111111b
TH0	00000000b	PSW	00000000b
TH1	00000000b	WDCON	0x0x0xx0b
CKCON	00000001b	ACC	00000000b
P1	11111111b	EIE	xxx00000b
SCON	00000000b	B	00000000b
SBUF	xxxxxxxxb	EIP	xxx00000b
P2	11111111b	PC	00000000b
SADDR1	00000000b	SADEN1	00000000b
SCON1	00000000b	SBUF1	xxxxxxxxb
ROMMAP	01xxxxxxb	PMR	010xx0x0b
EXIF	0000xxx0b	STATUS	000x0000b
P4	xxxx1111b		

WTRF: WDCON.2 – Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWT = 0, then this bit will not be affected by the watchdog timer.

EWT: WDCON.1 – Enable Watchdog timer Reset. This bit when set to 1 will enable the Watchdog timer reset function. Setting this bit to 0 will disable the Watchdog timer reset function, but will leave the timer running

RWT: WDCON.0 – Reset Watchdog Timer. This bit is used to clear the Watchdog timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog timer reset is enabled, then the RWT has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog timer reset will occur.

7.4.2 Clock Control

WD1, WD0: CKCON.7, CKCON.6 – Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clock longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The EWT, WDIF and RWT bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the watchdog timer.

7.5 Serial Port

Serial port in the W77E516 is a full duplex port. The W77E516 provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial ports are capable of synchronous as well as asynchronous communication. In Synchronous mode the W77E516 generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receive buffer register. The serial port can operate in four different modes as described below.

7.5.1 Mode 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the W77E516 whether the device is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This baud rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and the W77E516.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of the

8. TIMED ACCESS PROTECTION

The W77E516 has several new features, like the Watchdog timer, on-chip ROM size adjustment, wait state control signal and Power on/fail reset flag, which are crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W77E516 has a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing Aah and immediately 55h to the Timed Access(TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG     0C7h            ; define new register TA, located at 0C7h
MOV     TA, #0Aah
MOV     TA, #055h
```

When the software writes Aah to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (Aah), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
MOV     TA, #0Aah       3 M/C       Note: M/C = Machine Cycles
MOV     TA, #055h       3 M/C
MOV     WDCON, #00h     3 M/C
```

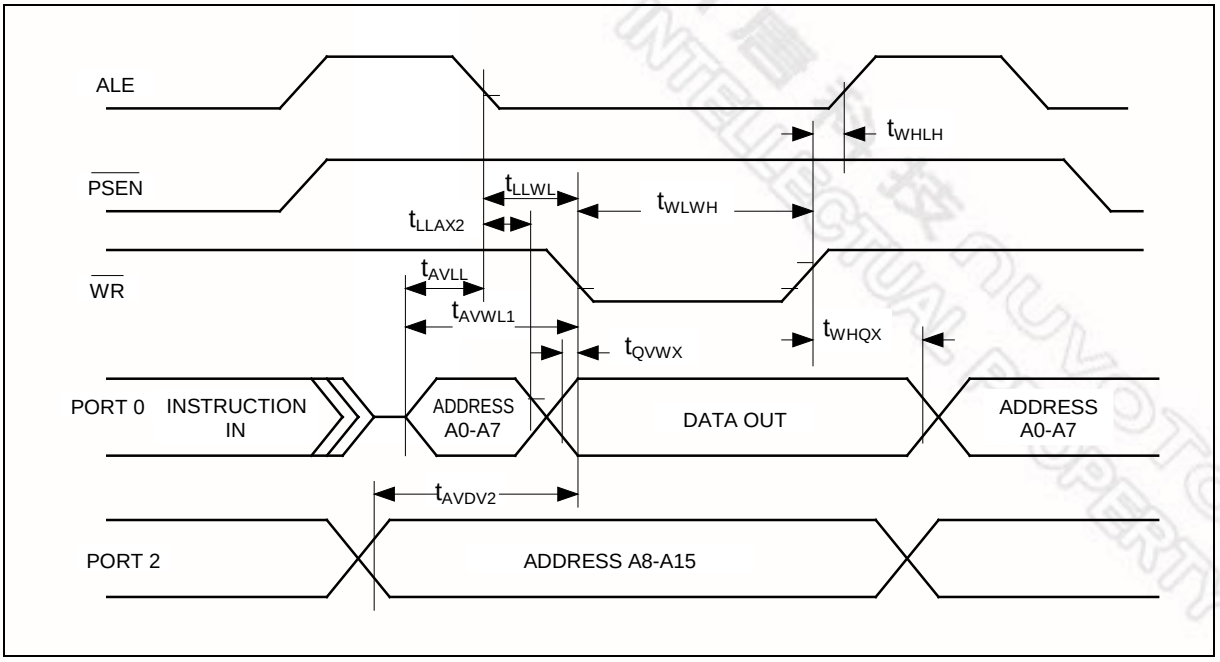
Example 2: Valid access

```
MOV     TA, #0Aah       3 M/C
MOV     TA, #055h       3 M/C
NOP                     1 M/C
SETB    EWT             2 M/C
```

Example 3: Invalid access

```
MOV     TA, #0Aah       3 M/C
MOV     TA, #055h       3 M/C
NOP                     1 M/C
NOP                     1 M/C
CLR     POR             2 M/C
```

11.3 Data Memory Write Cycle



12.2 Expanded External Data Memory and Oscillator

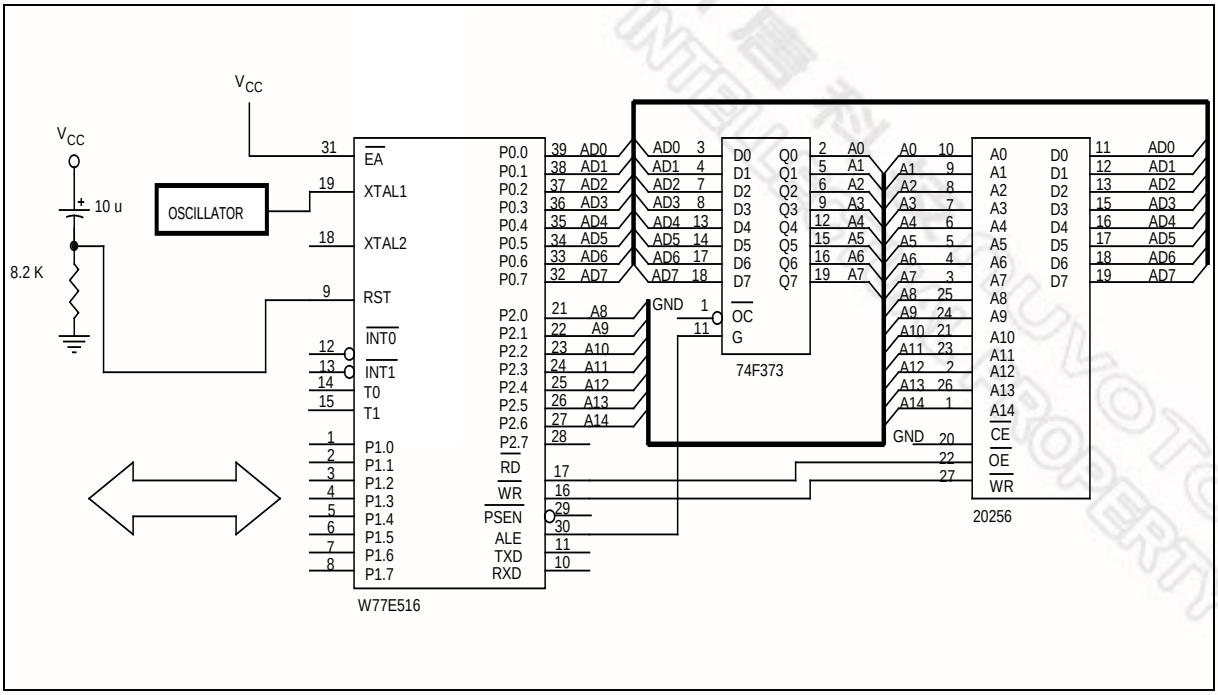


Figure B

```
MAIN_4K:
        MOV   TA, #AAH
        MOV   TA, #55H
        MOV   CHPCON, #03H      ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV   TCON, #00H        ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV   TMOD, #01H        ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV   IP, #00H          ; IP = 00H
        MOV   IE, #82H          ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV   R6, #F0H
        MOV   R7, #FFH
        MOV   TL0, R6
        MOV   TH0, R7
        MOV   TCON, #10H        ; TCON = 10H, TR0 = 1, GO
        MOV   PCON, #01H        ; ENTER IDLE MODE

 UPDATE_64K:
        MOV   TCON, #00H        ; TCON = 00H , TR = 0 TIM0 STOP
        MOV   IP, #00H          ; IP = 00H
        MOV   IE, #82H          ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV   TMOD,#01H         ; TMOD = 01H, MODE1
        MOV   R6, #D0H          ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 mS
                                  DEPENDING ON USER'S SYSTEM CLOCK RATE.
        MOV   R7,#8AH
        MOV   TL0,R6
        MOV   TH0,R7

ERASE_P_4K:
        MOV   SFRCN, #22H       ; SFRCN = 22H, ERASE 64K    APROM0
                                ; SFRCN = A2H, ERASE 64K APROM1
        MOV   TCON, #10H        ; TCON = 10H, TR0 = 1,GO
        MOV   PCON, #01H        ; ENTER IDLE MODE (FOR ERASE OPERATION)
;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV   SFRCN, #0H                ; SFRCN = 00H, READ 64KB APROM0
                                        ; SFRCN = 80H, READ 64KB APROM1
        MOV   SFRAH, #0H                ; START ADDRESS = 0H
        MOV   SFRAL, #0H
        MOV   R6, #FDH                  ; SET TIMER FOR READ OPERATION, ABOUT 1.5 σS.
        MOV   R7, #FFH
        MOV   TL0, R6
        MOV   TH0, R7

BLANK_CHECK_LOOP:
        SETB   TR0                      ; ENABLE TIMER 0
         MOV   PCON, #01H               ; ENTER IDLE MODE
        MOV   A, SFRFD                  ; READ ONE BYTE
         CJNE   A, #FFH, BLANK_CHECK_ERROR
         INC   SFRAL                    ; NEXT ADDRESS
         MOV    A, SFRAL
         JNZ    BLANK_CHECK_LOOP
         INC   SFRAH
         MOV    A, SFRAH
         CJNE   A, #0H,BLANK_CHECK_LOOP ; END ADDRESS = FFFFH
         JMP   PROGRAM_64KROM
```

15. VERSION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	Aug. 2002	-	Initial Issued
A2	Feb. 22, 2005	3	Add lead free package part number
A3	April 18, 2005	85	Add Important Notice
A4	Aug 11, 2005	3, 5, 12 72	Add Port 0 pull-up resisters information Remove encrypt function of Security bits B2 description
A5	September 29, 2006		Remove block diagram
A6	November 6, 2006		Remove all leaded package parts
A7	February 1, 2007	13	Revise the Timer Mode Setting to “Mode 1: 16-bits, no prescale”.
A8	April 12, 2007	50	Revise that Power Down Mode is released by external interrupt configured as either level or edge detect.
A9	November 19, 2007	- 80	Remove NVM description Change chapter 12.1 Figure A to crystal connections

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