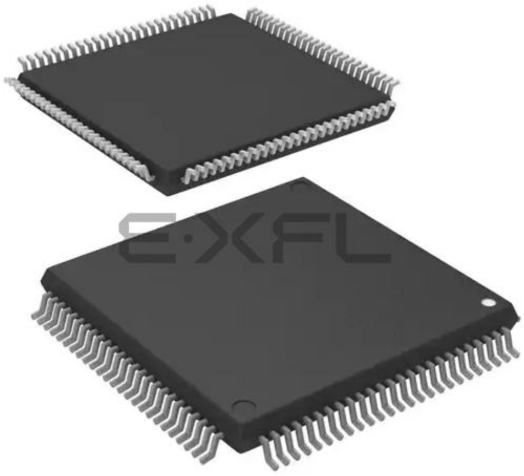
Renesas Electronics America Inc - DF71474BJ80FPV Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	SH-2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, SCI, SSU
Peripherals	POR, PWM, WDT
Number of I/O	57
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 12x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df71474bj80fpv

SH7147 Group Manuals:

Document Title	Document No.
SH7147 Group Hardware Manual	This manual
SH-1/SH-2/SH-DSP Software Manual	REJ09B0171

User's Manuals for Development Tools:

Document Title	Document No.
SuperH™ RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package V.9.00 User's Manual	REJ10B0152
SuperH™ RISC engine High-performance Embedded Workshop 3 User's Manual	REJ10B0025
SuperH RISC engine High-Performance Embedded Workshop 3 Tutorial	REJ10B0023

Application Note:

Document Title	Document No.
SuperH RISC engine C/C++ Compiler Package Application Note	REJ05B0463

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Classification	Symbol	I/O	Name	Function
Controller area network (RCAN-ET)	CTx1*, CTx0	O	Transmit data	Transmit data pin for CAN bus
	CRx1*, CRx0	I	Receive data	Receive data pin for CAN bus
A/D converter (ADC)	AN15 to AN0	I	Analog input pins	Analog input pins
	$\overline{\text{ADTRG}}$	I	A/D conversion trigger input	External trigger input pin for starting A/D conversion
	AVcc	I	Analog power supply	Power supply pin for the A/D converter Connect it to the system power supply (PVcc) when the A/D converter is not used. Connect all AVcc pins to the system power supply (PVcc) The A/D converter does not work if any pin is open.
	AVss	I	Analog ground	Ground pin for the A/D converter Connect it to the system ground (0 V). Connect all AVss pins to the system ground (0 V) correctly. The A/D converter does not work if any pin is open.
	AVrefh	I	Analog reference power supply (high)	Analog reference power supply (high)
	AVrefl	I	Analog reference power supply (low)	Analog reference power supply (low)
I/O ports	PA15 to PA0	I/O	General port	General input/output port pins
	PB7 to PB0	I/O	General port	General input/output port pins
	PD10 to PD0	I/O	General port	General input/output port pins
	PE21 to PE0	I/O	General port	General input/output port pins
User break controller (UBC)	$\overline{\text{UBCTRG}}$	O	User break trigger output	Trigger output pin for UBC condition match

Type	Kinds of Instruction	Op Code	Function	Number of Instructions
Branch instructions	9	BF	Conditional branch, delayed conditional branch (T = 0)	11
		BT	Conditional branch, delayed conditional branch (T = 1)	
		BRA	Unconditional branch	
		BRAF	Unconditional branch	
		BSR	Branch to subroutine procedure	
		BSRF	Branch to subroutine procedure	
		JMP	Unconditional branch	
		JSR	Branch to subroutine procedure	
		RTS	Return from subroutine procedure	
System control instructions	11	CLRT	T bit clear	31
		CLRMAC	MAC register clear	
		LDC	Load into control register	
		LDS	Load into system register	
		NOP	No operation	
		RTE	Return from exception handling	
		SETT	T bit setting	
		SLEEP	Transition to power-down mode	
		STC	Store from control register	
		STS	Store from system register	
		TRAPA	Trap exception handling	
Total:	62			142

9.2 Input/Output Pins

The pin configuration of the BSC is listed in table 9.1.

Table 9.1 Pin Configuration

Name	I/O	Function
A19 to A0	Output	Address bus
D7 to D0	I/O	Data bus
$\overline{\text{CS0}}$ and $\overline{\text{CS1}}$	Output	Chip select
$\overline{\text{RD}}$	Output	Read pulse signal (read data output enable signal)
$\overline{\text{WRL}}$	Output	Indicates byte write through D7 to D0.
$\overline{\text{WAIT}}$	Input	External wait input
$\overline{\text{BREQ}}$	Input	Bus request input
$\overline{\text{BACK}}$	Output	Bus acknowledge output

Table 10.17 TIOR_1 (Channel 1)

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_1 Function**	**TIOC1B Pin Function**
0	0	0	0	Output compare register	Output retained*
			1		Initial output is 0 0 output at compare match
		1	0		Initial output is 0 1 output at compare match
			1		Initial output is 0 Toggle output at compare match
	1	0	0		Output retained
			1		Initial output is 1 0 output at compare match
		1	0		Initial output is 1 1 output at compare match
			1		Initial output is 1 Toggle output at compare match
1	0	0	0	Input capture register	Input capture at rising edge
			1		Input capture at falling edge
		1	x		Input capture at both edges
	1	x	x		Input capture at generation of TGRC_0 compare match/input capture

[Legend]

x: Don't care

Note: * After power-on reset, 0 is output until TIOR is set.

Examples of Phase Counting Mode Operation: In phase counting mode, TCNT counts up or down according to the phase difference between two external clocks. There are four modes, according to the count conditions.

1. Phase counting mode 1

   Figure 10.31 shows an example of phase counting mode 1 operation, and table 10.51 summarizes the TCNT up/down-count conditions.

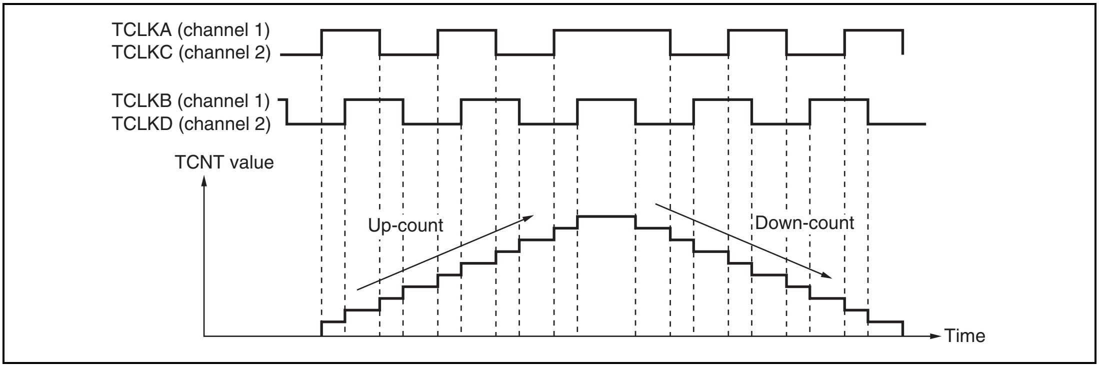

TCLKA (channel 1)
TCLKC (channel 2)
TCLKB (channel 1)
TCLKD (channel 2)
TCNT value
Up-count
Down-count
Time

Figure 10.31 Example of Phase Counting Mode 1 Operation

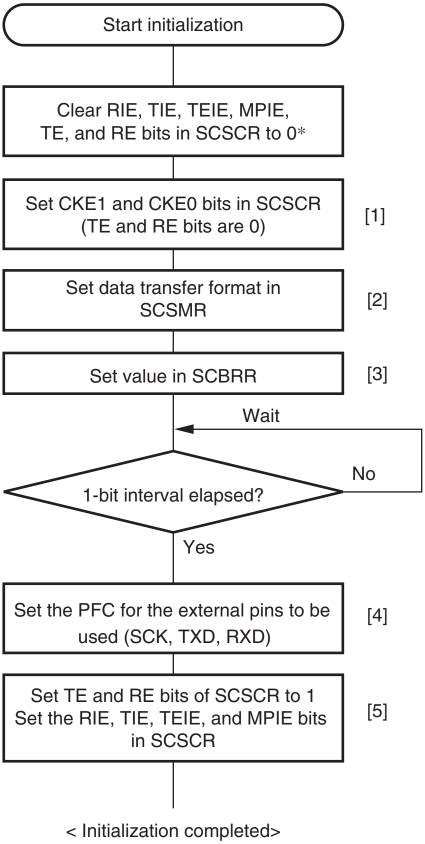
Table 10.51 Up/Down-Count Conditions in Phase Counting Mode 1

TCLKA (Channel 1) TCLKC (Channel 2)	TCLKB (Channel 1) TCLKD (Channel 2)	Operation
High level	↑	Up-count
Low level	↓	
↑	Low level	
↓	High level	
High level	↓	Down-count
Low level	↑	
↑	High level	
↓	Low level	

[Legend]

↑: Rising edge

↓: Falling edge


Start initialization
Clear RIE, TIE, TEIE, MPIE, TE, and RE bits in SCSCR to 0*
Set CKE1 and CKE0 bits in SCSCR (TE and RE bits are 0)
[1]
Set data transfer format in SCSMR
[2]
Set value in SCBRR
[3]
Wait
No
1-bit interval elapsed?
Yes
Set the PFC for the external pins to be used (SCK, TXD, RXD)
[4]
Set TE and RE bits of SCSCR to 1 Set the RIE, TIE, TEIE, and MPIE bits in SCSCR
[5]
< Initialization completed>

[1] Set the clock selection in SCSCR.

[2] Set the data transfer format in SCSMR and SCSDCR.

[3] Write a value corresponding to the bit rate to SCBRR. Not necessary if an external clock is used.

[4] Set PFC of the external pin used. Set RXD input during receiving and TXD output during transmitting. Set SCK input/output according to contents set by CKE1 and CKE0. When CKE1 and CKE0 are 0 in asynchronous mode, setting the SCK pin is unnecessary. Outputting clocks from the SCK pin starts at synchronous clock output setting.

[5] Set the TE bit or RE bit in SCSCR to 1.* Also make settings of the RIE, TIE, TEIE, and MPIE bits. At this time, the TXD, RXD, and SCK pins are ready to be used. The TXD pin is in a mark state during transmitting, and RXD pin is in an idle state for waiting the start bit during receiving.

Note : * In simultaneous transmit/receive operation, the TE and RE bits must be cleared to 0 or set to 1 simultaneously.

Figure 13.3 Sample Flowchart for SCI Initialization

Main Revisions for This Edition

Item | **Page** | **Revision (See Manual for Details)**

7.3.11 Break Control Register (BRCR) | 139 | Description amended

Bit	Bit Name	Initial Value	R/W	Description
7	DBEA	0	R/W	Data Break Enable A Selects whether or not the data bus value is included in the channel A break condition. 0: The data bus value is not included in the channel A break condition 1: The data bus value is included in the channel A break condition
5	DBEB	0	R/W	Data Break Enable B Selects whether or not the data bus value is included in the channel B break condition. 0: The data bus value is not included in the channel B break condition 1: The data bus value is included in the channel B break condition

140 | Note added

Note: The operand size must be specified if the data bus value is included in the break condition and the interrupt cycle is specified in the break condition with the RWA and/or RWB bits.

10.1 Features

Table 10.2 MTU2S Functions | 241 | Table amended

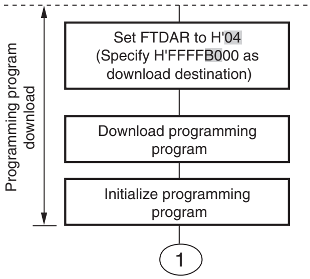
Item	Channel 3	Channel 4	Channel 5
PWM mode 1	—	√	—

15.3.2 A/D Status Registers_0 and _1 (ADSR_0 and ADSR_1) | 642 | Note added

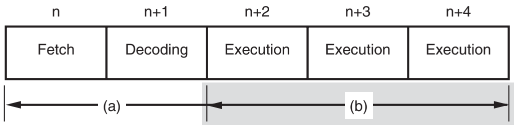
Bit	Bit Name	Initial Value	R/W	Description
7 to 1		All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ADF	0	R/(W)*	A/D End Flag A status flag that indicates the completion of A/D conversion. [Setting condition] • When A/D conversion on all specified channels is completed in scan mode [Clearing conditions] • When 0 is written after reading ADF = 1 • When the DTC is activated by an ADI interrupt and ADDR is read

Note: * Writing 0 to this bit after reading it as 1 clears the flag and is the only allowed way. Do not overwrite this bit with 0 when the value of this bit is 0.

<table>
<tr><th>Item</th><th>Page</th><th>Revision (See Manual for Details)</th></tr>
<tr><td>20.5.2 User Program Mode
(4) Erasing and Programming Procedure in User Program Mode
Figure 20.13 Sample Procedure of Repeating RAM Emulation, Erasing, and Programming (Overview)</td><td>849</td><td>Figure amended


Programming program download
Set FTDAR to H'04 (Specify H'FFFFB000 as download destination)
Download programming program
Initialize programming program
1

</td></tr>
<tr><td></td><td>850</td><td>Description amended
Initialization must be executed for both entry addresses: (download start address for erasing program) + 32 bytes (H'FFFF9020 in this example) and (download start address for programming program) + 32 bytes (H'FFFFB020 in this example).</td></tr>
<tr><td>20.8.2 Interrupts during Programming/Erasing
Figure 20.21 Timing of Contention between SCO Download Request and Interrupt Request</td><td>863</td><td>Figure amended


n
n+1
n+2
n+3
n+4
Fetch
Decoding
Execution
Execution
Execution
(a)
(b)

</td></tr>
<tr><td>(2) Interrupts during Programming/Erasing</td><td></td><td>Description amended
Interrupts during execution of write or erase operations with a downloaded on-chip program and acquisition of bus rights by bus masters other than the CPU are forbidden.</td></tr>
<tr><td>20.8.3 Other Notes
(8) Stack address</td><td>865</td><td>Description added</td></tr>
<tr><td>(9) Illegal access areas when the RAM emulation function is used</td><td></td><td>Description added</td></tr>
<tr><td>Table 20.13 Illegal Access Areas During RAM Emulation Function Use</td><td>866</td><td>Table amended
<table>
<tr><th></th><th>EB0 Selected</th><th>EB1 Selected</th><th>EB2 Selected</th><th>EB3 Selected</th><th>EB4 Selected</th><th>EB5 Selected</th><th>EB6 Selected</th><th>EB7 Selected</th></tr>
<tr><td>Illegal access area</td><td>H'00008000 to H'00008FFF</td><td>H'00009000 to H'00009FFF</td><td>H'0000A000 to H'0000AFFF</td><td>H'0000B000 to H'0000BFFF</td><td>H'0000C000 to H'0000CFFF</td><td>H'0000D000 to H'0000DFFF</td><td>H'0000E000 to H'0000EFFF</td><td>H'0000F000 to H'0000FFFF</td></tr>
<tr><td></td><td>H'00010000 to H'00010FFF</td><td>H'00011000 to H'00011FFF</td><td>H'00012000 to H'00012FFF</td><td>H'00013000 to H'00013FFF</td><td>H'00014000 to H'00014FFF</td><td>H'00015000 to H'00015FFF</td><td>H'00016000 to H'00016FFF</td><td>H'00017000 to H'00017FFF</td></tr>
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