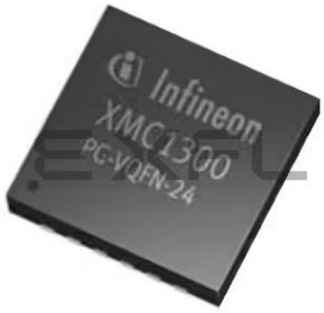
Infineon Technologies - XMC1301Q024F0016ABXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	18
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-24-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301q024f0016abxuma1

  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for processing of external and internal service requests
- MATH Co-processor (MATH)
  - CORDIC unit for trigonometric calculation
  - division unit

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces

Analog Frontend Peripherals

- A/D Converters
  - up to 12 analog input pins
  - 2 sample and hold stages with 8 analog input channels each
  - fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) as general purpose timers
- Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Position Interfaces (POSIF) for hall and quadrature encoders and motor positioning
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG) for fast random data generation

Input/Output Lines

- Tri-stated in input mode
- Push/pull or open drain output mode

Table 4 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T016F0032	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T028X0016	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038X0032	00013013 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038F0064	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083$_H$	AB

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
VSSP	31	25	-	-	-	Power	I/O port ground
VDDP	32	26	-	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	-	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.2 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

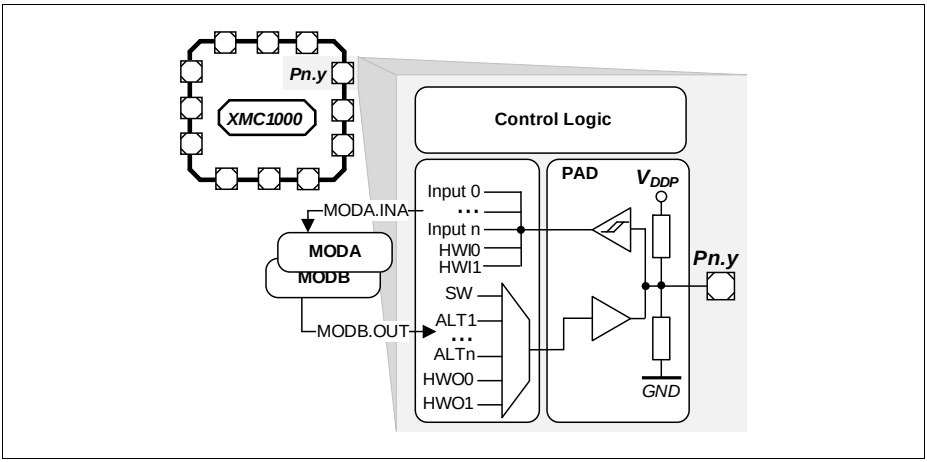


Figure 9 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the **Port I/O Functions** table for the complete Port I/O function mapping.

Table 9 Port I/O Functions (cont'd)

Function	Outputs							Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.6								ACMP1.INN	VADC0.G0CH0		ERU0.2A1	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D	ORC4.AIN		
P2.7								ACMP1.INP	VADC0.G1CH1		ERU0.3A1	USIC0_CH0.DX5C	USIC0_CH1.DX3D	USIC0_CH1.DX4D	ORC5.AIN		
P2.8								ACMP0.INN	VADC0.G0CH1	VADC0.G1CH0	ERU0.3B1	USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C	ORC6.AIN		
P2.9								ACMP0.INP	VADC0.G0CH2	VADC0.G1CH4	ERU0.3B0	USIC0_CH0.DX5A	USIC0_CH1.DX3B	USIC0_CH1.DX4B	ORC7.AIN		
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1		CCU80.OUT30	ACMP0.OUT	USIC0_CH1.DOUT0		VADC0.G0CH3	VADC0.G1CH2	ERU0.2B0	USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F			
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0		CCU80.OUT31	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0	ACMP.REF	VADC0.G0CH4	VADC0.G1CH3	ERU0.2B1	USIC0_CH1.DX0E	USIC0_CH1.DX1E				

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_{ST}	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP} [1]	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on P2 pins with respect to V_{SSP} [2]	V_{INP2}	SR	-0.3	–	V_{DDP} + 0.3	V	–
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN}	SR	-50	–	+50	mA	–

1) Excluding port pins P2.[1,2,6,7,8,9,11].

2) Applicable to port pins P2.[1,2,6,7,8,9,11].

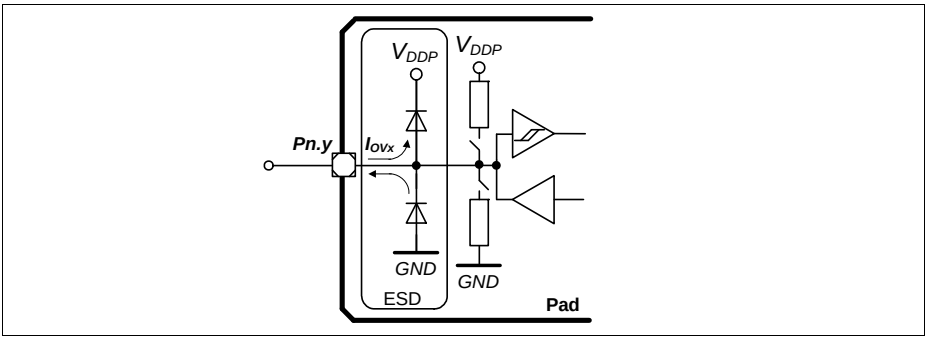


Figure 10 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5$ V $V_{AIN} = V_{DDP} + 0.5$ V $V_{AREF} = V_{DDP} + 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP} + 0.3$ V

Table 14 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5$ V $V_{AIN} = V_{SS} - 0.5$ V $V_{AREF} = V_{SS} - 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS} - 0.3$ V

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis[8)]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.5 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.4 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.2 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up resistor on port pins	R_{PUP}	CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	R_{PDP}	CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current[9)]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[10)]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high currrent pins	I_{MP1A}	SR	-10	50	mA	–
Maximum current into V_{DDP} (TSSOP16, VQFN24)	I_{MVDD1}	SR	–	130	mA	[18)]
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	[18)]

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current out of V_{SS} (TSSOP16, VQFN24)	I_{MVSS1}	SR	–	130	mA	18)
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	18)

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
4) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
5) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
7) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.
8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

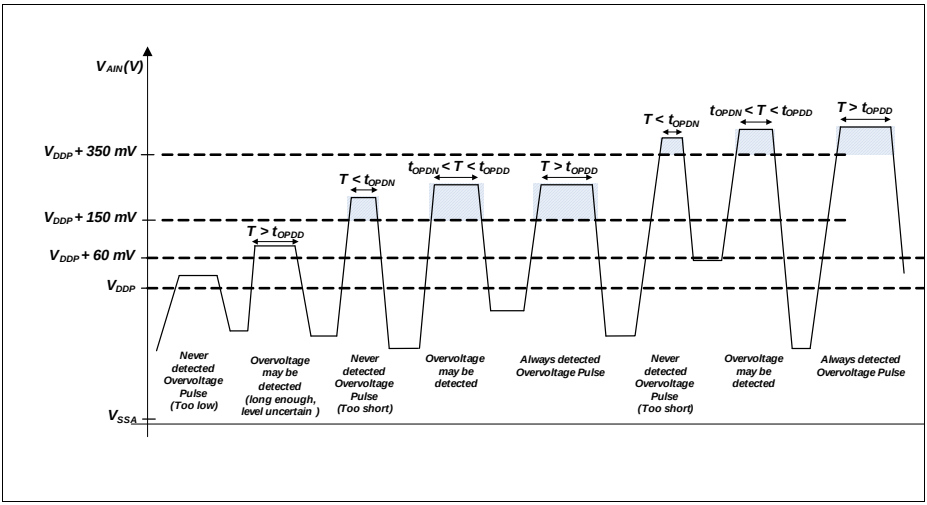


Figure 13 ORC Detection Ranges

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

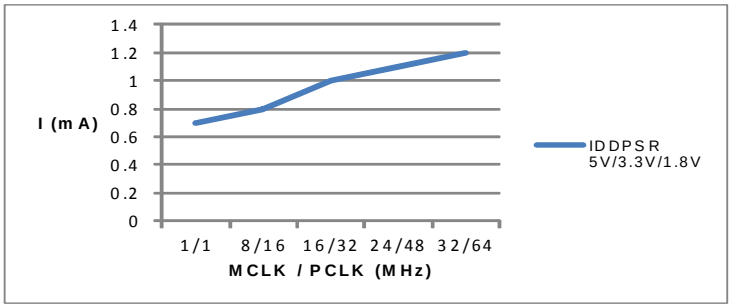
Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
			–	+/-20	–	mV	Low power mode ΔV_{CMP} < 200 mV
Propagation Delay[1)]	t_{PDELAY}	CC	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
			–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
			–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
			–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current Consumption	I_{ACMP}	CC	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	10	–	µA	First active ACMP in low power mode
			–	6	–	µA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	–	+/-15	–	mV	
Filter Delay[1)]	t_{FDELAY}	CC	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

Figure 15 shows typical graphs for sleep mode current for V_{DDP} = 5V, V_{DDP} = 3.3V, V_{DDP} = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSR} over supply voltage V_{DDP} for different clock frequencies

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page / sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	1.3	2		f_{MCLK} = 32 MHz
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{FWSFLASH}$ SR	0	0	1		NVM_CONFIG1.FIXWS = 1_B, $f_{MCLK} \leq$ 16 MHz
		1	1	1		NVM_CONFIG1.FIXWS = 1_B, 16 MHz < $f_{MCLK} \leq$ 32 MHz
Erase Cycles	N_{ECYC} CC	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.3 On-Chip Oscillator Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	64	–	MHz	under nominal conditions[1] after trimming
Accuracy[2]	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (T_A = 0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (T_A = -40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) The accuracy can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

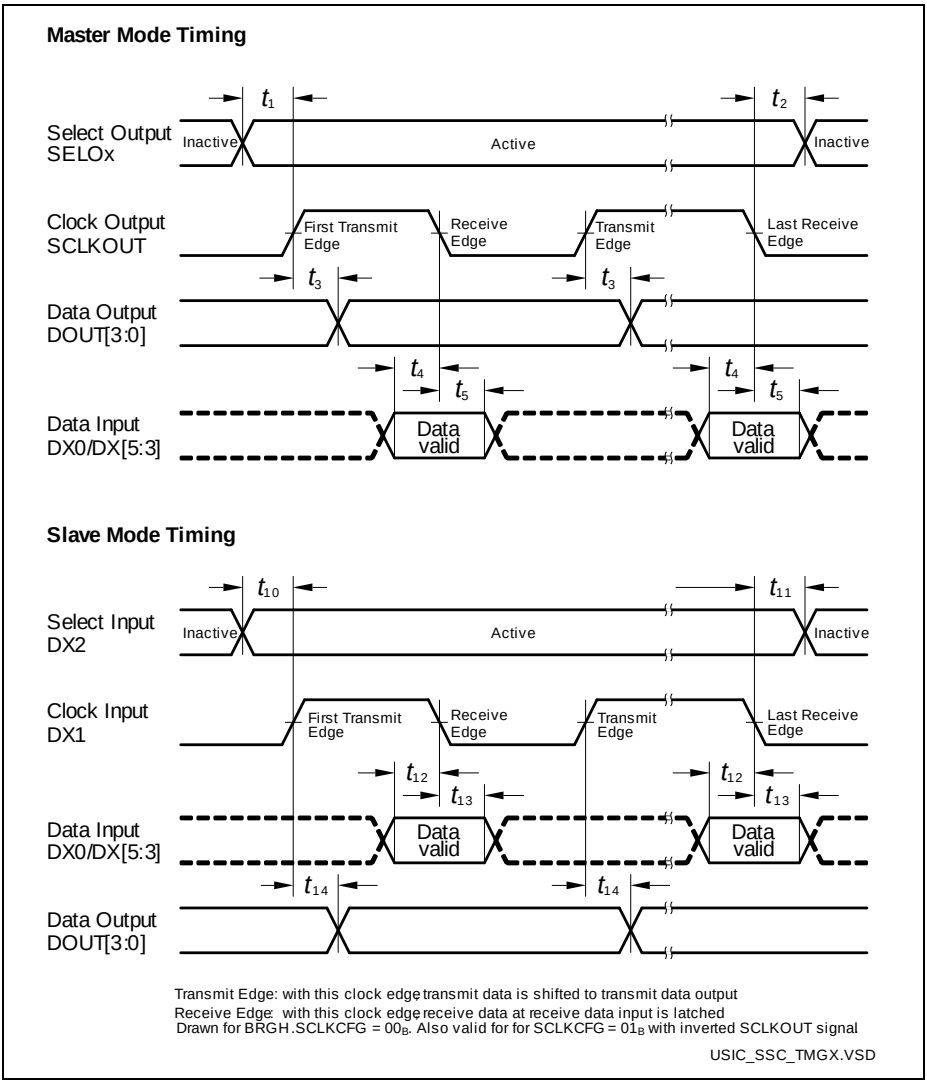


Figure 22 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 31 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

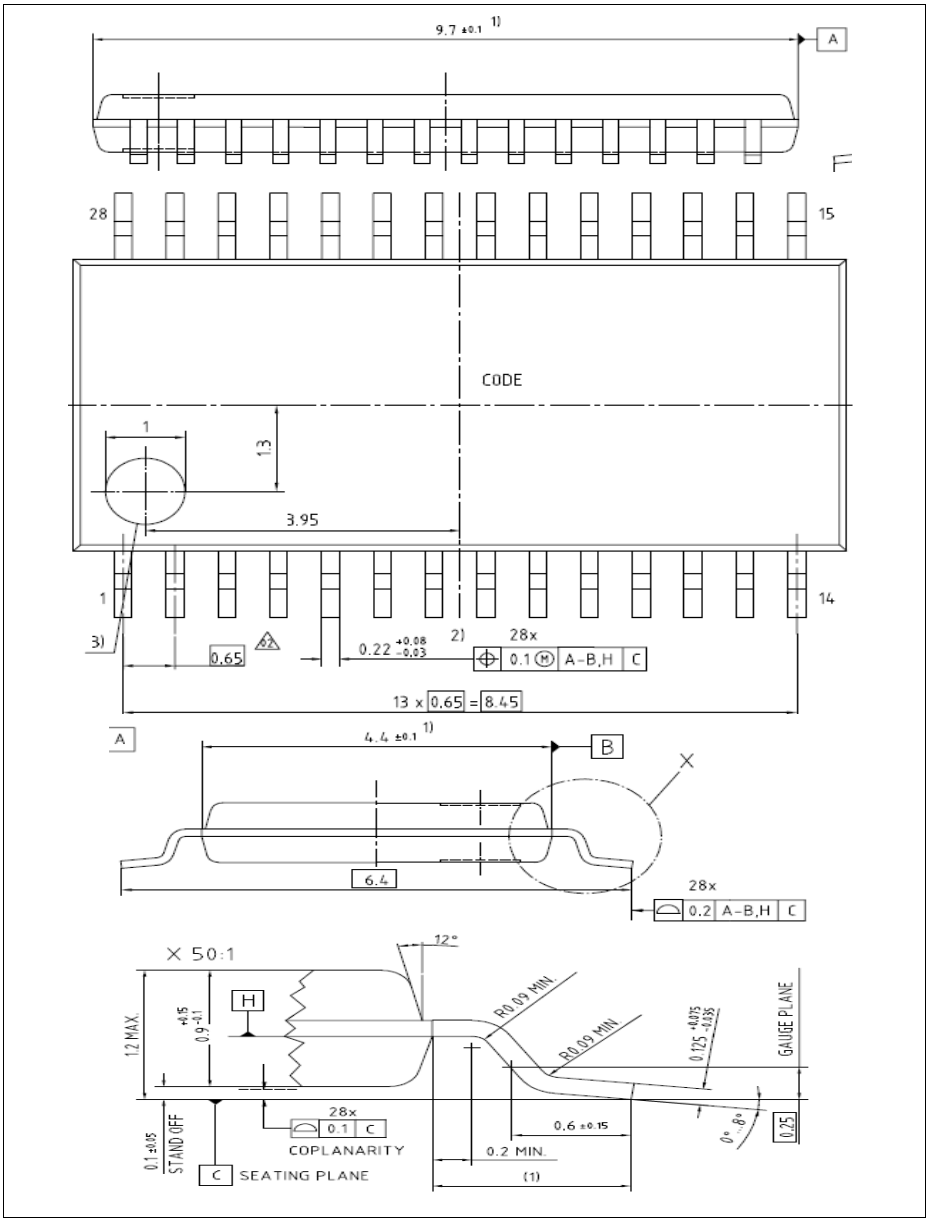


Figure 27 PG-TSSOP-28-16

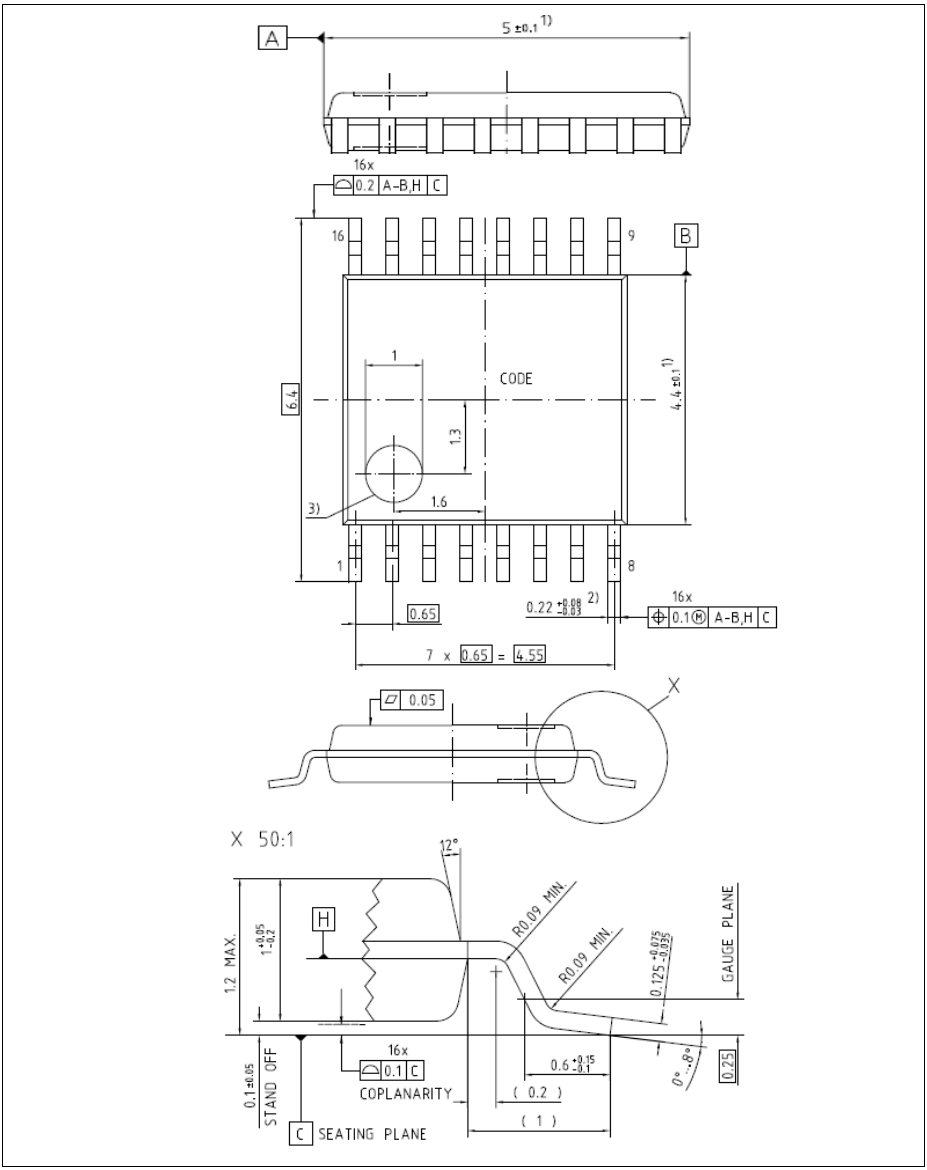


Figure 28 PG-TSSOP-16-8

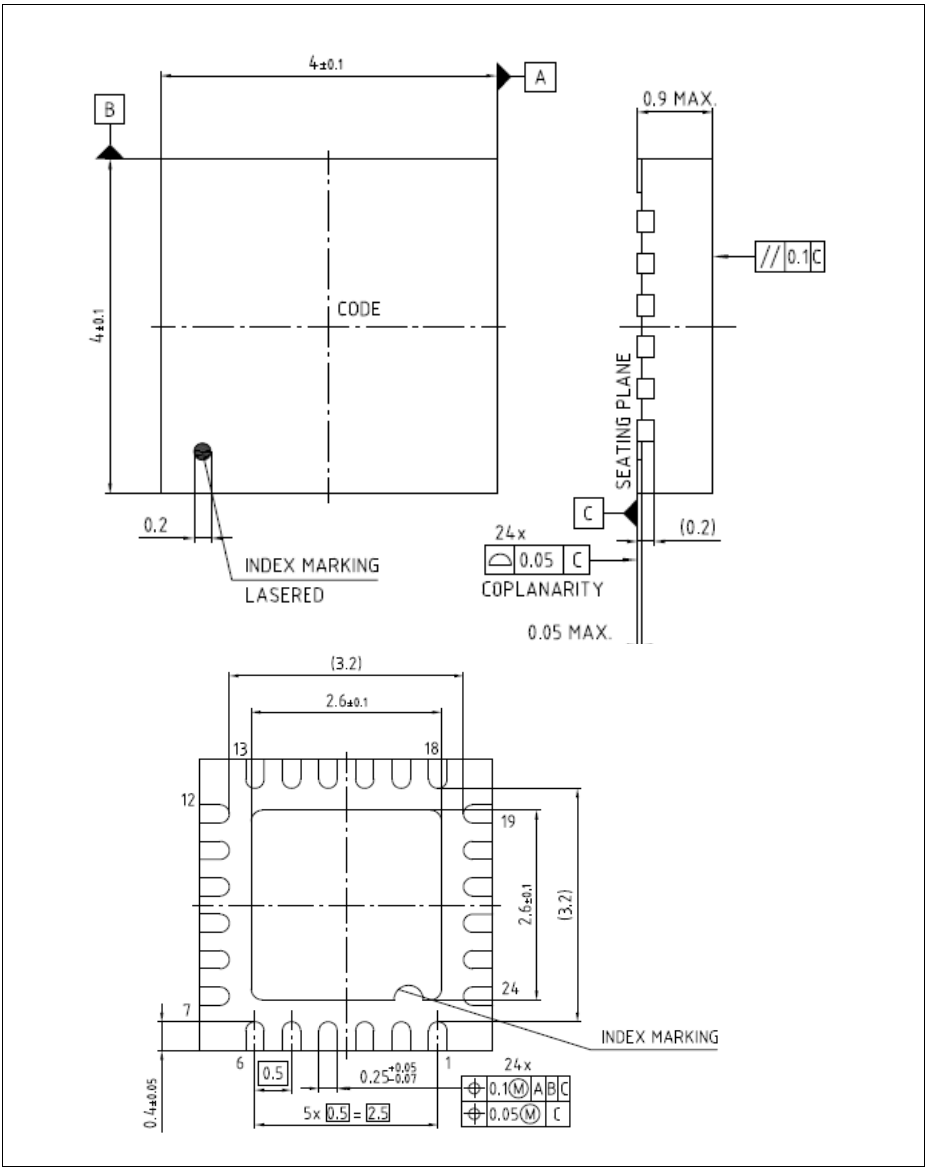


Figure 29 PG-VQFN-24-19