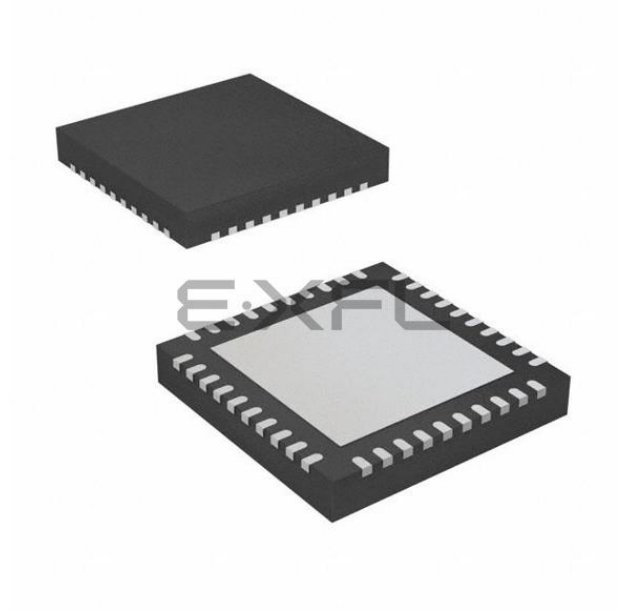
Infineon Technologies - XMC1301Q040F0008ABXUMA1 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301q040f0008abxuma1

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- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC1300 Device Types

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1301-T016F0008	PG-TSSOP-16-8	8	16
XMC1301-T016F0016	PG-TSSOP-16-8	16	16
XMC1301-T016F0032	PG-TSSOP-16-8	32	16
XMC1301-T016X0008	PG-TSSOP-16-8	8	16
XMC1301-T016X0016	PG-TSSOP-16-8	16	16
XMC1302-T016X0008	PG-TSSOP-16-8	8	16

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Table 4 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T016F0032	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T028X0016	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038X0032	00013013 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038F0064	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083$_H$	AB

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Table 4 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1302-Q040X0128	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 $201ED083_H$	AB
XMC1302-Q040X0200	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 $201ED083_H$	AB

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2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

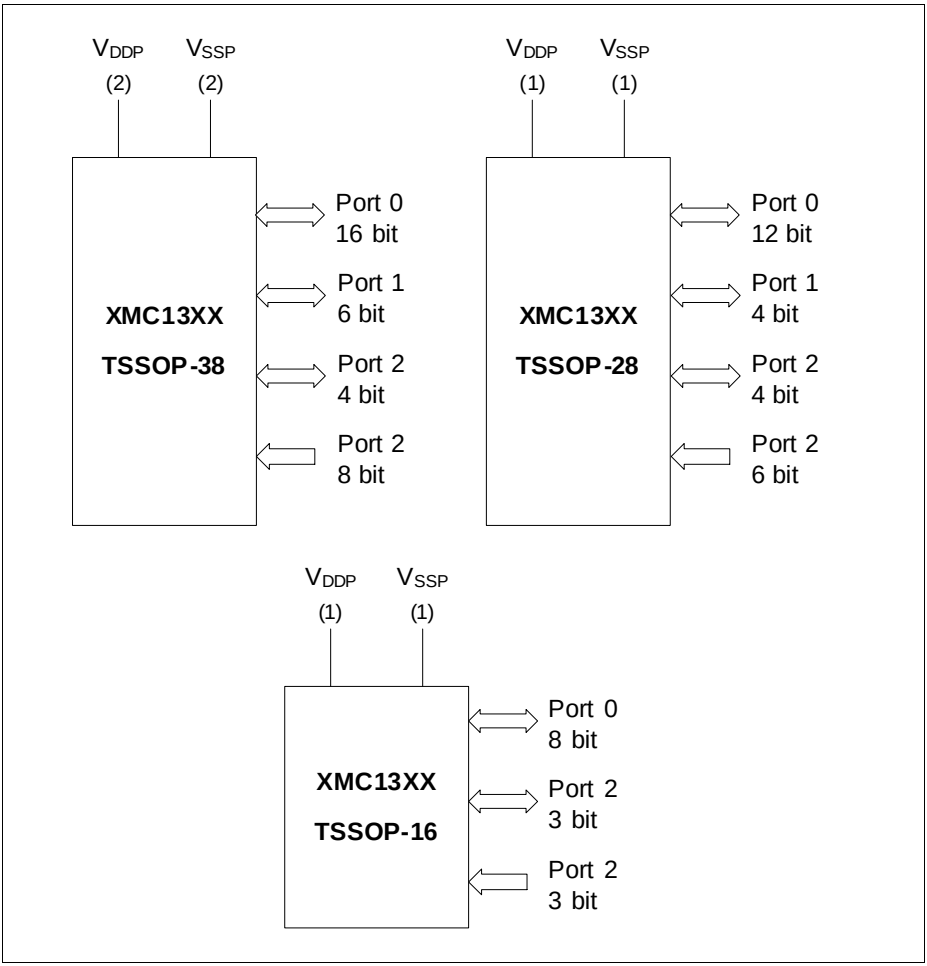

Figure 2 XMC1300 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

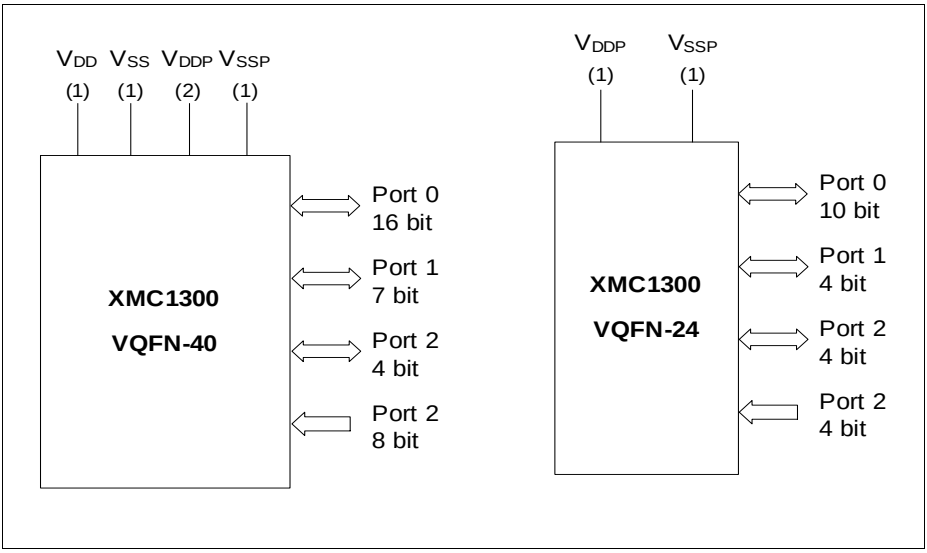

Figure 3 XMC1300 Logic Symbol for VQFN-24 and VQFN-40

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2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

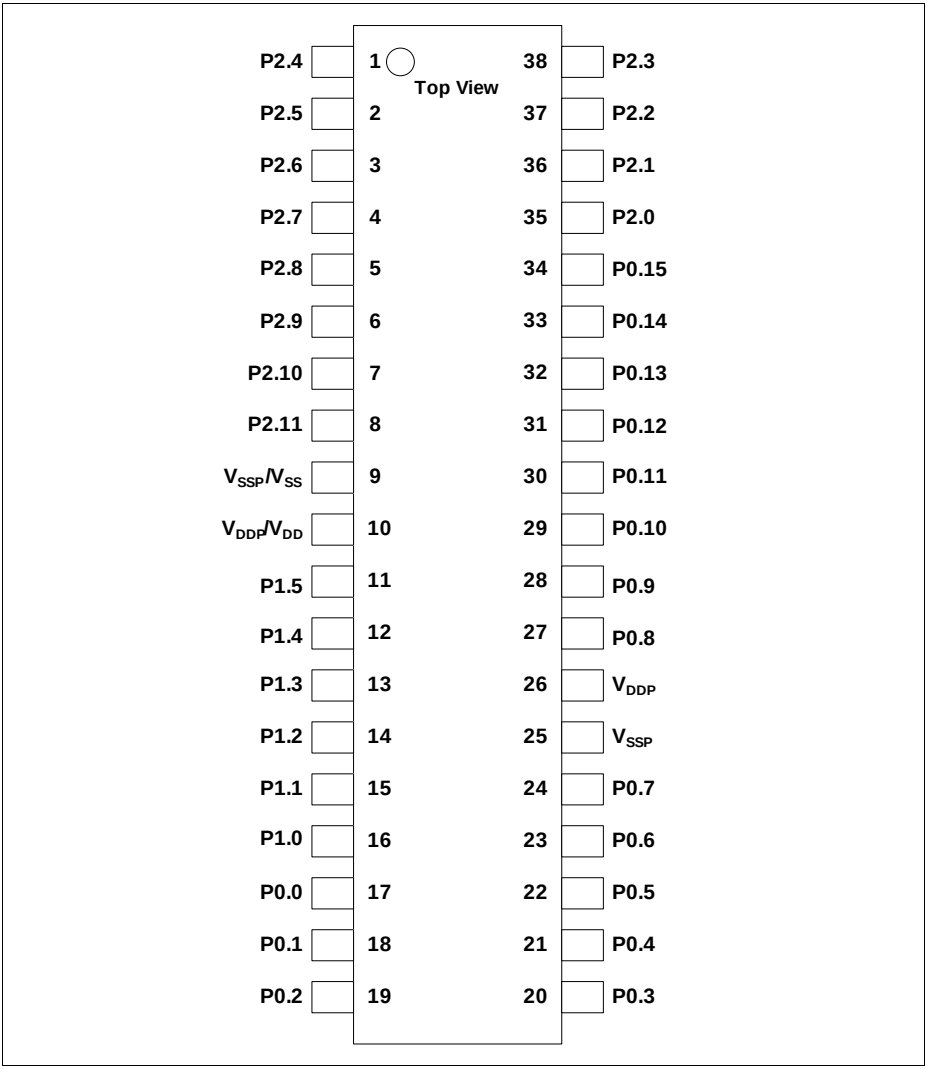

Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration (top view)

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.7	30	24	17	18	10	STD_IN OUT	
P0.8	33	27	18	19	11	STD_IN OUT	
P0.9	34	28	19	20	12	STD_IN OUT	
P0.10	35	29	20	-	-	STD_IN OUT	
P0.11	36	30	-	-	-	STD_IN OUT	
P0.12	37	31	21	21	-	STD_IN OUT	
P0.13	38	32	22	22	-	STD_IN OUT	
P0.14	39	33	23	23	13	STD_IN OUT	
P0.15	40	34	24	24	14	STD_IN OUT	
P1.0	22	16	12	14	-	High Current	
P1.1	21	15	11	13	-	High Current	
P1.2	20	14	10	12	-	High Current	
P1.3	19	13	9	11	-	High Current	
P1.4	18	12	-	-	-	High Current	
P1.5	17	11	-	-	-	High Current	
P1.6	16	-	-	-	-	STD_IN OUT	
P2.0	1	35	25	1	15	STD_IN OUT/AN	

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3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV}	SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS}	SR	–	–	25	mA	

Figure 10 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)[1)]

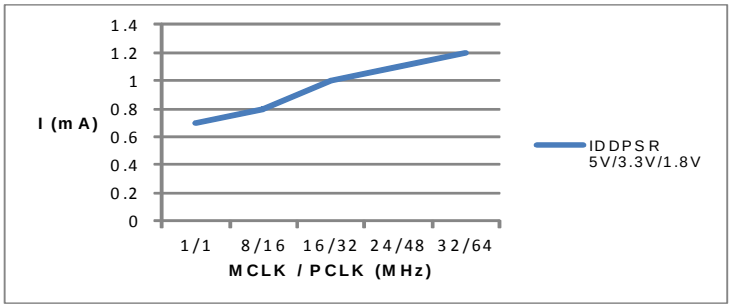
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B CALCTR.CALGNSTC = $0C_H$
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground	V_{REFGND} SR	V_{SSP} - 0.05	–	1.0	V	G0CH0
		V_{SSP} - 0.05	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	

Table 21 Power Supply Parameters; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	1.8	-	mA	32 / 64
			1.7	-	mA	24 / 48
			1.6	-	mA	16 / 32
			1.5	-	mA	8 / 16
			1.4	-	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	1.2	-	mA	32 / 64
			1.1	-	mA	24 / 48
			1.0	-	mA	16 / 32
			0.8	-	mA	8 / 16
			0.7	-	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.24	-	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	-	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	280	-	µsec	

1) The typical values are measured at T_A = + 25 °C and VDDP = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Figure 15 shows typical graphs for sleep mode current for V_{DDP} = 5V, V_{DDP} = 3.3V, V_{DDP} = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSR} over supply voltage V_{DDP} for different clock frequencies

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page / sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	1.3	2		f_{MCLK} = 32 MHz
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{FWSFLASH}$ SR	0	0	1		NVM_CONFIG1.FIXWS = 1_B, $f_{MCLK} \leq$ 16 MHz
		1	1	1		NVM_CONFIG1.FIXWS = 1_B, 16 MHz < $f_{MCLK} \leq$ 32 MHz
Erase Cycles	N_{ECYC} CC	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.2 Power-Up and Supply Monitoring Characteristics

Table 24 provides the characteristics of the power-up and supply monitoring in XMC1300.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

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3.3.6 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 29 USIC SSC Master Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK}	CC	62.5	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1	CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2	CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3	CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4	SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5	SR	0	–	–	ns	

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Table 30 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	125	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11}	SR	10	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1)]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1)]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

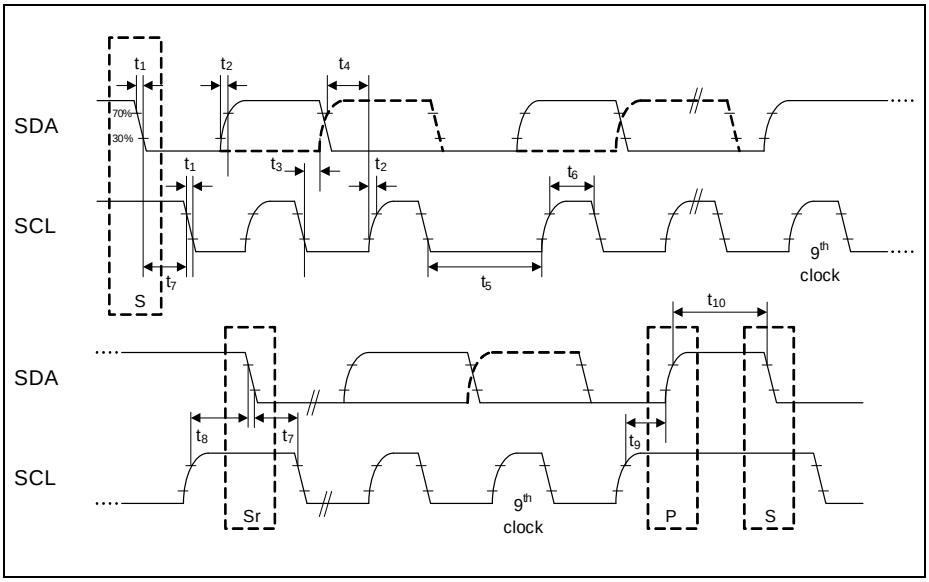

Figure 23 USIC IIC Stand and Fast Mode Timing

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 33 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	-	-	ns	$V_{DDP} \geq 3$ V
		$4/f_{MCLK}$	-	-	ns	$V_{DDP} < 3$ V
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

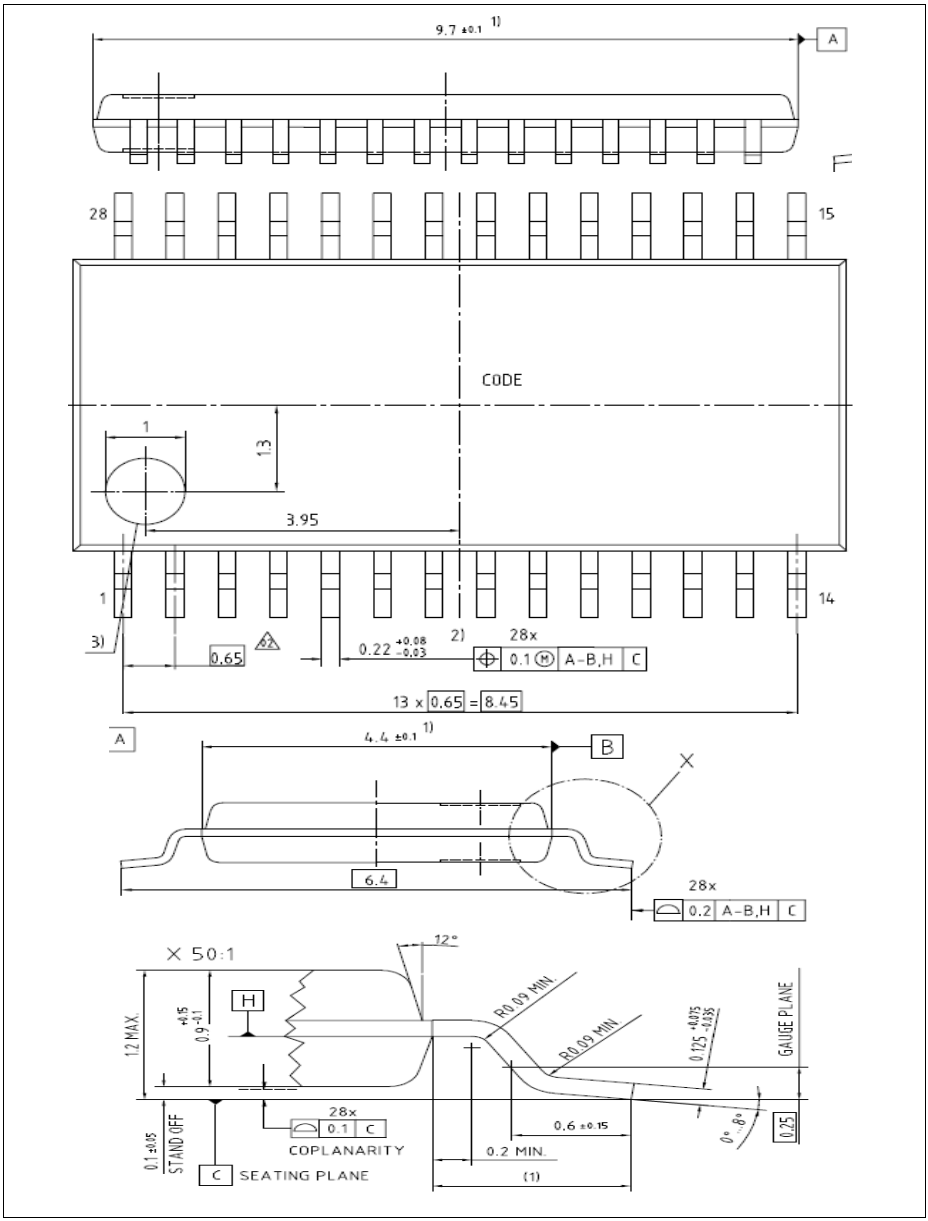

Figure 27 PG-TSSOP-28-16

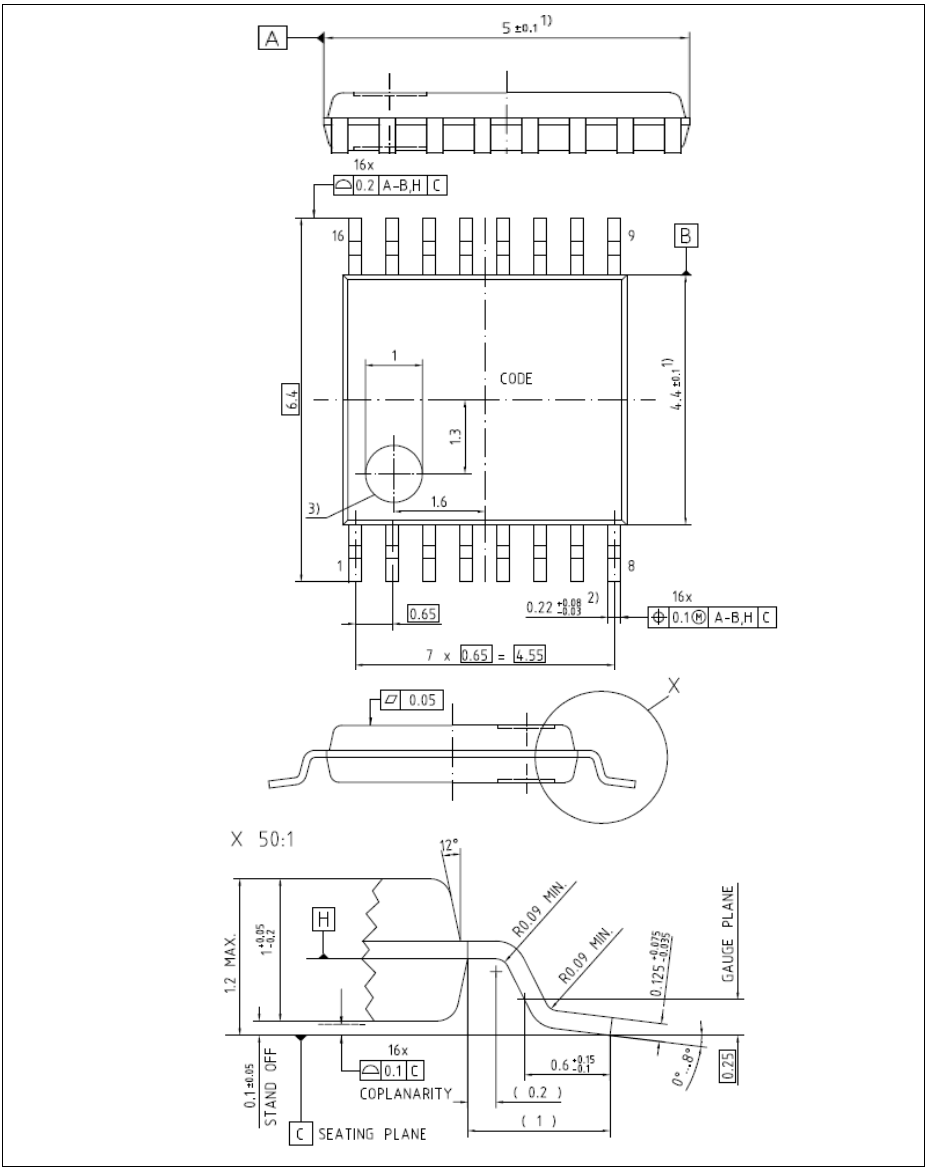

Figure 28 PG-TSSOP-16-8

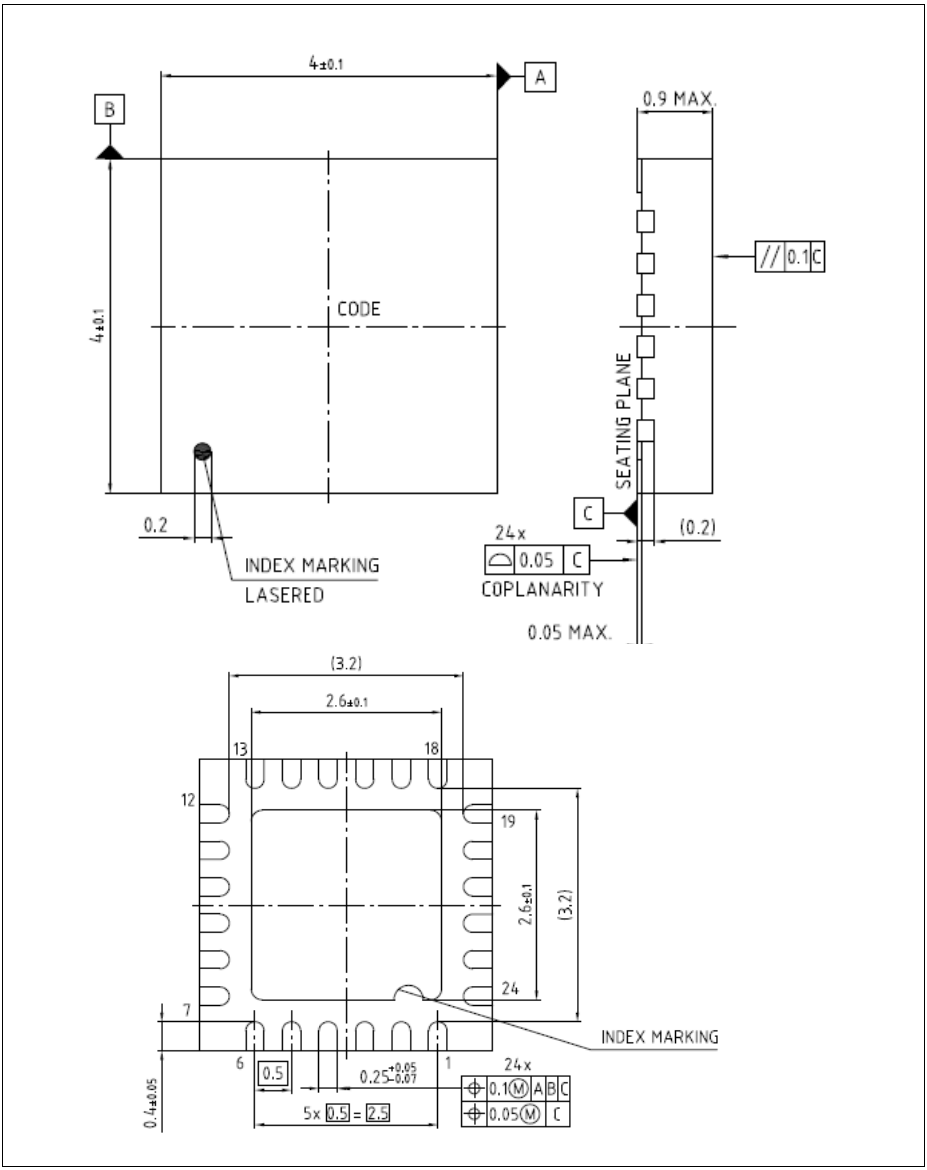

Figure 29 PG-VQFN-24-19