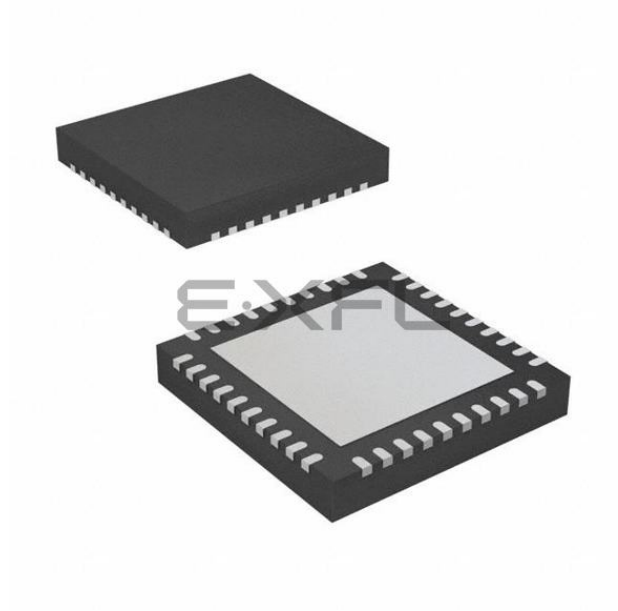
Infineon Technologies - XMC1301Q040F0032ABXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301q040f0032abxuma1

XMC1300 Data Sheet

Revision History: V1.9 2017-03

Previous Version: V1.8 2016-09	
Page	Subjects
Page 10, **Page 12**	Add marking option for XMC1301-T038X0032.

Trademarks

C166™, TriCore™, XMC™ and DAVE™ are trademarks of Infineon Technologies AG.

ARM®, ARM Powered® and AMBA® are registered trademarks of ARM, Limited.

Cortex™, CoreSight™, ETM™, Embedded Trace Macrocell™ and Embedded Trace Buffer™ are trademarks of ARM, Limited.

We Listen to Your Comments

Is there any information in this document that you feel is wrong, unclear or missing? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Table of Contents

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1300 series devices.

The document describes the characteristics of a superset of the XMC1300 series devices. For simplicity, the various device types are referred to by the collective term XMC1300 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

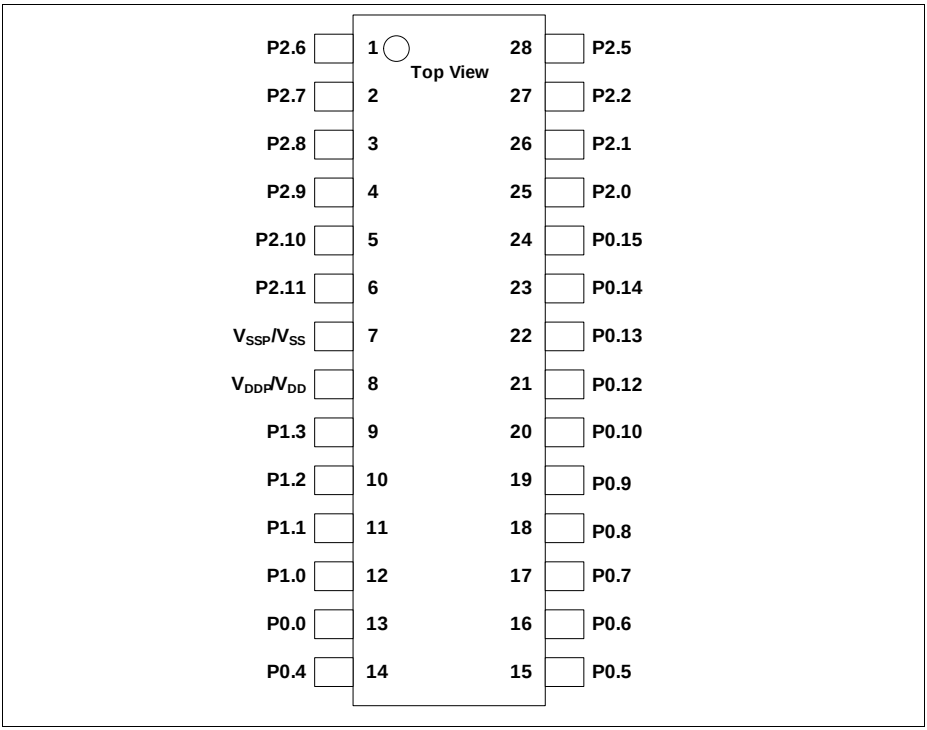


Figure 5 XMC1300 PG-TSSOP-28 Pin Configuration (top view)

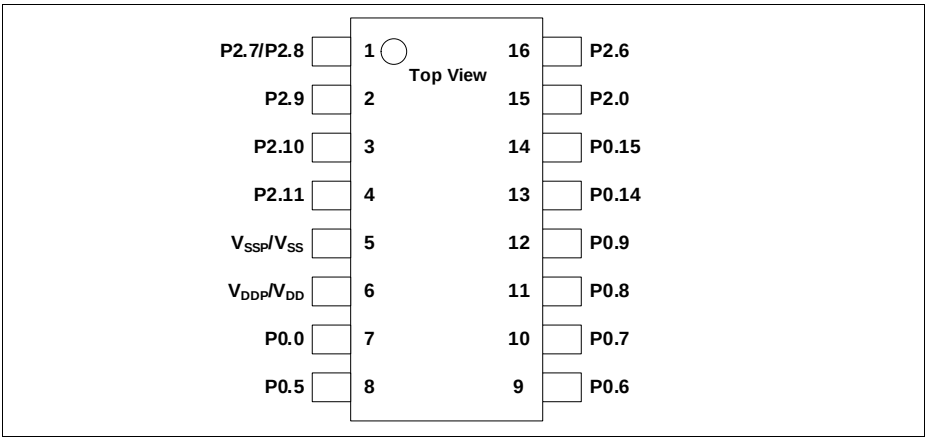


Figure 6 XMC1300 PG-TSSOP-16 Pin Configuration (top view)

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT(standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_INOUT	
P0.1	24	18	-	-	-	STD_INOUT	
P0.2	25	19	-	-	-	STD_INOUT	
P0.3	26	20	-	-	-	STD_INOUT	
P0.4	27	21	14	-	-	STD_INOUT	
P0.5	28	22	15	16	8	STD_INOUT	
P0.6	29	23	16	17	9	STD_INOUT	

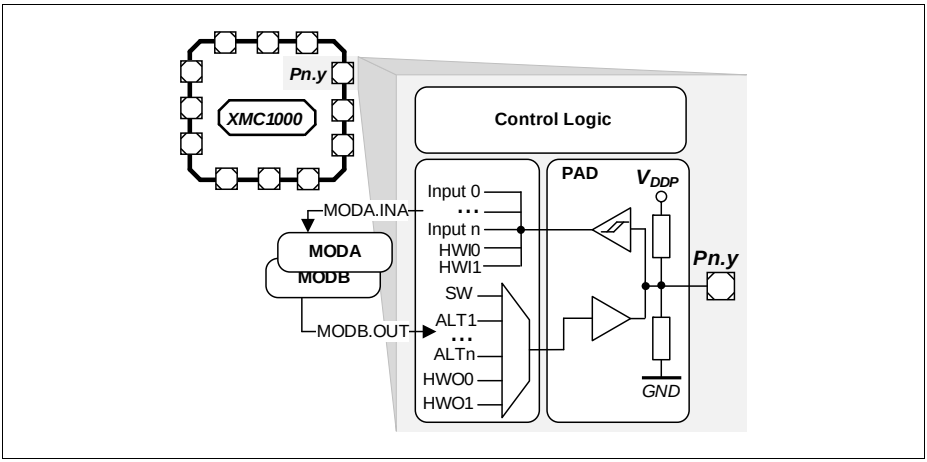


Figure 9 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the **Port I/O Functions** table for the complete Port I/O function mapping.

Table 9 Port I/O Functions (cont'd)

Function	Outputs							Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.14	BCCU0.OUT7				CCU80.OUT31	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT			POSIF0.IN1B		USIC0_CH0.DX0A	USIC0_CH0.DX1A				
P0.15	BCCU0.OUT8				CCU80.OUT30	USIC0_CH0.DOUT0	USIC0_CH1.MCLKOUT			POSIF0.IN2B		USIC0_CH0.DX0B					
P1.0	BCCU0.OUT0	CCU40.OUT0			CCU80.OUT00	ACMP1.OUT	USIC0_CH0.DOUT0			POSIF0.IN2A		USIC0_CH0.DX0C					
P1.1	VADC0.EMUX00	CCU40.OUT1			CCU80.OUT01	USIC0_CH0.DOUT0	USIC0_CH1.SELO0			POSIF0.IN1A		USIC0_CH0.DX0D	USIC0_CH0.DX1D	USIC0_CH1.DX2E			
P1.2	VADC0.EMUX01	CCU40.OUT2			CCU80.OUT10	ACMP2.OUT	USIC0_CH1.DOUT0			POSIF0.IN0A		USIC0_CH1.DX0B					
P1.3	VADC0.EMUX02	CCU40.OUT3			CCU80.OUT11	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0					USIC0_CH1.DX0A	USIC0_CH1.DX1A				
P1.4	VADC0.EMUX10	USIC0_CH1.SCLKOUT			CCU80.OUT20	USIC0_CH0.SELO0	USIC0_CH1.SELO1					USIC0_CH0.DX5E	USIC0_CH1.DX5E				
P1.5	VADC0.EMUX11	USIC0_CH0.DOUT0		BCCU0.OUT1	CCU80.OUT21	USIC0_CH0.SELO1	USIC0_CH1.SELO2					USIC0_CH1.DX5F					
P1.6	VADC0.EMUX12	USIC0_CH1.DOUT0		USIC0_CH0.SCLKOUT	BCCU0.OUT2	USIC0_CH0.SELO2	USIC0_CH1.SELO3			USIC0_CH0.DX5F							
P2.0	ERU0.PDOUT3	CCU40.OUT0	ERU0.GOUT3		CCU80.OUT20	USIC0_CH0.DOUT0	USIC0_CH0.SCLKOUT		VADC0.G0CH5		ERU0.0B0	USIC0_CH0.DX0E	USIC0_CH0.DX1E	USIC0_CH1.DX2F			
P2.1	ERU0.PDOUT2	CCU40.OUT1	ERU0.GOUT2		CCU80.OUT21	USIC0_CH0.DOUT0	USIC0_CH1.SCLKOUT	ACMP2.INP	VADC0.G0CH6		ERU0.1B0	USIC0_CH0.DX0F	USIC0_CH1.DX3A	USIC0_CH1.DX4A			
P2.2								ACMP2.INN	VADC0.G0CH7		ERU0.0B1	USIC0_CH0.DX3A	USIC0_CH0.DX4A	USIC0_CH1.DX5A	ORC0.AIN		
P2.3									VADC0.G1CH5		ERU0.1B1	USIC0_CH0.DX5B	USIC0_CH1.DX3C	USIC0_CH1.DX4C	ORC1.AIN		
P2.4									VADC0.G1CH6		ERU0.0A1	USIC0_CH0.DX3B	USIC0_CH0.DX4B	USIC0_CH1.DX5B	ORC2.AIN		
P2.5									VADC0.G1CH7		ERU0.1A1	USIC0_CH0.DX5D	USIC0_CH1.DX3E	USIC0_CH1.DX4E	ORC3.AIN		

3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15 Operating Conditions Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient Temperature	T_A	SR	-40	–	85	°C	Temp. Range F
			-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP}	SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK}	CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK}	CC	–	–	66.4	MHz	Peripherals clock
Short circuit current of digital outputs	I_{SC}	SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D}	SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, **Chapter 3.3.2**.

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1300.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

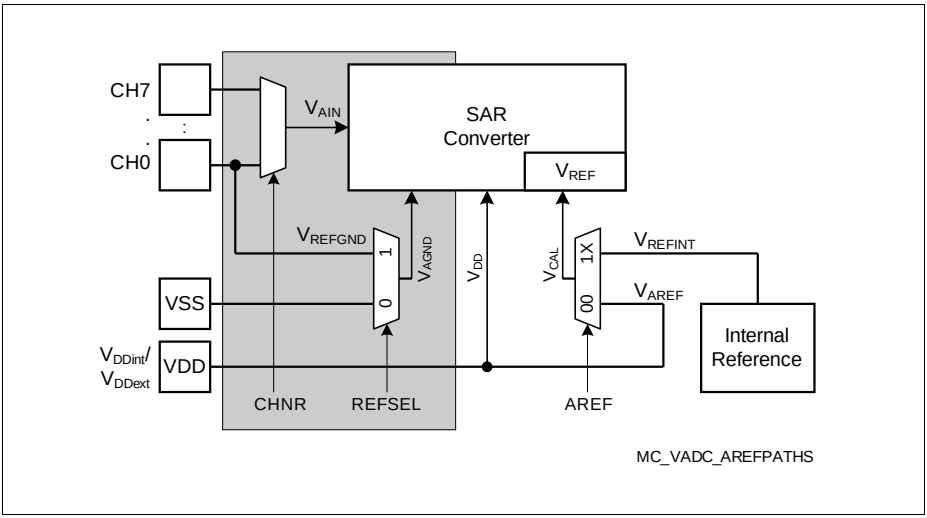


Figure 11 ADC Voltage Supply

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

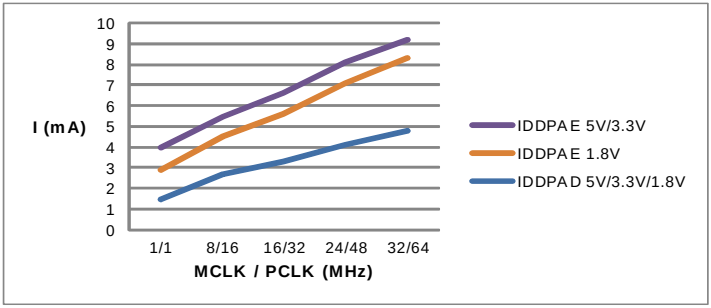
Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
			–	+/-20	–	mV	Low power mode ΔV_{CMP} < 200 mV
Propagation Delay[1)]	t_{PDELAY}	CC	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
			–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
			–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
			–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current Consumption	I_{ACMP}	CC	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	10	–	µA	First active ACMP in low power mode
			–	6	–	µA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	–	+/-15	–	mV	
Filter Delay[1)]	t_{FDELAY}	CC	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

Figure 14 shows typical graphs for active mode supply current for V_{DDP} = 5V, V_{DDP} = 3.3V, V_{DDP} = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 14 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page / sector	t_{ERASE} CC	6.8	7.1	7.6	ms	
Program time per block	t_{PSER} CC	102	152	204	µs	
Wake-Up time	t_{WU} CC	–	32.2	–	µs	
Read time per word	t_a CC	–	50	–	ns	
Data Retention Time	t_{RET} CC	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States [1]	$N_{WSFLASH}$ CC	0	0	0		f_{MCLK} = 8 MHz
		0	1	1		f_{MCLK} = 16 MHz
		1	1.3	2		f_{MCLK} = 32 MHz
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{FWSFLASH}$ SR	0	0	1		NVM_CONFIG1.FIXWS = 1_B, $f_{MCLK} \leq$ 16 MHz
		1	1	1		NVM_CONFIG1.FIXWS = 1_B, 16 MHz < $f_{MCLK} \leq$ 32 MHz
Erase Cycles	N_{ECYC} CC	–	–	$5*10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	N_{TECYC} CC	–	–	$2*10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.2 Power-Up and Supply Monitoring Characteristics

Table 24 provides the characteristics of the power-up and supply monitoring in XMC1300.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 31 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

Table 32 USIC IIC Fast Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1*C_b [2)]	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1*C_b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

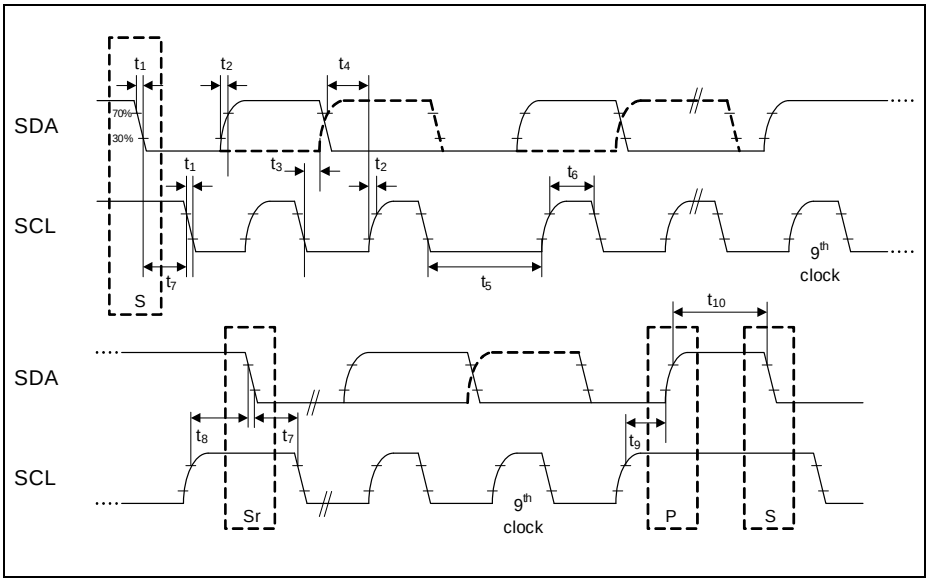


Figure 23 USIC IIC Stand and Fast Mode Timing

3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

Note: Operating Conditions apply.

Table 33 USIC IIS Master Transmitter Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_1 CC	$2/f_{MCLK}$	-	-	ns	$V_{DDP} \geq 3$ V
		$4/f_{MCLK}$	-	-	ns	$V_{DDP} < 3$ V
Clock HIGH	t_2 CC	0.35 x t_{1min}	-	-	ns	
Clock Low	t_3 CC	0.35 x t_{1min}	-	-	ns	
Hold time	t_4 CC	0	-	-	ns	
Clock rise time	t_5 CC	-	-	0.15 x t_{1min}	ns	

4 Package and Reliability

The XMC1300 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

4.1 Package Parameters

Table 35 provides the thermal characteristics of the packages used in XMC1300.

Table 35 Thermal Characteristics of the Packages

Parameter	Symbol	Limit Values		Unit	Package Types
		Min.	Max.		
Exposed Die Pad Dimensions	Ex × Ey CC	-	2.7 × 2.7	mm	PG-VQFN-24-19
		-	3.7 × 3.7	mm	PG-VQFN-40-13
Thermal resistance Junction-Ambient	$R_{\Theta JA}$ CC	-	104.6	K/W	PG-TSSOP-16-8[1)]
		-	83.2	K/W	PG-TSSOP-28-16[1)]
		-	70.3	K/W	PG-TSSOP-38-9[1)]
		-	46.0	K/W	PG-VQFN-24-19[1)]
		-	38.4	K/W	PG-VQFN-40-13[1)]

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

Note: For electrical reasons, it is required to connect the exposed pad to the board ground V_{SSP}, independent of EMC and thermal requirements.

4.1.1 Thermal Considerations

When operating the XMC1300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

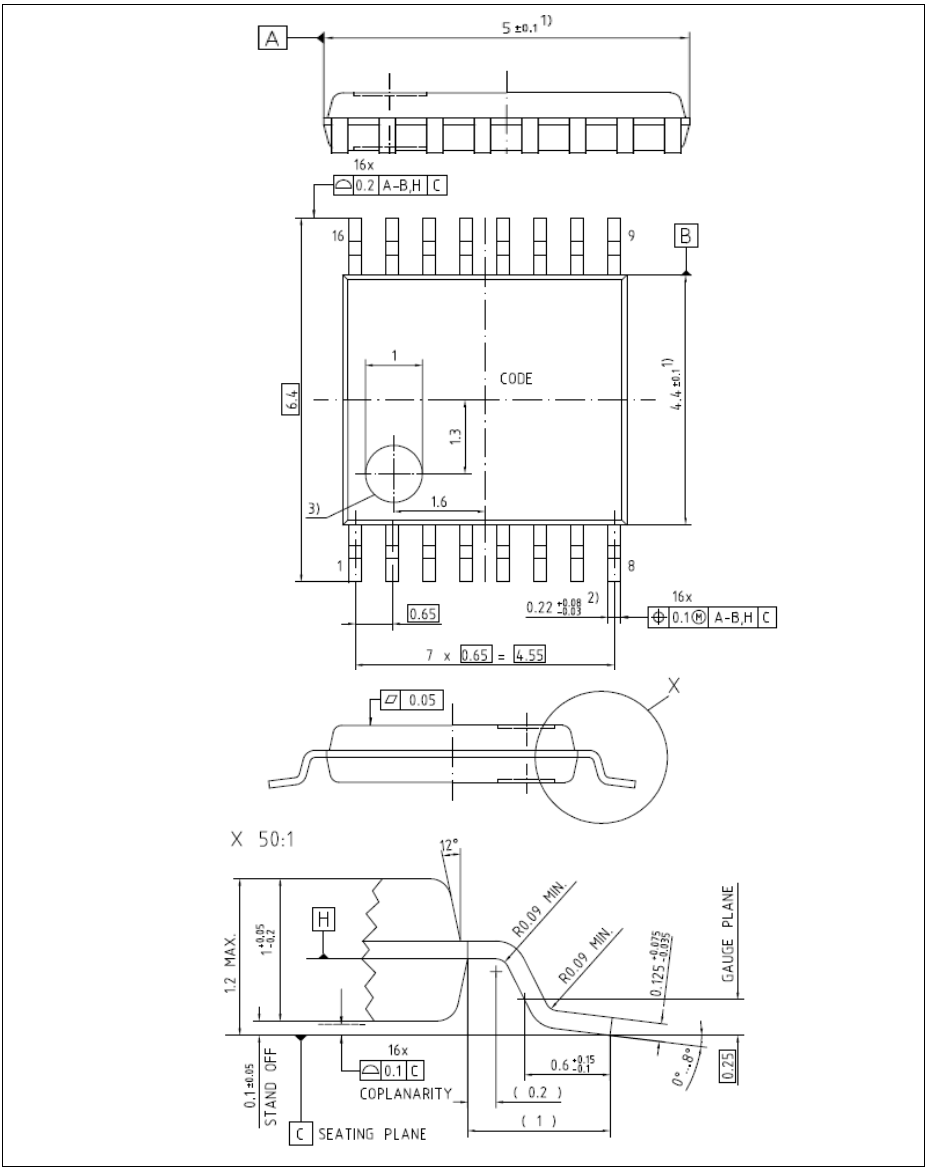


Figure 28 PG-TSSOP-16-8

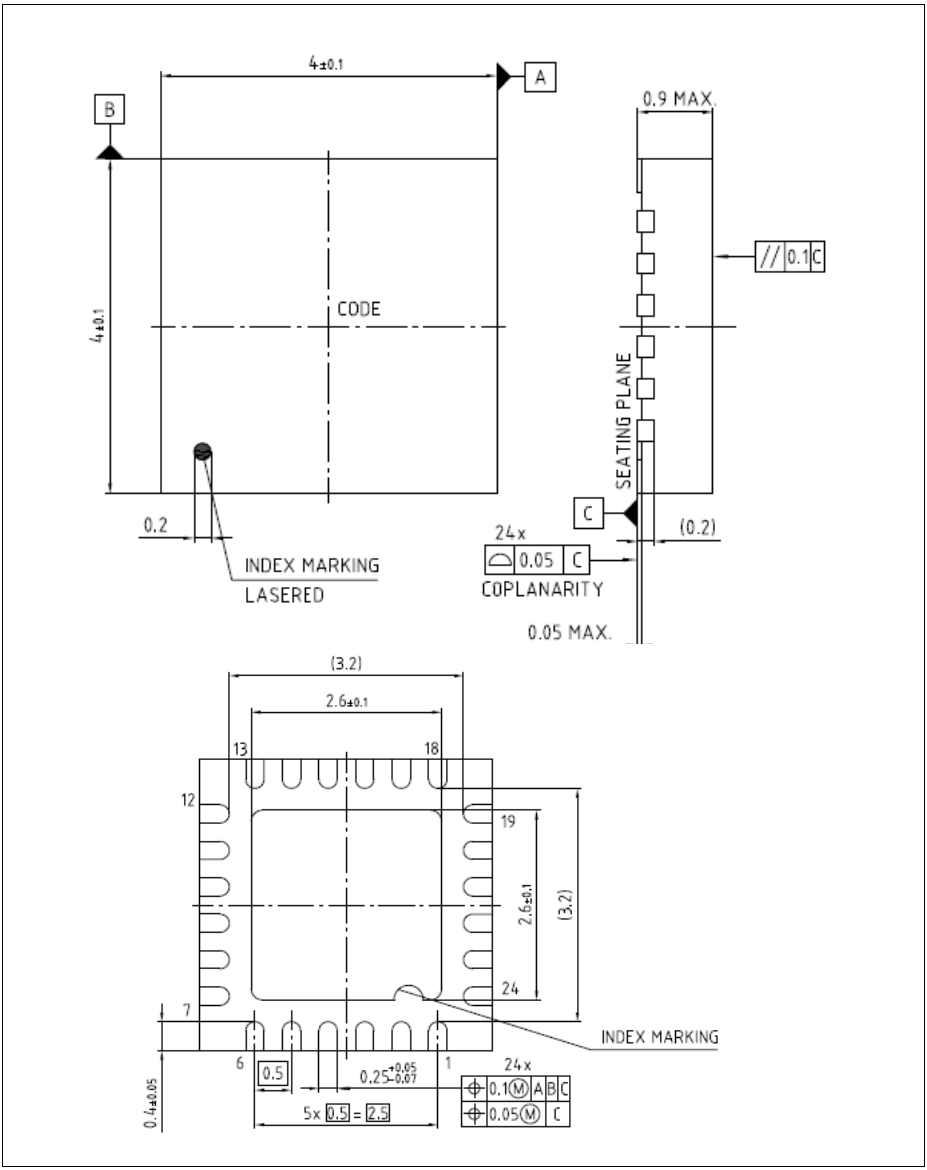


Figure 29 PG-VQFN-24-19