Infineon Technologies - XMC1301T016F0016ABXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	11
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 11x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-16-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t016f0016abxuma1

XMC1300 AB-Step

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

Data Sheet

V1.9 2017-03

Microcontrollers

XMC1300 Data Sheet

Revision History: V1.9 2017-03

Previous Version: V1.8 2016-09	
Page	Subjects
Page 10, **Page 12**	Add marking option for XMC1301-T038X0032.

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1 Summary of Features

The XMC1300 devices are members of the XMC1000 Family of microcontrollers based on the ARM Cortex-M0 processor core. The XMC1300 series addresses the real-time control needs of motor control, digital power conversion. It also features peripherals for LED Lighting applications.

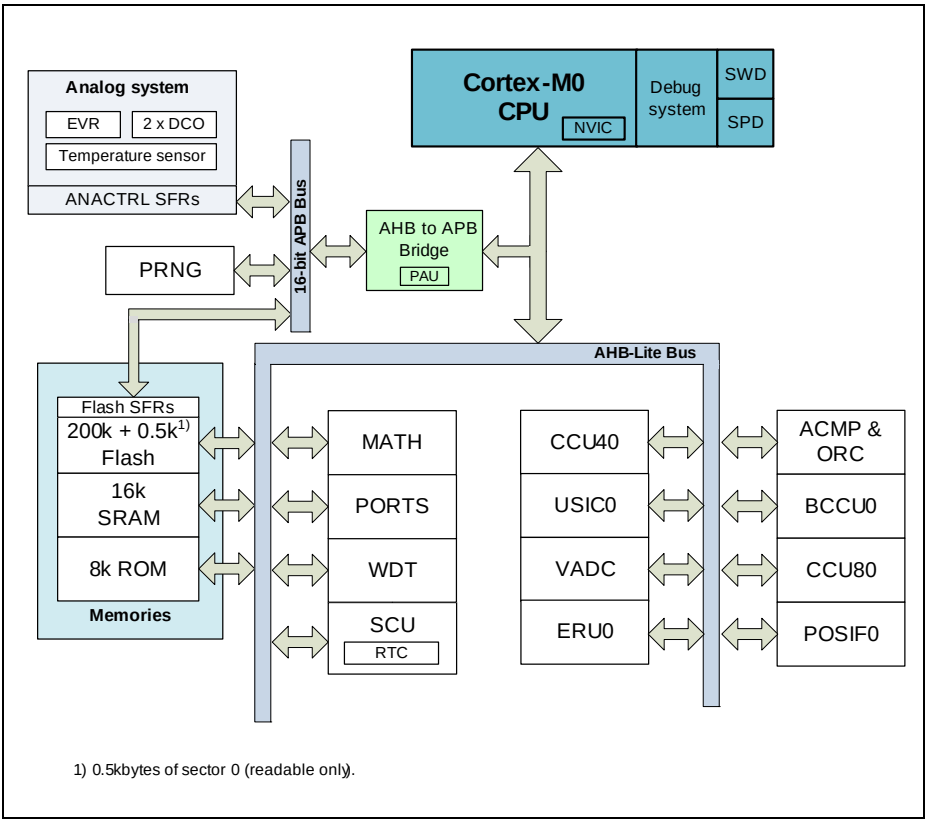


Figure 1 System Block Diagram

CPU Subsystem

- CPU Core
  - High-performance 32-bit ARM Cortex-M0 CPU
  - Most 16-bit Thumb and subset of 32-bit Thumb2 instruction set
  - Single cycle 32-bit hardware multiplier
  - System timer (SysTick) for Operating System support

- Configurable pad hysteresis

On-Chip Debug Support

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

Table 1 Synopsis of XMC1300 Device Types

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1301-T016F0008	PG-TSSOP-16-8	8	16
XMC1301-T016F0016	PG-TSSOP-16-8	16	16
XMC1301-T016F0032	PG-TSSOP-16-8	32	16
XMC1301-T016X0008	PG-TSSOP-16-8	8	16
XMC1301-T016X0016	PG-TSSOP-16-8	16	16
XMC1302-T016X0008	PG-TSSOP-16-8	8	16

Table 1 Synopsis of XMC1300 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1302-T016X0016	PG-TSSOP-16-8	16	16
XMC1302-T016X0032	PG-TSSOP-16-8	32	16
XMC1302-T028X0016	PG-TSSOP-28-8	16	16
XMC1301-T038F0008	PG-TSSOP-38-9	8	16
XMC1301-T038F0016	PG-TSSOP-38-9	16	16
XMC1301-T038F0032	PG-TSSOP-38-9	32	16
XMC1301-T038X0032	PG-TSSOP-38-9	32	16
XMC1301-T038F0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0016	PG-TSSOP-38-9	16	16
XMC1302-T038X0032	PG-TSSOP-38-9	32	16
XMC1302-T038X0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0128	PG-TSSOP-38-9	128	16
XMC1302-T038X0200	PG-TSSOP-38-9	200	16
XMC1301-Q024F0008	PG-VQFN-24-19	8	16
XMC1301-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0032	PG-VQFN-24-19	32	16
XMC1302-Q024F0064	PG-VQFN-24-19	64	16
XMC1302-Q024X0016	PG-VQFN-24-19	16	16
XMC1302-Q024X0032	PG-VQFN-24-19	32	16
XMC1302-Q024X0064	PG-VQFN-24-19	64	16
XMC1301-Q040F0008	PG-VQFN-40-13	8	16
XMC1301-Q040F0016	PG-VQFN-40-13	16	16
XMC1301-Q040F0032	PG-VQFN-40-13	32	16
XMC1302-Q040X0016	PG-VQFN-40-13	16	16
XMC1302-Q040X0032	PG-VQFN-40-13	32	16
XMC1302-Q040X0064	PG-VQFN-40-13	64	16
XMC1302-Q040X0128	PG-VQFN-40-13	128	16
XMC1302-Q040X0200	PG-VQFN-40-13	200	16

1.3 Device Type Features

The following table lists the available features per device type.

Table 2 Features of XMC1300 Device Types[1)]

Derivative	ADC channel	ACMP	BCCU	MATH
XMC1301-T016	11	2	-	-
XMC1302-T016	11	2	1	1
XMC1302-T028	14	3	1	1
XMC1301-T038	16	3	-	-
XMC1302-T038	16	3	1	1
XMC1301-Q024	13	3	-	-
XMC1302-Q024	13	3	1	1
XMC1301-Q040	16	3	-	-
XMC1302-Q040	16	3	1	1

1) Features that are not included in this table are available in all the derivatives

Table 3 ADC Channels [1)]

Package	VADC0 G0	VADC0 G1
PG-TSSOP-16	CH0..CH5	CH0..CH4
PG-TSSOP-28	CH0..CH7	CH0 .. CH4, CH7
PG-TSSOP-38	CH0..CH7	CH0..CH7
PG-VQFN-24	CH0..CH7	CH0..CH4
PG-VQFN-40	CH0..CH7	CH0..CH7

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.7	30	24	17	18	10	STD_IN OUT	
P0.8	33	27	18	19	11	STD_IN OUT	
P0.9	34	28	19	20	12	STD_IN OUT	
P0.10	35	29	20	-	-	STD_IN OUT	
P0.11	36	30	-	-	-	STD_IN OUT	
P0.12	37	31	21	21	-	STD_IN OUT	
P0.13	38	32	22	22	-	STD_IN OUT	
P0.14	39	33	23	23	13	STD_IN OUT	
P0.15	40	34	24	24	14	STD_IN OUT	
P1.0	22	16	12	14	-	High Current	
P1.1	21	15	11	13	-	High Current	
P1.2	20	14	10	12	-	High Current	
P1.3	19	13	9	11	-	High Current	
P1.4	18	12	-	-	-	High Current	
P1.5	17	11	-	-	-	High Current	
P1.6	16	-	-	-	-	STD_IN OUT	
P2.0	1	35	25	1	15	STD_IN OUT/AN	

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
VSSP	31	25	-	-	-	Power	I/O port ground
VDDP	32	26	-	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	-	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.2 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

Table 9 Port I/O Functions

Function	Outputs							Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0		ERU0.GOUT0	CCU40.OUT0	CCU80.OUT00	USIC0_CH0.SELO0	USIC0_CH1.SELO0	BCCU0.TRAPINB	CCU40.IN0C			USIC0_CH0.DX2A	USIC0_CH1.DX2A				
P0.1	ERU0.PDOUT1		ERU0.GOUT1	CCU40.OUT1	CCU80.OUT01	BCCU0.OUT8	SCU.VDROP		CCU40.IN1C								
P0.2	ERU0.PDOUT2		ERU0.GOUT2	CCU40.OUT2	CCU80.OUT02	VADC0.EMUX02	CCU80.OUT10		CCU40.IN2C								
P0.3	ERU0.PDOUT3		ERU0.GOUT3	CCU40.OUT3	CCU80.OUT03	VADC0.EMUX01	CCU80.OUT11		CCU40.IN3C								
P0.4	BCCU0.OUT0			CCU40.OUT1	CCU80.OUT13	VADC0.EMUX00	WWDT.SERVICE_OUT		CCU80.IN0B								
P0.5	BCCU0.OUT1			CCU40.OUT0	CCU80.OUT12	ACMP2.OUT	CCU80.OUT01		CCU80.IN1B								
P0.6	BCCU0.OUT2			CCU40.OUT0	CCU80.OUT11	USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0		CCU40.IN0B			USIC0_CH1.DX0C					
P0.7	BCCU0.OUT3			CCU40.OUT1	CCU80.OUT10	USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0		CCU40.IN1B			USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C			
P0.8	BCCU0.OUT4			CCU40.OUT2	CCU80.OUT20	USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT		CCU40.IN2B			USIC0_CH0.DX1B	USIC0_CH1.DX1B				
P0.9	BCCU0.OUT5			CCU40.OUT3	CCU80.OUT21	USIC0_CH0.SELO0	USIC0_CH1.SELO0		CCU40.IN3B			USIC0_CH0.DX2B	USIC0_CH1.DX2B				
P0.10	BCCU0.OUT6			ACMP0.OUT	CCU80.OUT22	USIC0_CH0.SELO1	USIC0_CH1.SELO1		CCU80.IN2B			USIC0_CH0.DX2C	USIC0_CH1.DX2C				
P0.11	BCCU0.OUT7			USIC0_CH0.MCLKOUT	CCU80.OUT23	USIC0_CH0.SELO2	USIC0_CH1.SELO2					USIC0_CH0.DX2D	USIC0_CH1.DX2D				
P0.12	BCCU0.OUT6				CCU80.OUT33	USIC0_CH0.SELO3	CCU80.OUT20	BCCU0.TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A	USIC0_CH0.DX2E
P0.13	WWDT.SERVICE_OUT				CCU80.OUT32	USIC0_CH0.SELO4	CCU80.OUT21		CCU80.IN3B	POSIF0.IN0B		USIC0_CH0.DX2F					

Table 10 Hardware Controlled I/O Functions (cont'd)

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P2.6					$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.7					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.8					$\overline{\text{BCCU0.OUT1}}$	BCCU0.OUT1	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.9					$\overline{\text{BCCU0.OUT7}}$	BCCU0.OUT7	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.10					$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		
P2.11					$\overline{\text{BCCU0.OUT5}}$	BCCU0.OUT5		

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_{ST}	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP} [1]	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on P2 pins with respect to V_{SSP} [2]	V_{INP2}	SR	-0.3	–	V_{DDP} + 0.3	V	–
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN}	SR	-50	–	+50	mA	–

1) Excluding port pins P2.[1,2,6,7,8,9,11].

2) Applicable to port pins P2.[1,2,6,7,8,9,11].

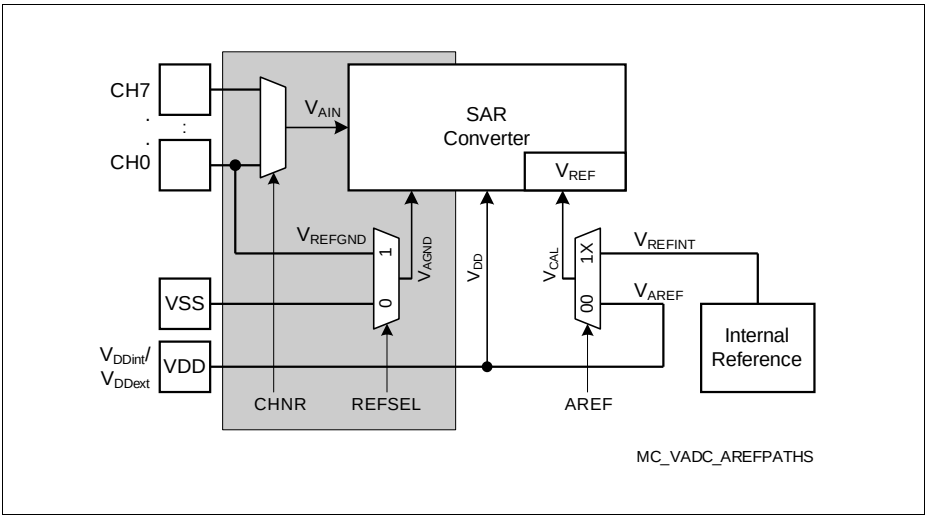


Figure 11 ADC Voltage Supply

3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

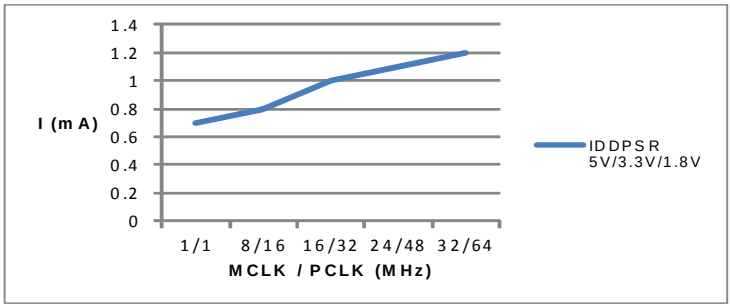
Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 Power Supply Parameters; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Active mode current Peripherals enabled f_{MCLK} / f_{PCLK} in MHz[2]	I_{DDPAE} CC	–	9.2	12	mA	32 / 64
		–	8.1	-	mA	24 / 48
		–	6.6	-	mA	16 / 32
		–	5.5	-	mA	8 / 16
		–	4	-	mA	1 / 1
Active mode current Peripherals disabled f_{MCLK} / f_{PCLK} in MHz[3]	I_{DDPAD} CC	–	4.8	-	mA	32 / 64
		–	4.1	-	mA	24 / 48
		–	3.3	-	mA	16 / 32
		–	2.7	-	mA	8 / 16
		–	1.5	-	mA	1 / 1
Active mode current Code execution from RAM Flash is powered down f_{MCLK} / f_{PCLK} in MHz	I_{DDPAR} CC	–	7.3	-	mA	32 / 64
		–	6.3	-	mA	24 / 48
		–	5.2	-	mA	16 / 32
		–	4.2	-	mA	8 / 16
		–	3.3	-	mA	1 / 1
Sleep mode current Peripherals clock enabled f_{MCLK} / f_{PCLK} in MHz[4]	I_{DDPSE} CC	–	6.6	-	mA	32 / 64
			5.8	-	mA	24 / 48
			5.1	-	mA	16 / 32
			4.4	-	mA	8 / 16
			3.7	-	mA	1 / 1

Figure 15 shows typical graphs for sleep mode current for V_{DDP} = 5V, V_{DDP} = 3.3V, V_{DDP} = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down: Supply current I_{DDPSR} over supply voltage V_{DDP} for different clock frequencies

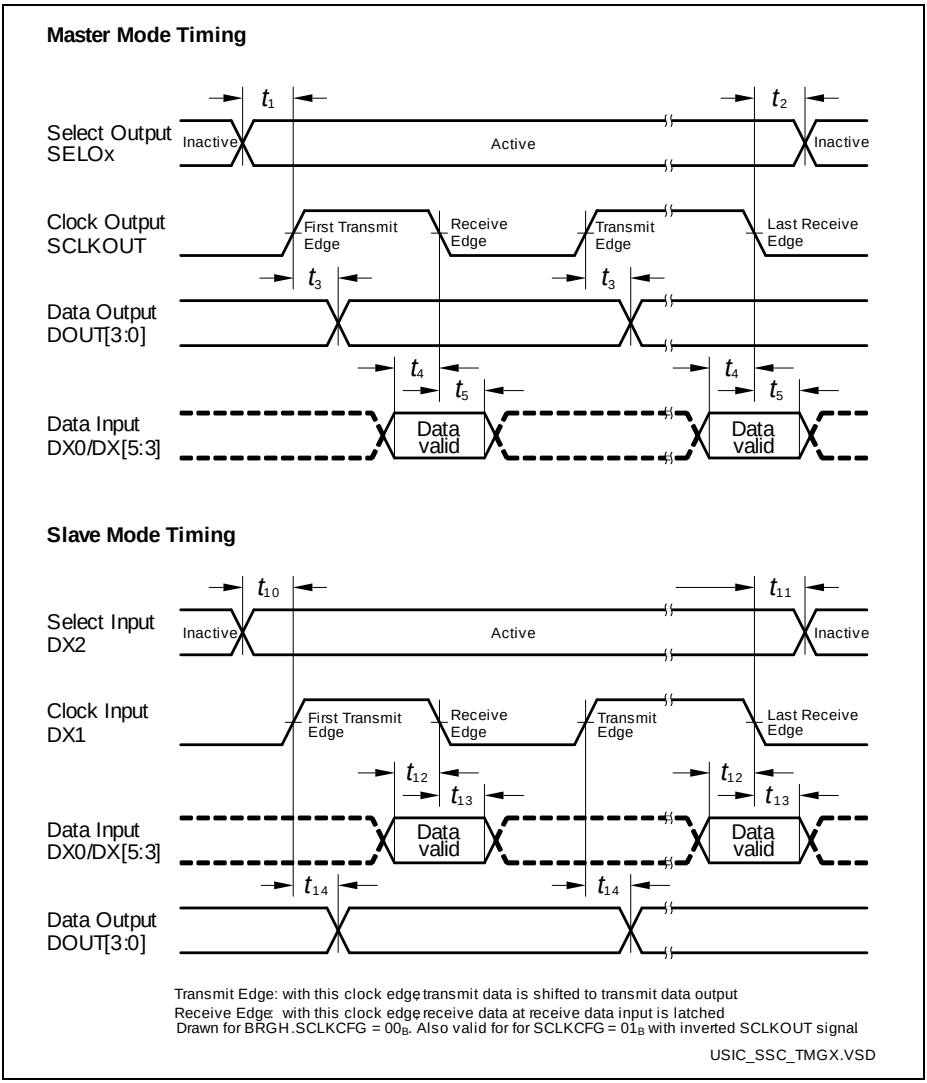


Figure 22 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

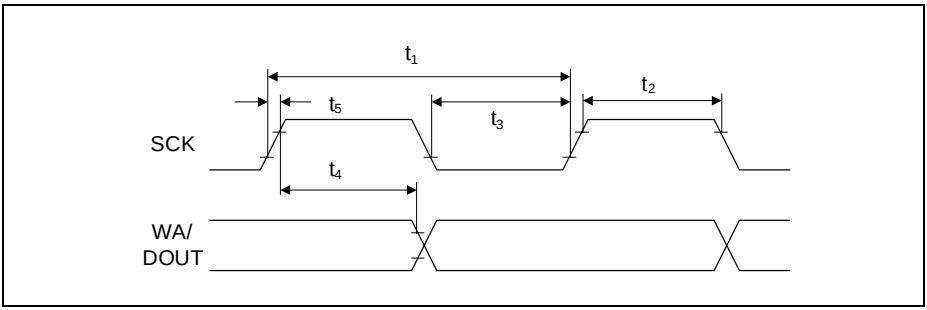


Figure 24 USIC IIS Master Transmitter Timing

Table 34 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	$4/f_{MCLK}$	-	-	ns	
Clock HIGH	t7 SR	0.35 x t_{6min}	-	-	ns	
Clock Low	t8 SR	0.35 x $t_6$min	-	-	ns	
Set-up time	t9 SR	0.2 x $t_6$min	-	-	ns	
Hold time	t10 SR	10	-	-	ns	

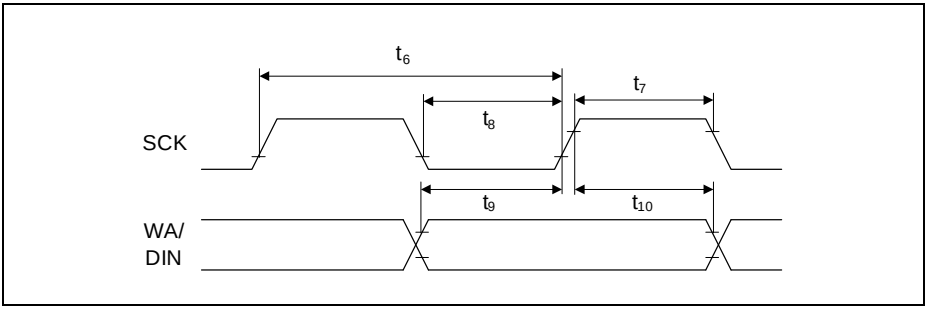


Figure 25 USIC IIS Slave Receiver Timing

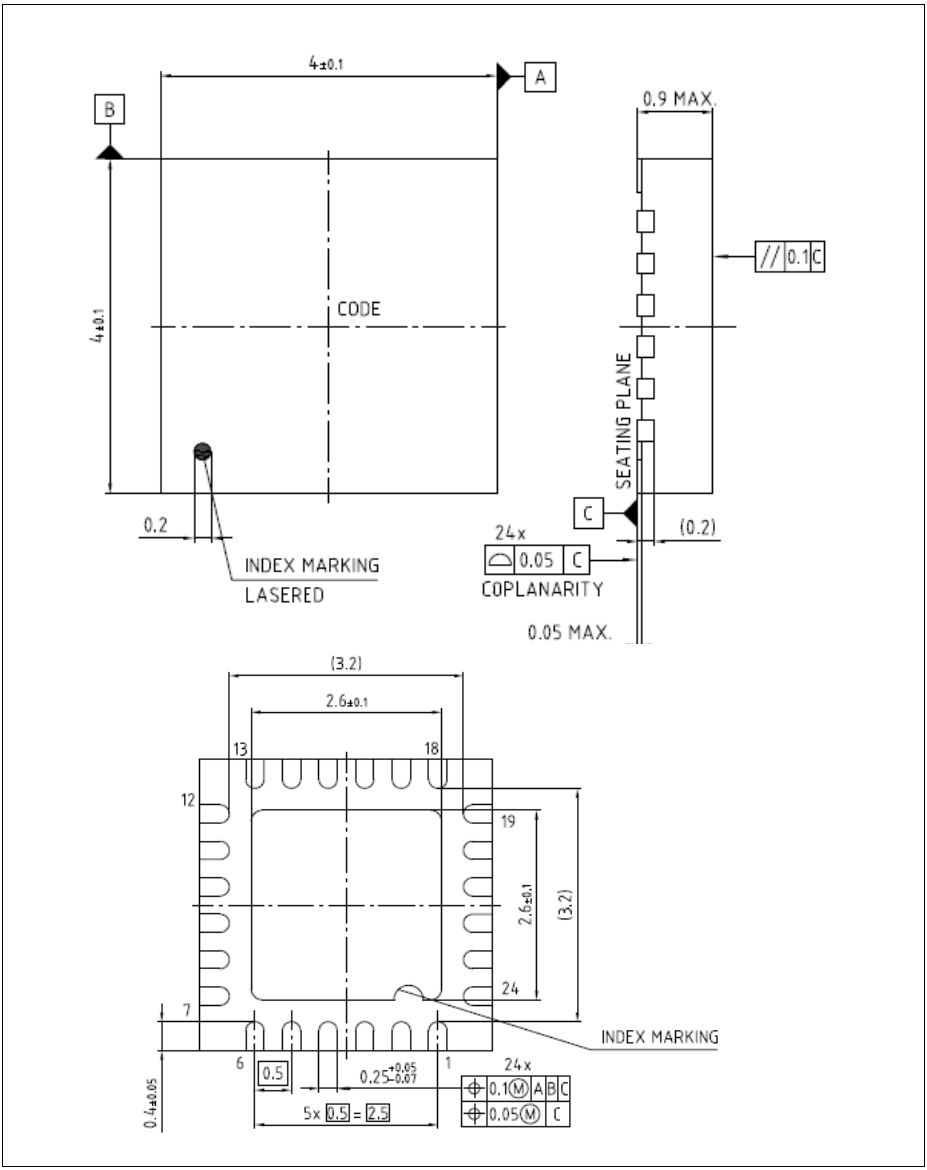


Figure 29 PG-VQFN-24-19

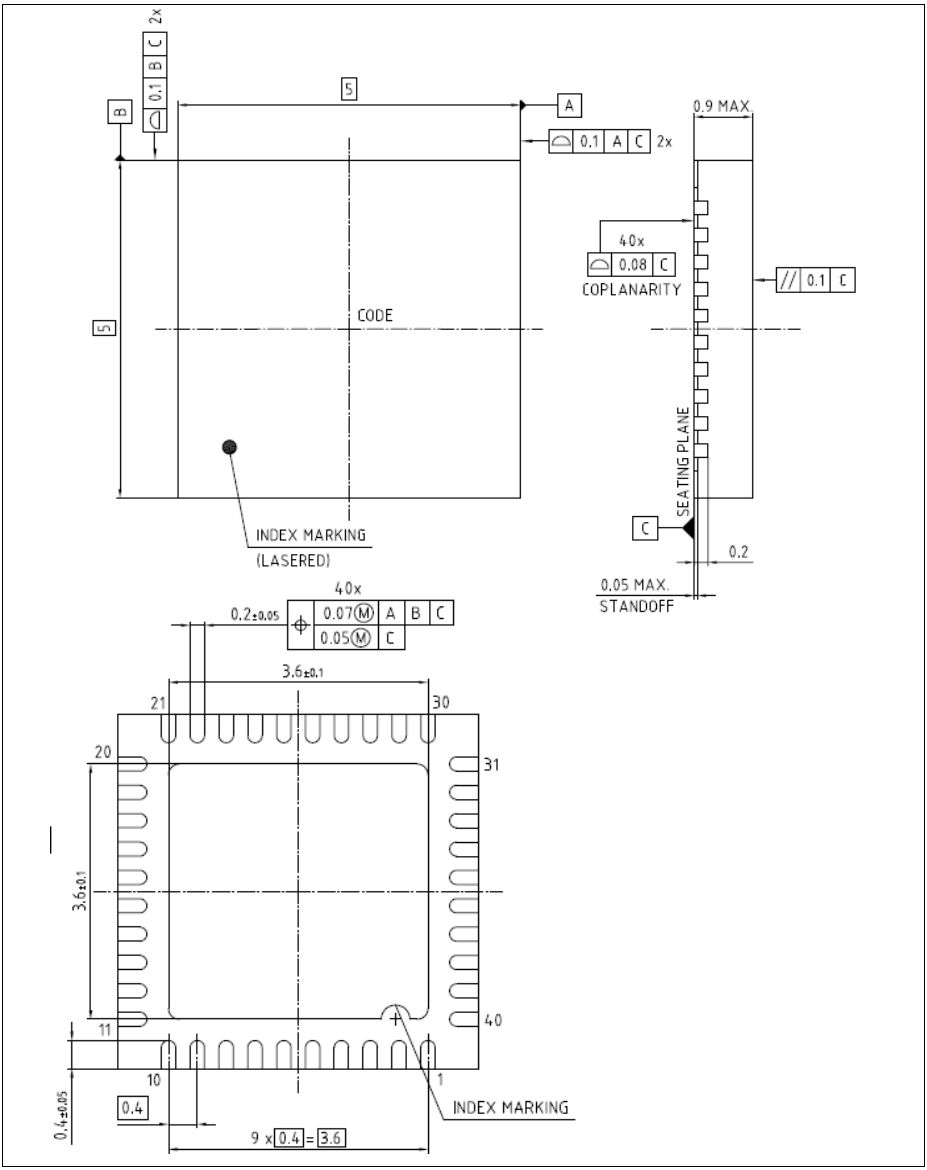


Figure 30 PG-VQFN-40-13

All dimensions in mm.

5 Quality Declaration

Table 36 shows the characteristics of the quality parameters in the XMC1300.

Table 36 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D