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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 11 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 11x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 16-TSSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-16-8 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t016f0032abxuma1 |

# XMC1300 AB-Step

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

## Data Sheet

V1.9 2017-03

Microcontrollers

Table of Contents

# About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1300 series devices.

The document describes the characteristics of a superset of the XMC1300 series devices. For simplicity, the various device types are referred to by the collective term XMC1300 throughout this document.

### XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

***Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.***

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

## 1.3 Device Type Features

The following table lists the available features per device type.

**Table 2 Features of XMC1300 Device Types[1)]**

| Derivative | ADC channel | ACMP | BCCU | MATH |
|---|---|---|---|---|
| XMC1301-T016 | 11 | 2 | - | - |
| XMC1302-T016 | 11 | 2 | 1 | 1 |
| XMC1302-T028 | 14 | 3 | 1 | 1 |
| XMC1301-T038 | 16 | 3 | - | - |
| XMC1302-T038 | 16 | 3 | 1 | 1 |
| XMC1301-Q024 | 13 | 3 | - | - |
| XMC1302-Q024 | 13 | 3 | 1 | 1 |
| XMC1301-Q040 | 16 | 3 | - | - |
| XMC1302-Q040 | 16 | 3 | 1 | 1 |

1) Features that are not included in this table are available in all the derivatives

**Table 3 ADC Channels [1)]**

| Package | VADC0 G0 | VADC0 G1 |
|---|---|---|
| PG-TSSOP-16 | CH0..CH5 | CH0..CH4 |
| PG-TSSOP-28 | CH0..CH7 | CH0 .. CH4, CH7 |
| PG-TSSOP-38 | CH0..CH7 | CH0..CH7 |
| PG-VQFN-24 | CH0..CH7 | CH0..CH4 |
| PG-VQFN-40 | CH0..CH7 | CH0..CH7 |

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

## 1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

# 2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

## 2.1 Logic Symbols

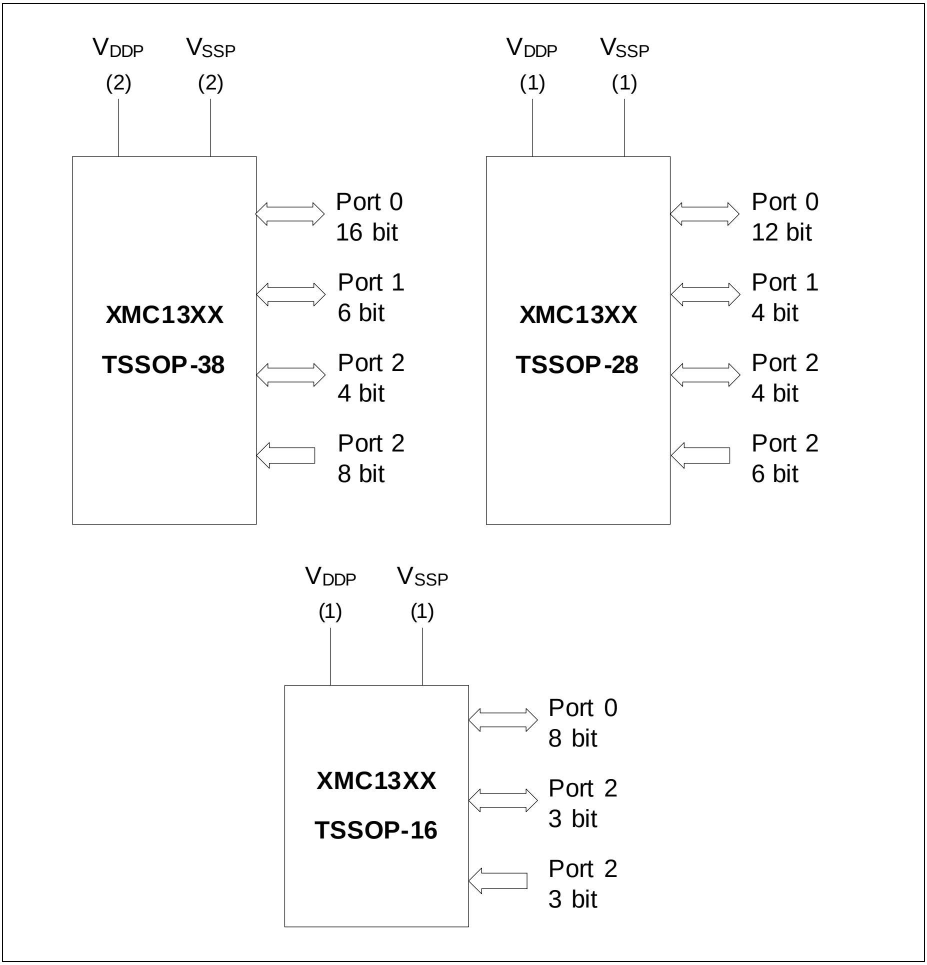


**Figure 2 XMC1300 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16**

## 2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

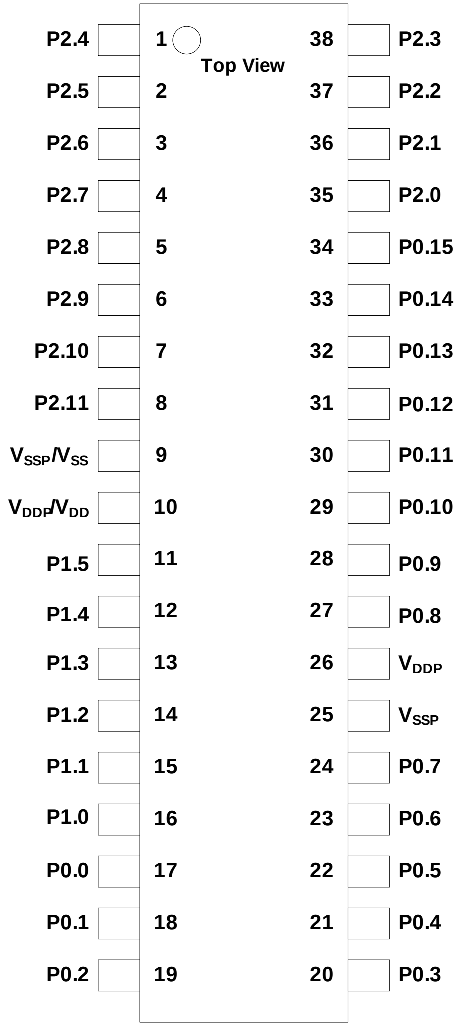


**Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration** (top view)

## Table 10 Hardware Controlled I/O Functions

| Function | Outputs | | Inputs | | Pull Control | | | |
|---|---|---|---|---|---|---|---|---|
| | HWO0 | HWO1 | HWI0 | HWI1 | HW0_PD | HW0_PU | HW1_PD | HW1_PU |
| P0.0 | | | | | | | | |
| P0.1 | | | | | | | | |
| P0.2 | | | | | | | | |
| P0.3 | | | | | | | | |
| P0.4 | | | | | | | | |
| P0.5 | | | | | | | | |
| P0.6 | | | | | | | | |
| P0.7 | | | | | | | | |
| P0.8 | | | | | | | | |
| P0.9 | | | | | | | | |
| P0.10 | | | | | | | | |
| P0.11 | | | | | | | | |
| P0.12 | | | | | | | | |
| P0.13 | | | | | | | | |
| P0.14 | | | | | | | | |
| P0.15 | | | | | | | | |
| P1.0 | | USIC0_CH0.DOUT0 | | USIC0_CH0.HWIN0 | $\overline{\text{BCCU0.OUT2}}$ | BCCU0.OUT2 | | |
| P1.1 | | USIC0_CH0.DOUT1 | | USIC0_CH0.HWIN1 | $\overline{\text{BCCU0.OUT3}}$ | BCCU0.OUT3 | | |
| P1.2 | | USIC0_CH0.DOUT2 | | USIC0_CH0.HWIN2 | $\overline{\text{BCCU0.OUT4}}$ | BCCU0.OUT4 | | |
| P1.3 | | USIC0_CH0.DOUT3 | | USIC0_CH0.HWIN3 | $\overline{\text{BCCU0.OUT5}}$ | BCCU0.OUT5 | | |
| P1.4 | | | | | $\overline{\text{BCCU0.OUT6}}$ | BCCU0.OUT6 | | |
| P1.5 | | | | | $\overline{\text{BCCU0.OUT7}}$ | BCCU0.OUT7 | | |
| P1.6 | | | | | $\overline{\text{BCCU0.OUT8}}$ | BCCU0.OUT8 | | |
| P2.0 | | | | | $\overline{\text{BCCU0.OUT1}}$ | BCCU0.OUT1 | | |
| P2.1 | | | | | $\overline{\text{BCCU0.OUT6}}$ | BCCU0.OUT6 | | |
| P2.2 | | | | | $\overline{\text{BCCU0.OUT0}}$ | BCCU0.OUT0 | $\overline{\text{CCU40.OUT3}}$ | CCU40.OUT3 |
| P2.3 | | | | | $\overline{\text{ACMP2.OUT}}$ | ACMP2.OUT | | |
| P2.4 | | | | | $\overline{\text{BCCU0.OUT8}}$ | BCCU0.OUT8 | | |
| P2.5 | | | | | $\overline{\text{ACMP1.OUT}}$ | ACMP1.OUT | | |

### 3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

**Table 12** defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels ($V_{DDP}$)
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

*Note: An overload condition on one or more pins does not require a reset.*

*Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.*

**Table 12 Overload Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input current on any port pin during overload condition | $I_{OV}$ | SR | -5 | – | 5 | mA | |
| Absolute sum of all input circuit currents during overload condition | $I_{OVS}$ | SR | – | – | 25 | mA | |

**Figure 10** shows the path of the input currents during overload via the ESD protection structures. The diodes against $V_{DDP}$ and ground are a simplified representation of these ESD protection structures.

### 3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

**Table 15 Operating Conditions Parameters**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Ambient Temperature | $T_A$ | SR | -40 | – | 85 | °C | Temp. Range F |
| | | | -40 | – | 105 | °C | Temp. Range X |
| Digital supply voltage[1] | $V_{DDP}$ | SR | 1.8 | – | 5.5 | V | |
| MCLK Frequency | $f_{MCLK}$ | CC | – | – | 33.2 | MHz | CPU clock |
| PCLK Frequency | $f_{PCLK}$ | CC | – | – | 66.4 | MHz | Peripherals clock |
| Short circuit current of digital outputs | $I_{SC}$ | SR | -5 | – | 5 | mA | |
| Absolute sum of short circuit currents of the device | $\Sigma I_{SC\_D}$ | SR | – | – | 25 | mA | |

1) See also the Supply Monitoring thresholds, Chapter 3.3.2.

### 3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages ($V_{AIN}$) above the $V_{DDP}$ on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 18 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; $V_{DDP}$ = 3.0 V - 5.5 V; $C_L$ = 0.25 pF)**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| DC Switching Level | $V_{ODC}$ | CC | 54 | – | 183 | mV | VAIN ≥ $V_{DDP}$ + $V_{ODC}$ |
| Hysteresis | $V_{OHYS}$ | CC | 15 | – | 54 | mV | |
| Always detected Overvoltage Pulse | $t_{OPDD}$ | CC | 103 | – | - | ns | $V_{AIN} \geq V_{DDP}$ + 150 mV |
| | | | 88 | – | - | ns | $V_{AIN} \geq V_{DDP}$ + 350 mV |
| Never detected Overvoltage Pulse | $t_{OPDN}$ | CC | – | – | 21 | ns | $V_{AIN} \geq V_{DDP}$ + 150 mV |
| | | | – | – | 11 | ns | $V_{AIN} \geq V_{DDP}$ + 350 mV |
| Detection Delay of a persistent Overvoltage | $t_{ODD}$ | CC | 39 | – | 132 | ns | $V_{AIN} \geq V_{DDP}$ + 150 mV |
| | | | 31 | – | 121 | ns | $V_{AIN} \geq V_{DDP}$ + 350 mV |
| Release Delay | $t_{ORD}$ | CC | 44 | – | 240 | ns | $V_{AIN} \leq V_{DDP}$; $V_{DDP}$ = 5 V |
| | | | 57 | – | 340 | ns | $V_{AIN} \leq V_{DDP}$; $V_{DDP}$ = 3.3 V |
| Enable Delay | $t_{OED}$ | CC | – | – | 300 | ns | ORCCTRL.ENORCx = 1 |

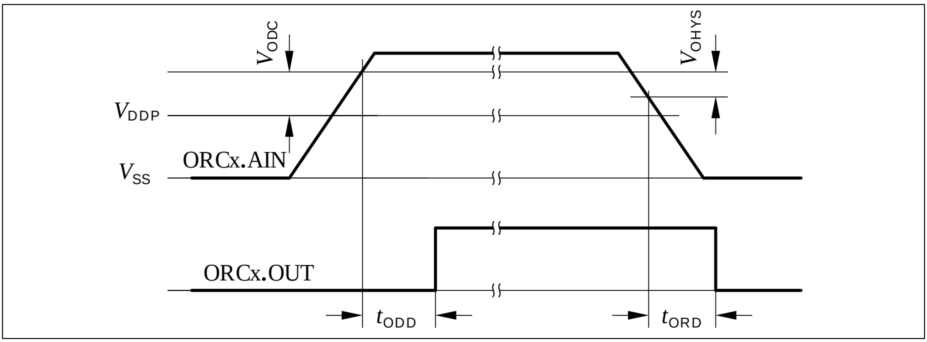


**Figure 12 ORCx.OUT Trigger Generation**

### 3.2.4 Analog Comparator Characteristics

**Table 19** below shows the Analog Comparator characteristics.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 19 Analog Comparator Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Notes/ Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input Voltage | $V_{CMP}$ | SR | -0.05 | – | $V_{DDP}$ + 0.05 | V | |
| Input Offset | $V_{CMPOFF}$ | CC | – | +/-3 | – | mV | High power mode $\Delta V_{CMP}$ < 200 mV |
| | | | – | +/-20 | – | mV | Low power mode $\Delta V_{CMP}$ < 200 mV |
| Propagation Delay[1)] | $t_{PDELAY}$ | CC | – | 25 | – | ns | High power mode, $\Delta V_{CMP}$ = 100 mV |
| | | | – | 80 | – | ns | High power mode, $\Delta V_{CMP}$ = 25 mV |
| | | | – | 250 | – | ns | Low power mode, $\Delta V_{CMP}$ = 100 mV |
| | | | – | 700 | – | ns | Low power mode, $\Delta V_{CMP}$ = 25 mV |
| Current Consumption | $I_{ACMP}$ | CC | – | 100 | – | μA | First active ACMP in high power mode, $\Delta V_{CMP}$ > 30 mV |
| | | | – | 66 | – | μA | Each additional ACMP in high power mode, $\Delta V_{CMP}$ > 30 mV |
| | | | – | 10 | – | μA | First active ACMP in low power mode |
| | | | – | 6 | – | μA | Each additional ACMP in low power mode |
| Input Hysteresis | $V_{HYS}$ | CC | – | +/-15 | – | mV | |
| Filter Delay[1)] | $t_{FDELAY}$ | CC | – | 5 | – | ns | |

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

### 3.2.5 Temperature Sensor Characteristics

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 20 Temperature Sensor Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Measurement time | $t_M$ CC | – | – | 10 | ms | |
| Temperature sensor range | $T_{SR}$ SR | -40 | – | 115 | °C | |
| Sensor Accuracy[1] | $T_{TSAL}$ CC | -6 | – | 6 | °C | $T_J > 20°C$ |
| | | -10 | – | 10 | °C | $0°C \leq T_J \leq 20°C$ |
| | | – | -/+8 | – | °C | $T_J < 0°C$ |
| Start-up time after enabling | $t_{TSSTE}$ SR | – | – | 15 | µs | |

1) The temperature sensor accuracy is independent of the supply voltage.

## 3.3 AC Parameters

### 3.3.1 Testing Waveforms

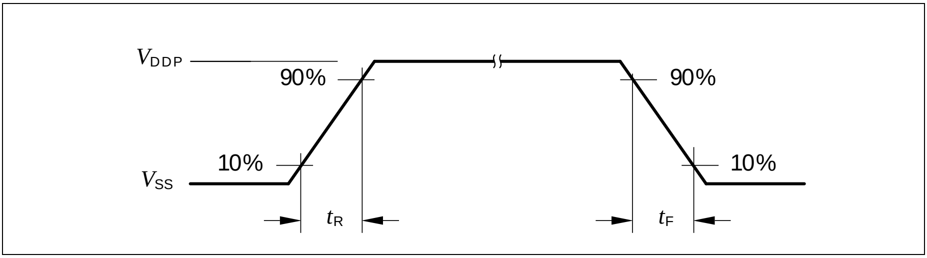


**Figure 16 Rise/Fall Time Parameters**

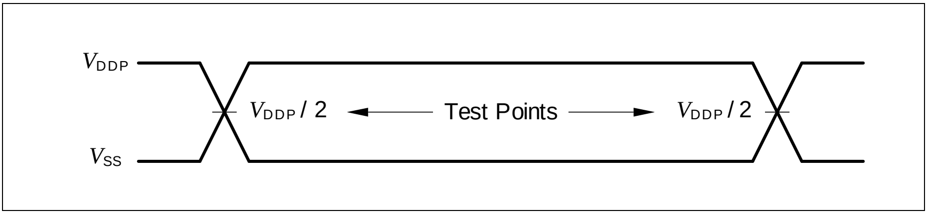


**Figure 17 Testing Waveform, Output Delay**

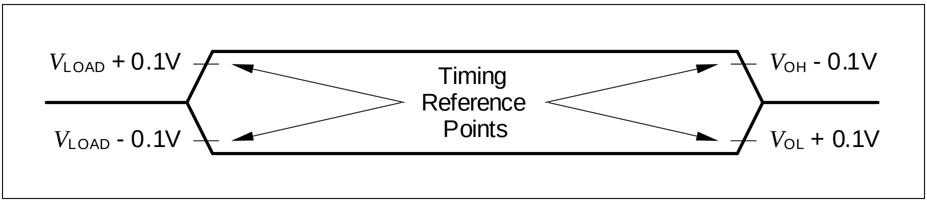


**Figure 18 Testing Waveform, Output High Impedance**

### 3.3.3 On-Chip Oscillator Characteristics

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

Table 25 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

**Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | – | 64 | – | MHz | under nominal conditions[1] after trimming |
| Accuracy[2] | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature ($T_A$ = 0 °C to 85 °C) |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature ($T_A$ = -40 °C to 105 °C) |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

2) The accuracy can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

Figure 20 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

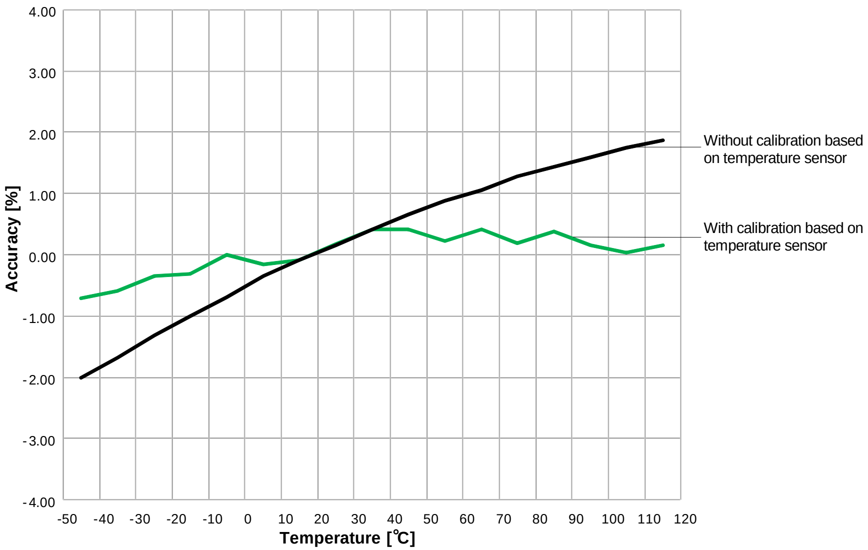


**Figure 20 Typical DCO1 accuracy over temperature**

Table 26 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

**Table 26 32 kHz DCO2 Characteristics (Operating Conditions apply)**

| Parameter | Symbol | | Limit Values | | | Unit | Test Conditions |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Nominal frequency | $f_{NOM}$ | CC | – | 32.75 | – | kHz | under nominal conditions[1] after trimming |
| Accuracy | $\Delta f_{LT}$ | CC | -1.7 | – | 3.4 | % | with respect to $f_{NOM}$(typ), over temperature (0 °C to 85 °C) |
| | | | -3.9 | – | 4.0 | % | with respect to $f_{NOM}$(typ), over temperature (-40 °C to 105 °C) |

1) The deviation is relative to the factory trimmed frequency at nominal $V_{DDC}$ and $T_A$ = + 25 °C.

### 3.3.5 SPD Timing Requirements

The optimum SPD decision time between $0_B$ and $1_B$ is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

**Table 28 Optimum Number of Sample Clocks for SPD**

| Sample Freq. | Sampling Factor | Sample Clocks $0_B$ | Sample Clocks $1_B$ | Effective Decision Time[1)] | Remark |
|---|---|---|---|---|---|
| 8 MHz | 4 | 1 to 5 | 6 to 12 | 0.69 µs | The other closest option (0.81 µs) for the effective decision time is less robust. |

1) Nominal sample frequency period multiplied with 0.5 + (max. number of $0_B$ sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

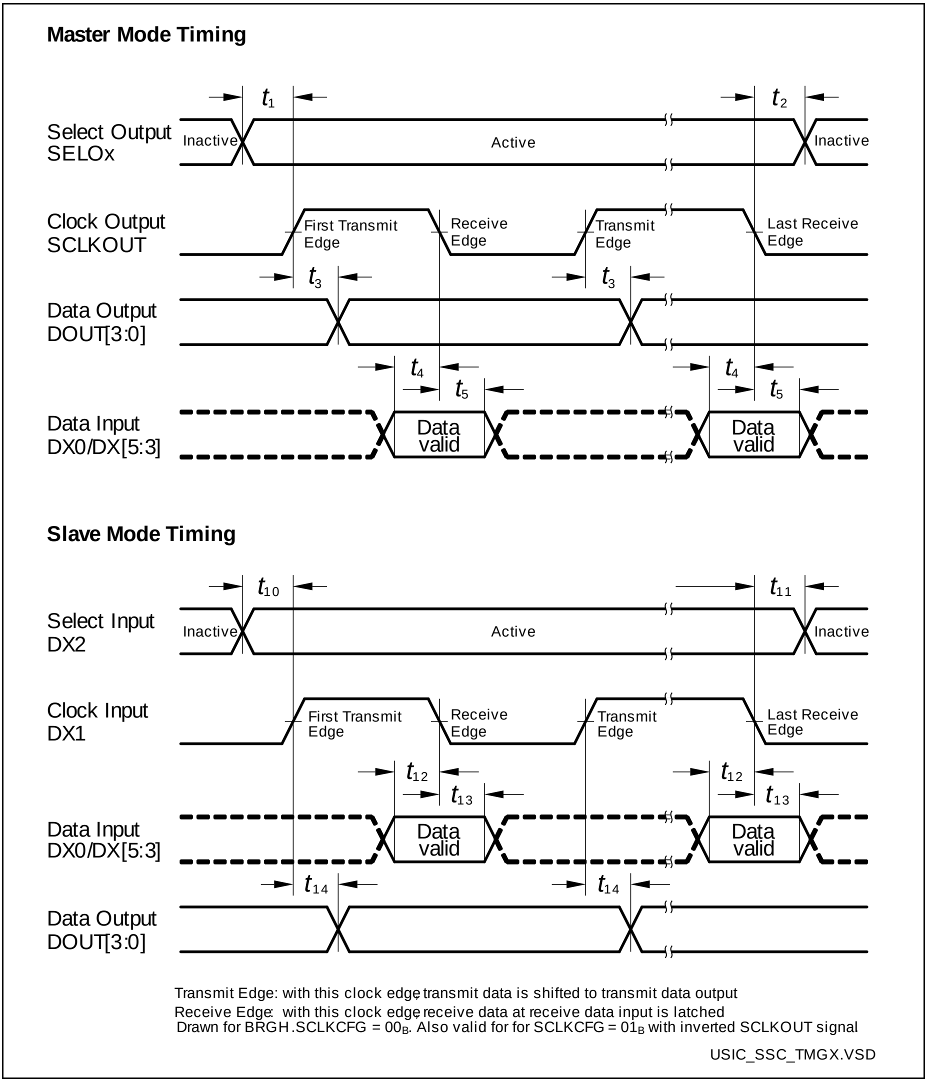


**Figure 22 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

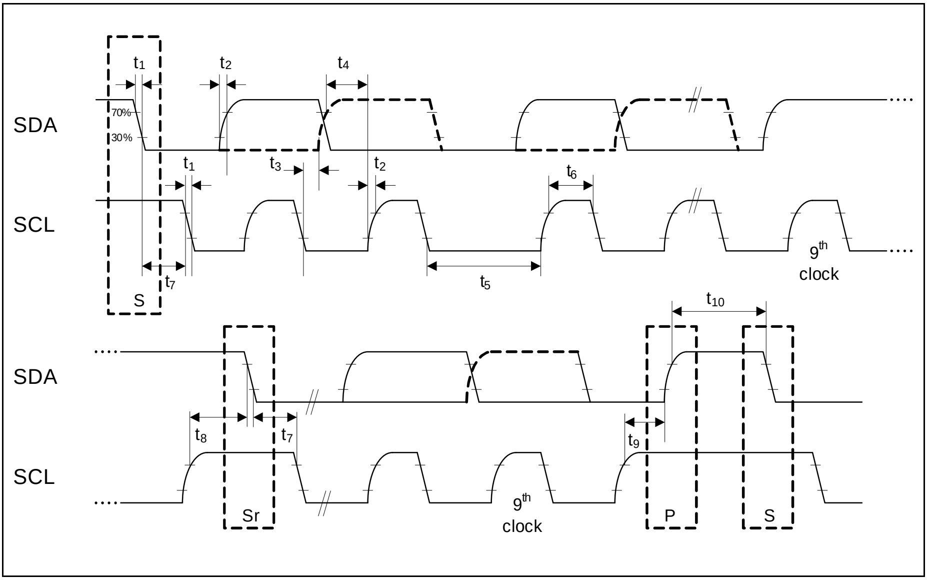


**Figure 23 USIC IIC Stand and Fast Mode Timing**

## 3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 33 USIC IIS Master Transmitter Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | $2/f_{MCLK}$ | - | - | ns | $V_{DDP} \geq 3$ V |
| | | $4/f_{MCLK}$ | - | - | ns | $V_{DDP} < 3$ V |
| Clock HIGH | $t_2$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Clock Low | $t_3$ CC | 0.35 x $t_{1min}$ | - | - | ns | |
| Hold time | $t_4$ CC | 0 | - | - | ns | |
| Clock rise time | $t_5$ CC | - | - | 0.15 x $t_{1min}$ | ns | |

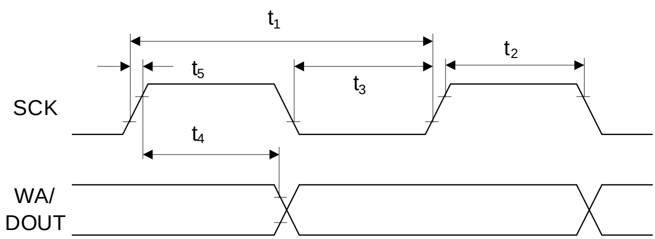


**Figure 24 USIC IIS Master Transmitter Timing**

**Table 34 USIC IIS Slave Receiver Timing**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_6$ SR | $4/f_{MCLK}$ | - | - | ns | |
| Clock HIGH | $t7$ SR | 0.35 x $t_{6min}$ | - | - | ns | |
| Clock Low | $t8$ SR | 0.35 x $t_6$min | - | - | ns | |
| Set-up time | $t9$ SR | 0.2 x $t_6$min | - | - | ns | |
| Hold time | $t10$ SR | 10 | - | - | ns | |

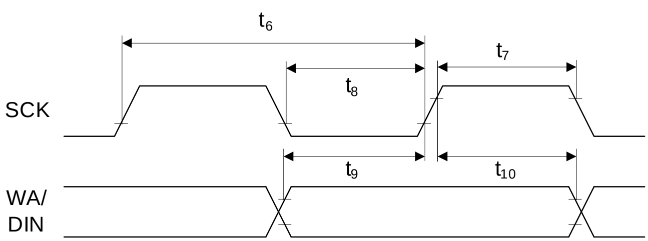


**Figure 25 USIC IIS Slave Receiver Timing**

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