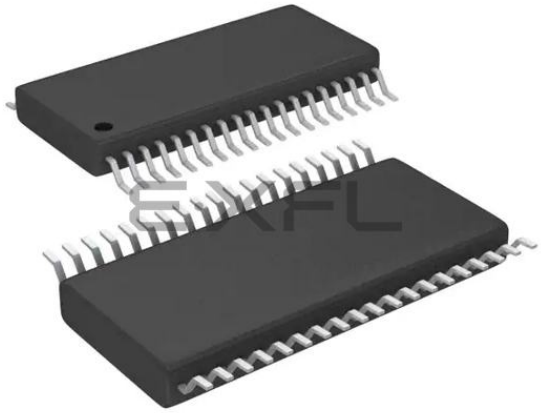
Infineon Technologies - XMC1301T038F0008ABXUMA1 Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t038f0008abxuma1

Table 4 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1302-Q040X0128	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 $201ED083_H$	AB
XMC1302-Q040X0200	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 $201ED083_H$	AB

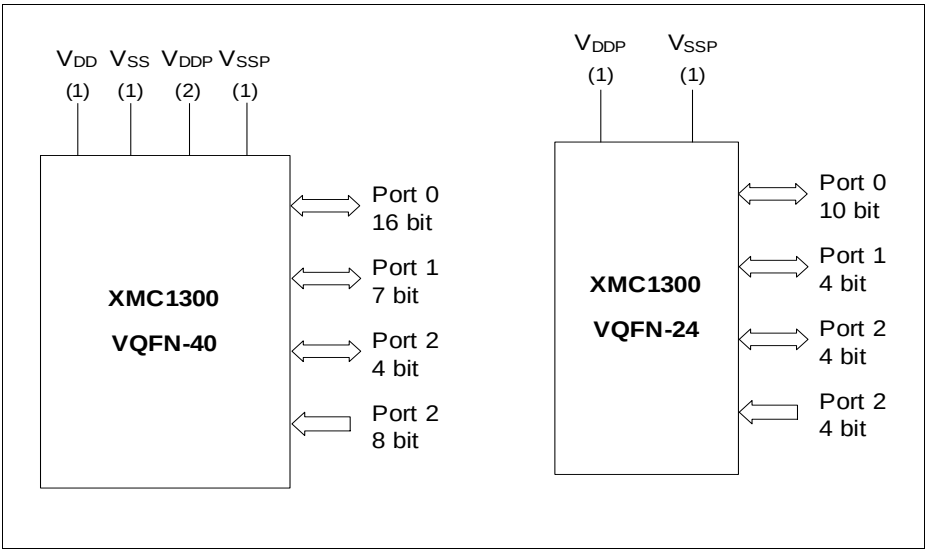


Figure 3 XMC1300 Logic Symbol for VQFN-24 and VQFN-40

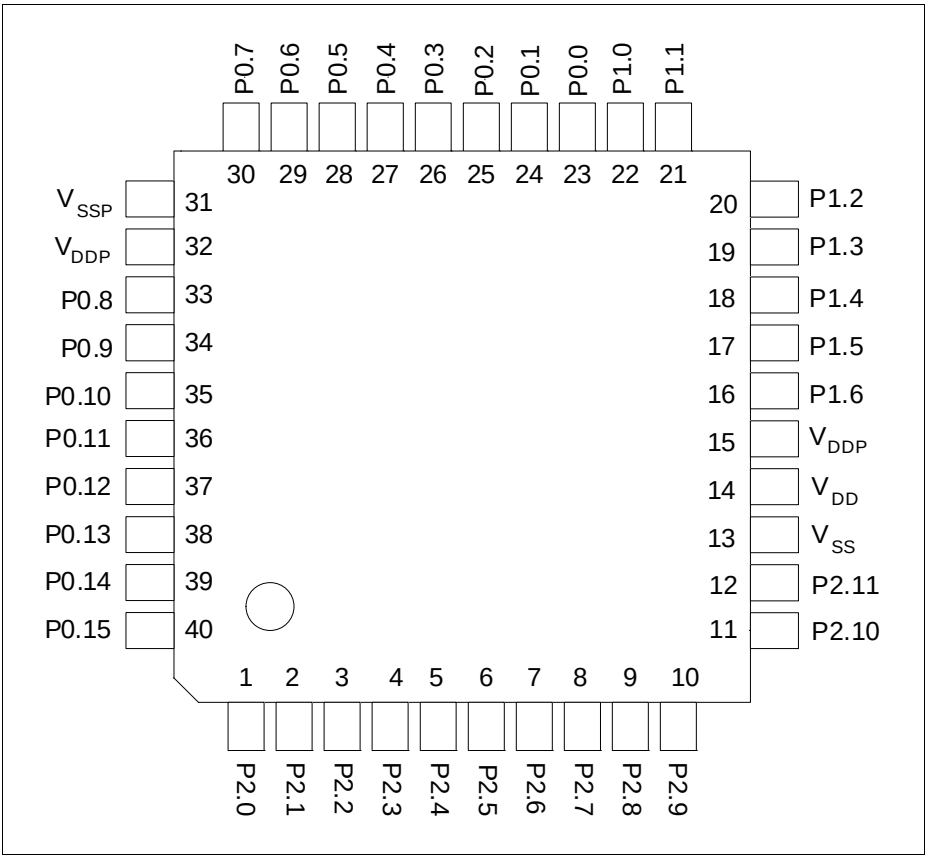


Figure 8 XMC1300 PG-VQFN-40 Pin Configuration (top view)

Table 9 Port I/O Functions

Function	Outputs							Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0		ERU0.GOUT0	CCU40.OUT0	CCU80.OUT00	USIC0_CH0.SELO0	USIC0_CH1.SELO0	BCCU0.TRAPINB	CCU40.IN0C			USIC0_CH0.DX2A	USIC0_CH1.DX2A				
P0.1	ERU0.PDOUT1		ERU0.GOUT1	CCU40.OUT1	CCU80.OUT01	BCCU0.OUT8	SCU.VDROP		CCU40.IN1C								
P0.2	ERU0.PDOUT2		ERU0.GOUT2	CCU40.OUT2	CCU80.OUT02	VADC0.EMUX02	CCU80.OUT10		CCU40.IN2C								
P0.3	ERU0.PDOUT3		ERU0.GOUT3	CCU40.OUT3	CCU80.OUT03	VADC0.EMUX01	CCU80.OUT11		CCU40.IN3C								
P0.4	BCCU0.OUT0			CCU40.OUT1	CCU80.OUT13	VADC0.EMUX00	WWDT.SERVICE_OUT		CCU80.IN0B								
P0.5	BCCU0.OUT1			CCU40.OUT0	CCU80.OUT12	ACMP2.OUT	CCU80.OUT01		CCU80.IN1B								
P0.6	BCCU0.OUT2			CCU40.OUT0	CCU80.OUT11	USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0		CCU40.IN0B			USIC0_CH1.DX0C					
P0.7	BCCU0.OUT3			CCU40.OUT1	CCU80.OUT10	USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0		CCU40.IN1B			USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C			
P0.8	BCCU0.OUT4			CCU40.OUT2	CCU80.OUT20	USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT		CCU40.IN2B			USIC0_CH0.DX1B	USIC0_CH1.DX1B				
P0.9	BCCU0.OUT5			CCU40.OUT3	CCU80.OUT21	USIC0_CH0.SELO0	USIC0_CH1.SELO0		CCU40.IN3B			USIC0_CH0.DX2B	USIC0_CH1.DX2B				
P0.10	BCCU0.OUT6			ACMP0.OUT	CCU80.OUT22	USIC0_CH0.SELO1	USIC0_CH1.SELO1		CCU80.IN2B			USIC0_CH0.DX2C	USIC0_CH1.DX2C				
P0.11	BCCU0.OUT7			USIC0_CH0.MCLKOUT	CCU80.OUT23	USIC0_CH0.SELO2	USIC0_CH1.SELO2					USIC0_CH0.DX2D	USIC0_CH1.DX2D				
P0.12	BCCU0.OUT6				CCU80.OUT33	USIC0_CH0.SELO3	CCU80.OUT20	BCCU0.TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A	USIC0_CH0.DX2E
P0.13	WWDT.SERVICE_OUT				CCU80.OUT32	USIC0_CH0.SELO4	CCU80.OUT21		CCU80.IN3B	POSIF0.IN0B		USIC0_CH0.DX2F					

3.1.3 Pin Reliability in Overload

When receiving signals from higher voltage devices, low-voltage devices experience overload currents and voltages that go beyond their own IO power supplies specification.

Table 12 defines overload conditions that will not cause any negative reliability impact if all the following conditions are met:

- full operation life-time is not exceeded
- **Operating Conditions** are met for
  - pad supply levels (V_{DDP})
  - temperature

If a pin current is outside of the **Operating Conditions** but within the overload conditions, then the parameters of this pin as stated in the Operating Conditions can no longer be guaranteed. Operation is still possible in most cases but with relaxed parameters.

Note: An overload condition on one or more pins does not require a reset.

Note: A series resistor at the pin to limit the current to the maximum permitted overload current is sufficient to handle failure situations like short to battery.

Table 12 Overload Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Input current on any port pin during overload condition	I_{OV}	SR	-5	–	5	mA	
Absolute sum of all input circuit currents during overload condition	I_{OVS}	SR	–	–	25	mA	

Figure 10 shows the path of the input currents during overload via the ESD protection structures. The diodes against V_{DDP} and ground are a simplified representation of these ESD protection structures.

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	–	0.08 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[18]
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	0.85 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)[18]
Rise time on High Current Pad[1]	t_{HCPR}	CC	–	9	ns	50 pF @ 5 V[2]
			–	12	ns	50 pF @ 3.3 V[3]
			–	25	ns	50 pF @ 1.8 V[4]
Fall time on High Current Pad[1]	t_{HCPF}	CC	–	9	ns	50 pF @ 5 V[2]
			–	12	ns	50 pF @ 3.3 V[3]
			–	25	ns	50 pF @ 1.8 V[4]
Rise time on Standard Pad[1]	t_R	CC	–	12	ns	50 pF @ 5 V[5]
			–	15	ns	50 pF @ 3.3 V[6]
			–	31	ns	50 pF @ 1.8 V[7]
Fall time on Standard Pad[1]	t_F	CC	–	12	ns	50 pF @ 5 V[5]
			–	15	ns	50 pF @ 3.3 V[6]
			–	31	ns	50 pF @ 1.8 V[7]

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis[8)]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.5 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.4 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.2 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up resistor on port pins	R_{PUP}	CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	R_{PDP}	CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current[9)]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[10)]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high currrent pins	I_{MP1A}	SR	-10	50	mA	–
Maximum current into V_{DDP} (TSSOP16, VQFN24)	I_{MVDD1}	SR	–	130	mA	[18)]
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	[18)]

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current out of V_{SS} (TSSOP16, VQFN24)	I_{MVSS1}	SR	–	130	mA	18)
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	18)

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
4) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
5) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
7) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.
8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 17 ADC Characteristics (Operating Conditions apply)[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00_B (unity gain)
		3			–	GNCTRxz.GAINy = 01_B (gain g1)
		6			–	GNCTRxz.GAINy = 10_B (gain g2)
		12			–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DD} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DD} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DD} = 2.0 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC	20			1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode 3)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode 3)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			1 / f_{ADC}	2)

Table 17 ADC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Maximum sample rate in 8-bit mode [3]	f_{C8} CC	–	–	f_{ADC} / 38.5	–	1 sample pending
		–	–	f_{ADC} / 54.5	–	2 samples pending
RMS noise [4]	EN_{RMS} CC	–	1.5	–	LSB 12	DC input, V_{DD} = 5.0 V, $V_{AIN = 2.5 V}$, 25°C
DNL error	EA_{DNL} CC	–	±2.0	–	LSB 12	
INL error	EA_{INL} CC	–	±4.0	–	LSB 12	
Gain error with external reference	EA_{GAIN} CC	–	±0.5	–	%	SHSCFG.AREF = 00_B (calibrated)
Gain error with internal reference [5]	EA_{GAIN} CC	–	±3.6	–	%	SHSCFG.AREF = $1X_B$ (calibrated), -40°C - 105°C
		–	±2.0	–	%	SHSCFG.AREF = $1X_B$ (calibrated), 0°C - 85°C
Offset error	EA_{OFF} CC	–	±8.0	–	mV	Calibrated, V_{DD} = 5.0 V

1) The parameters are defined for ADC clock frequency f_{SH} = 32MHz, SHSCFG.DIVS = 0000_B. Usage of any other frequencies may affect the ADC performance.

2) No pending samples assumed, excluding sampling time and calibration.

3) Includes synchronization and calibration (average of gain and offset calibration).

4) This parameter can also be defined as an SNR value: SNR[dB] = 20 × log(A_{MAXeff} / N_{RMS}).
With $A_{MAXeff} = 2^N / 2$, SNR[dB] = 20 × log (2048 / N_{RMS}) [N = 12].
N_{RMS} = 1.5 LSB12, therefore, equals SNR = 20 × log (2048 / 1.5) = 62.7 dB.

5) Includes error from the reference voltage.

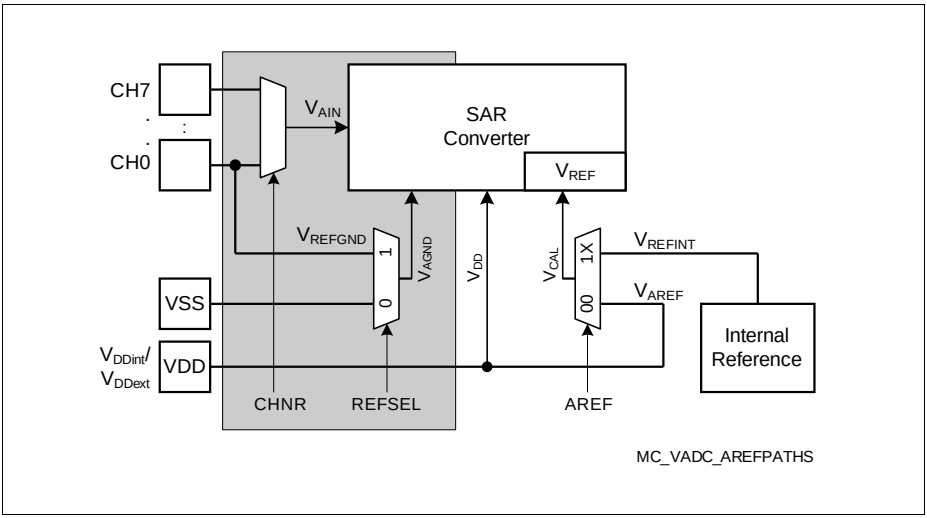


Figure 11 ADC Voltage Supply

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25 pF)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	54	–	183	mV	$VAIN \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	15	–	54	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	-	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			88	–	-	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

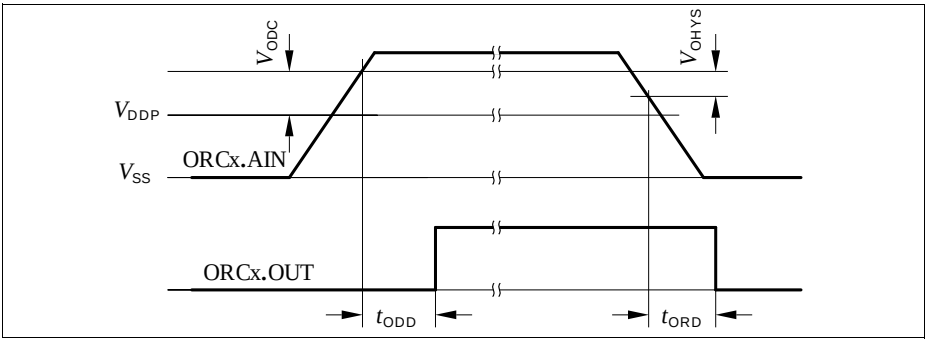
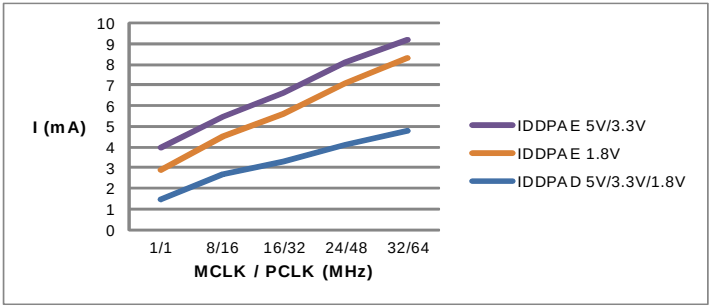


Figure 12 ORCx.OUT Trigger Generation

Figure 14 shows typical graphs for active mode supply current for V_{DDP} = 5V, V_{DDP} = 3.3V, V_{DDP} = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

Figure 14 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

3.3.2 Power-Up and Supply Monitoring Characteristics

Table 24 provides the characteristics of the power-up and supply monitoring in XMC1300.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while V_{DDP} is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} ramp-up time	t_{RAMPUP} SR	V_{DDP}/ $S_{VDDPrise}$	–	10^7	µs	
V_{DDP} slew rate	S_{VDDPOP} SR	0	–	0.1	V/µs	Slope during normal operation
	S_{VDDP10} SR	0	–	10	V/µs	Slope during fast transient within +/- 10% of V_{DDP}
	$S_{VDDPrise}$ SR	0	–	10	V/µs	Slope during power-on or restart after brownout event
	$S_{VDDPfall}$ [1] SR	0	–	0.25	V/µs	Slope during supply falling out of the +/-10% limits[2]
V_{DDP} prewarning voltage	V_{DDPPW} CC	2.1	2.25	2.4	V	ANAVDEL.VDEL_SELECT = 00_B
		2.85	3	3.15	V	ANAVDEL.VDEL_SELECT = 01_B
		4.2	4.4	4.6	V	ANAVDEL.VDEL_SELECT = 10_B

3.3.3 On-Chip Oscillator Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	64	–	MHz	under nominal conditions[1] after trimming
Accuracy[2]	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (T_A = 0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (T_A = -40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

2) The accuracy can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 28 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 31 USIC IIC Standard Mode Timing[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	µs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP}, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

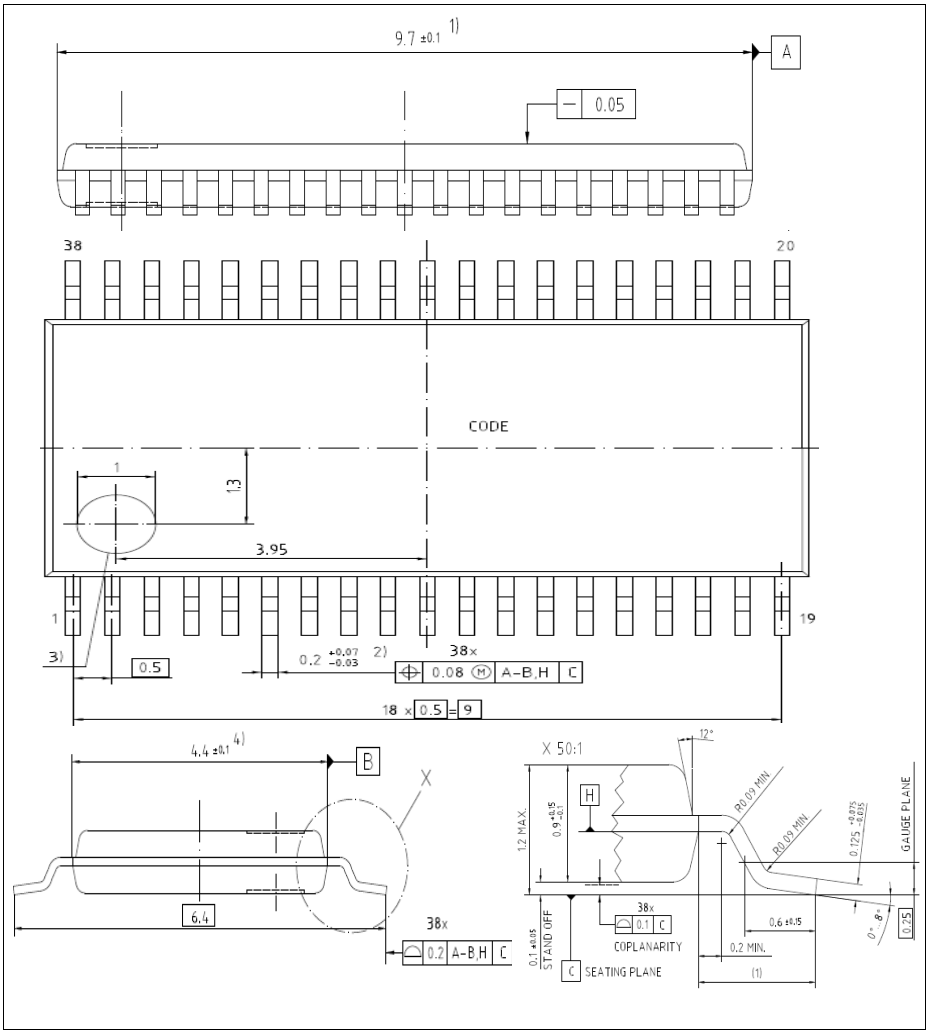


Figure 26 PG-TSSOP-38-9

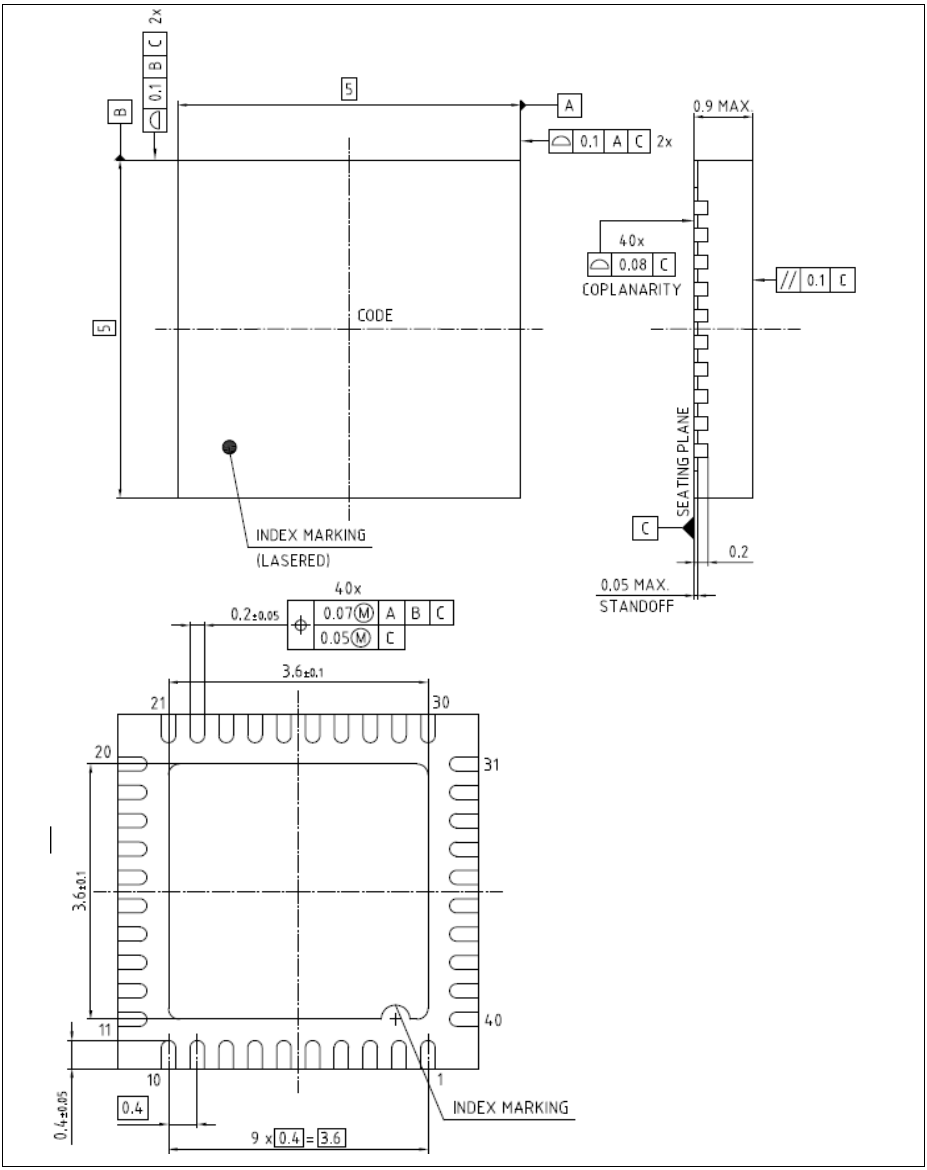


Figure 30 PG-VQFN-40-13

All dimensions in mm.