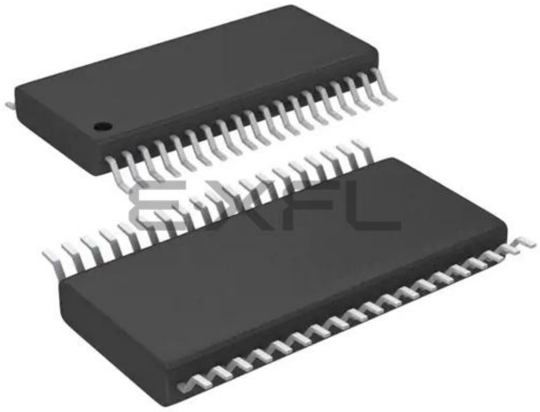


## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| **Details** | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 26 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 16x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 38-TFSOP (0.173", 4.40mm Width) |
| Supplier Device Package | PG-TSSOP-38-9 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1301t038f0064abxuma1 |

# Table of Contents

- Configurable pad hysteresis

**On-Chip Debug Support**

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

## 1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

## 1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

**Table 1 Synopsis of XMC1300 Device Types**

| Derivative | Package | Flash Kbytes | SRAM Kbytes |
|---|---|---|---|
| XMC1301-T016F0008 | PG-TSSOP-16-8 | 8 | 16 |
| XMC1301-T016F0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1301-T016F0032 | PG-TSSOP-16-8 | 32 | 16 |
| XMC1301-T016X0008 | PG-TSSOP-16-8 | 8 | 16 |
| XMC1301-T016X0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1302-T016X0008 | PG-TSSOP-16-8 | 8 | 16 |

**Table 1 Synopsis of XMC1300 Device Types** (cont'd)

| Derivative | Package | Flash Kbytes | SRAM Kbytes |
|---|---|---|---|
| XMC1302-T016X0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1302-T016X0032 | PG-TSSOP-16-8 | 32 | 16 |
| XMC1302-T028X0016 | PG-TSSOP-28-8 | 16 | 16 |
| XMC1301-T038F0008 | PG-TSSOP-38-9 | 8 | 16 |
| XMC1301-T038F0016 | PG-TSSOP-38-9 | 16 | 16 |
| XMC1301-T038F0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1301-T038X0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1301-T038F0064 | PG-TSSOP-38-9 | 64 | 16 |
| XMC1302-T038X0016 | PG-TSSOP-38-9 | 16 | 16 |
| XMC1302-T038X0032 | PG-TSSOP-38-9 | 32 | 16 |
| XMC1302-T038X0064 | PG-TSSOP-38-9 | 64 | 16 |
| XMC1302-T038X0128 | PG-TSSOP-38-9 | 128 | 16 |
| XMC1302-T038X0200 | PG-TSSOP-38-9 | 200 | 16 |
| XMC1301-Q024F0008 | PG-VQFN-24-19 | 8 | 16 |
| XMC1301-Q024F0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1302-Q024F0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1302-Q024F0032 | PG-VQFN-24-19 | 32 | 16 |
| XMC1302-Q024F0064 | PG-VQFN-24-19 | 64 | 16 |
| XMC1302-Q024X0016 | PG-VQFN-24-19 | 16 | 16 |
| XMC1302-Q024X0032 | PG-VQFN-24-19 | 32 | 16 |
| XMC1302-Q024X0064 | PG-VQFN-24-19 | 64 | 16 |
| XMC1301-Q040F0008 | PG-VQFN-40-13 | 8 | 16 |
| XMC1301-Q040F0016 | PG-VQFN-40-13 | 16 | 16 |
| XMC1301-Q040F0032 | PG-VQFN-40-13 | 32 | 16 |
| XMC1302-Q040X0016 | PG-VQFN-40-13 | 16 | 16 |
| XMC1302-Q040X0032 | PG-VQFN-40-13 | 32 | 16 |
| XMC1302-Q040X0064 | PG-VQFN-40-13 | 64 | 16 |
| XMC1302-Q040X0128 | PG-VQFN-40-13 | 128 | 16 |
| XMC1302-Q040X0200 | PG-VQFN-40-13 | 200 | 16 |

## 1.3 Device Type Features

The following table lists the available features per device type.

**Table 2 Features of XMC1300 Device Types**[1)]

| Derivative | ADC channel | ACMP | BCCU | MATH |
|---|---|---|---|---|
| XMC1301-T016 | 11 | 2 | - | - |
| XMC1302-T016 | 11 | 2 | 1 | 1 |
| XMC1302-T028 | 14 | 3 | 1 | 1 |
| XMC1301-T038 | 16 | 3 | - | - |
| XMC1302-T038 | 16 | 3 | 1 | 1 |
| XMC1301-Q024 | 13 | 3 | - | - |
| XMC1302-Q024 | 13 | 3 | 1 | 1 |
| XMC1301-Q040 | 16 | 3 | - | - |
| XMC1302-Q040 | 16 | 3 | 1 | 1 |

1) Features that are not included in this table are available in all the derivatives

**Table 3 ADC Channels** [1)]

| Package | VADC0 G0 | VADC0 G1 |
|---|---|---|
| PG-TSSOP-16 | CH0..CH5 | CH0..CH4 |
| PG-TSSOP-28 | CH0..CH7 | CH0 .. CH4, CH7 |
| PG-TSSOP-38 | CH0..CH7 | CH0..CH7 |
| PG-VQFN-24 | CH0..CH7 | CH0..CH4 |
| PG-VQFN-40 | CH0..CH7 | CH0..CH7 |

1) Some pins in a package may be connected to more than one channel. For the detailed mapping see the Port I/O Function table.

## 1.4 Chip Identification Number

The Chip Identification Number allows software to identify the marking. It is a 8 words value with the most significant 7 words stored in Flash configuration sector 0 (CS0) at address location : 1000 $0F00_H$ (MSB) - 1000 $0F1B_H$ (LSB). The least significant word and most significant word of the Chip Identification Number are the value of registers DBGROMID and IDCHIP, respectively.

**Table 4 XMC1300 Chip Identification Number** (cont'd)

| Derivative | Value | Marking |
|---|---|---|
| XMC1302-Q040X0128 | 00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 $201ED083_H$ | AB |
| XMC1302-Q040X0200 | 00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 $201ED083_H$ | AB |

**Table 6 Package Pin Mapping** (cont'd)

| **Function** | **VQFN 40** | **TSSOP 38** | **TSSOP 28** | **VQFN 24** | **TSSOP 16** | **Pad Type** | **Notes** |
|---|---|---|---|---|---|---|---|
| P0.7 | 30 | 24 | 17 | 18 | 10 | STD_INOUT | |
| P0.8 | 33 | 27 | 18 | 19 | 11 | STD_INOUT | |
| P0.9 | 34 | 28 | 19 | 20 | 12 | STD_INOUT | |
| P0.10 | 35 | 29 | 20 | - | - | STD_INOUT | |
| P0.11 | 36 | 30 | - | - | - | STD_INOUT | |
| P0.12 | 37 | 31 | 21 | 21 | - | STD_INOUT | |
| P0.13 | 38 | 32 | 22 | 22 | - | STD_INOUT | |
| P0.14 | 39 | 33 | 23 | 23 | 13 | STD_INOUT | |
| P0.15 | 40 | 34 | 24 | 24 | 14 | STD_INOUT | |
| P1.0 | 22 | 16 | 12 | 14 | - | High Current | |
| P1.1 | 21 | 15 | 11 | 13 | - | High Current | |
| P1.2 | 20 | 14 | 10 | 12 | - | High Current | |
| P1.3 | 19 | 13 | 9 | 11 | - | High Current | |
| P1.4 | 18 | 12 | - | - | - | High Current | |
| P1.5 | 17 | 11 | - | - | - | High Current | |
| P1.6 | 16 | - | - | - | - | STD_INOUT | |
| P2.0 | 1 | 35 | 25 | 1 | 15 | STD_INOUT/AN | |

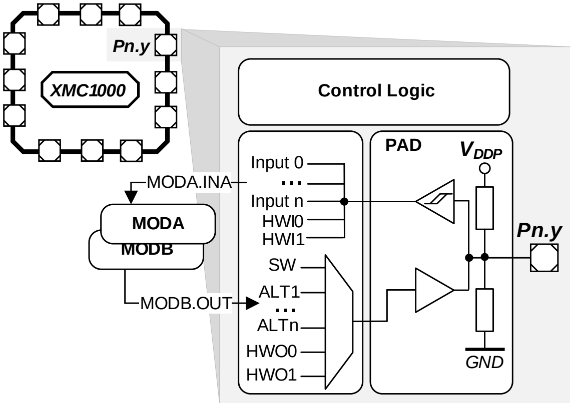


**Figure 9 Simplified Port Structure**

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOCR.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the **Port I/O Functions** table for the complete Port I/O function mapping.

## Table 9 Port I/O Functions

| **Function** | **Outputs** | | | | | | | **Inputs** | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **ALT1** | **ALT2** | **ALT3** | **ALT4** | **ALT5** | **ALT6** | **ALT7** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** |
| P0.0 | ERU0.PDOUT0 | | ERU0.GOUT0 | CCU40.OUT0 | CCU80.OUT00 | USIC0_CH0.SELO0 | USIC0_CH1.SELO0 | BCCU0.TRAPINB | CCU40.IN0C | | | USIC0_CH0.DX2A | USIC0_CH1.DX2A | | | | |
| P0.1 | ERU0.PDOUT1 | | ERU0.GOUT1 | CCU40.OUT1 | CCU80.OUT01 | BCCU0.OUT8 | SCU.VDROP | | CCU40.IN1C | | | | | | | | |
| P0.2 | ERU0.PDOUT2 | | ERU0.GOUT2 | CCU40.OUT2 | CCU80.OUT02 | VADC0.EMUX02 | CCU80.OUT10 | | CCU40.IN2C | | | | | | | | |
| P0.3 | ERU0.PDOUT3 | | ERU0.GOUT3 | CCU40.OUT3 | CCU80.OUT03 | VADC0.EMUX01 | CCU80.OUT11 | | CCU40.IN3C | | | | | | | | |
| P0.4 | BCCU0.OUT0 | | | CCU40.OUT1 | CCU80.OUT13 | VADC0.EMUX00 | WWDT.SERVICE_OUT | | CCU80.IN0B | | | | | | | | |
| P0.5 | BCCU0.OUT1 | | | CCU40.OUT0 | CCU80.OUT12 | ACMP2.OUT | CCU80.OUT01 | | CCU80.IN1B | | | | | | | | |
| P0.6 | BCCU0.OUT2 | | | CCU40.OUT0 | CCU80.OUT11 | USIC0_CH1.MCLKOUT | USIC0_CH1.DOUT0 | | CCU40.IN0B | | | USIC0_CH1.DX0C | | | | | |
| P0.7 | BCCU0.OUT3 | | | CCU40.OUT1 | CCU80.OUT10 | USIC0_CH0.SCLKOUT | USIC0_CH1.DOUT0 | | CCU40.IN1B | | | USIC0_CH0.DX1C | USIC0_CH1.DX0D | USIC0_CH1.DX1C | | | |
| P0.8 | BCCU0.OUT4 | | | CCU40.OUT2 | CCU80.OUT20 | USIC0_CH0.SCLKOUT | USIC0_CH1.SCLKOUT | | CCU40.IN2B | | | USIC0_CH0.DX1B | USIC0_CH1.DX1B | | | | |
| P0.9 | BCCU0.OUT5 | | | CCU40.OUT3 | CCU80.OUT21 | USIC0_CH0.SELO0 | USIC0_CH1.SELO0 | | CCU40.IN3B | | | USIC0_CH0.DX2B | USIC0_CH1.DX2B | | | | |
| P0.10 | BCCU0.OUT6 | | | ACMP0.OUT | CCU80.OUT22 | USIC0_CH0.SELO1 | USIC0_CH1.SELO1 | | CCU80.IN2B | | | USIC0_CH0.DX2C | USIC0_CH1.DX2C | | | | |
| P0.11 | BCCU0.OUT7 | | | USIC0_CH0.MCLKOUT | CCU80.OUT23 | USIC0_CH0.SELO2 | USIC0_CH1.SELO2 | | | | | USIC0_CH0.DX2D | USIC0_CH1.DX2D | | | | |
| P0.12 | BCCU0.OUT6 | | | | CCU80.OUT33 | USIC0_CH0.SELO3 | CCU80.OUT20 | BCCU0.TRAPINA | CCU40.IN0A | CCU40.IN1A | CCU40.IN2A | CCU40.IN3A | CCU80.IN0A | CCU80.IN1A | CCU80.IN2A | CCU80.IN3A | USIC0_CH0.DX2E |
| P0.13 | WWDT.SERVICE_OUT | | | | CCU80.OUT32 | USIC0_CH0.SELO4 | CCU80.OUT21 | | CCU80.IN3B | POSIF0.IN0B | | USIC0_CH0.DX2F | | | | | |

**Table 9 Port I/O Functions** (cont'd)

| Function | Outputs | | | | | | | Inputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **ALT1** | **ALT2** | **ALT3** | **ALT4** | **ALT5** | **ALT6** | **ALT7** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** | **Input** |
| P2.6 | | | | | | | | ACMP1.INN | VADC0.G0CH0 | | ERU0.2A1 | USIC0_CH0.DX3E | USIC0_CH0.DX4E | USIC0_CH1.DX5D | ORC4.AIN | | |
| P2.7 | | | | | | | | ACMP1.INP | VADC0.G1CH1 | | ERU0.3A1 | USIC0_CH0.DX5C | USIC0_CH1.DX3D | USIC0_CH1.DX4D | ORC5.AIN | | |
| P2.8 | | | | | | | | ACMP0.INN | VADC0.G0CH1 | VADC0.G1CH0 | ERU0.3B1 | USIC0_CH0.DX3D | USIC0_CH0.DX4D | USIC0_CH1.DX5C | ORC6.AIN | | |
| P2.9 | | | | | | | | ACMP0.INP | VADC0.G0CH2 | VADC0.G1CH4 | ERU0.3B0 | USIC0_CH0.DX5A | USIC0_CH1.DX3B | USIC0_CH1.DX4B | ORC7.AIN | | |
| P2.10 | ERU0.PDOUT1 | CCU40.OUT2 | ERU0.GOUT1 | | CCU80.OUT30 | ACMP0.OUT | USIC0_CH1.DOUT0 | | VADC0.G0CH3 | VADC0.G1CH2 | ERU0.2B0 | USIC0_CH0.DX3C | USIC0_CH0.DX4C | USIC0_CH1.DX0F | | | |
| P2.11 | ERU0.PDOUT0 | CCU40.OUT3 | ERU0.GOUT0 | | CCU80.OUT31 | USIC0_CH1.SCLKOUT | USIC0_CH1.DOUT0 | ACMP.REF | VADC0.G0CH4 | VADC0.G1CH3 | ERU0.2B1 | USIC0_CH1.DX0E | USIC0_CH1.DX1E | | | | |

## Table 10 Hardware Controlled I/O Functions (cont'd)

| Function | Outputs | | Inputs | | Pull Control | | | |
|---|---|---|---|---|---|---|---|---|
| | HWO0 | HWO1 | HWI0 | HWI1 | HW0_PD | HW0_PU | HW1_PD | HW1_PU |
| P2.6 | | | | | $\overline{\text{BCCU0.OUT2}}$ | BCCU0.OUT2 | $\overline{\text{CCU40.OUT3}}$ | CCU40.OUT3 |
| P2.7 | | | | | $\overline{\text{BCCU0.OUT8}}$ | BCCU0.OUT8 | $\overline{\text{CCU40.OUT3}}$ | CCU40.OUT3 |
| P2.8 | | | | | $\overline{\text{BCCU0.OUT1}}$ | BCCU0.OUT1 | $\overline{\text{CCU40.OUT2}}$ | CCU40.OUT2 |
| P2.9 | | | | | $\overline{\text{BCCU0.OUT7}}$ | BCCU0.OUT7 | $\overline{\text{CCU40.OUT2}}$ | CCU40.OUT2 |
| P2.10 | | | | | $\overline{\text{BCCU0.OUT4}}$ | BCCU0.OUT4 | | |
| P2.11 | | | | | $\overline{\text{BCCU0.OUT5}}$ | BCCU0.OUT5 | | |

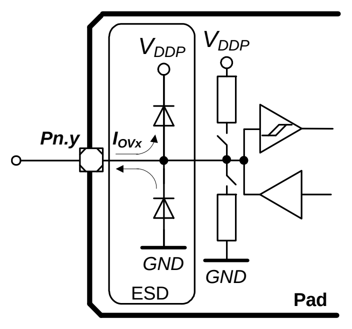


Figure 10 Input Overload Current via ESD structures

**Table 13** and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

**Table 13 PN-Junction Characterisitics for positive Overload**

| **Pad Type** | $I_{OV}$ **= 5 mA** |
|---|---|
| Standard, High-current, AN/DIG_IN | $V_{IN} = V_{DDP} + 0.5$ V<br>$V_{AIN} = V_{DDP} + 0.5$ V<br>$V_{AREF} = V_{DDP} + 0.5$ V |
| P2.[1,2,6:9,11] | $V_{INP2} = V_{DDP} + 0.3$ V |

**Table 14 PN-Junction Characterisitics for negative Overload**

| **Pad Type** | $I_{OV}$ **= 5 mA** |
|---|---|
| Standard, High-current, AN/DIG_IN | $V_{IN} = V_{SS} - 0.5$ V<br>$V_{AIN} = V_{SS} - 0.5$ V<br>$V_{AREF} = V_{SS} - 0.5$ V |
| P2.[1,2,6:9,11] | $V_{INP2} = V_{SS} - 0.3$ V |

**Table 16 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| **Parameter** | **Symbol** | | **Limit Values** | | **Unit** | **Test Conditions** |
|---|---|---|---|---|---|---|
| | | | **Min.** | **Max.** | | |
| Input Hysteresis[8] | $HYS$ | CC | 0.08 × $V_{DDP}$ | – | V | CMOS Mode (5 V), Standard Hysteresis |
| | | | 0.03 × $V_{DDP}$ | – | V | CMOS Mode (3.3 V), Standard Hysteresis |
| | | | 0.02 × $V_{DDP}$ | – | V | CMOS Mode (2.2 V), Standard Hysteresis |
| | | | 0.5 × $V_{DDP}$ | 0.75 × $V_{DDP}$ | V | CMOS Mode(5 V), Large Hysteresis |
| | | | 0.4 × $V_{DDP}$ | 0.75 × $V_{DDP}$ | V | CMOS Mode(3.3 V), Large Hysteresis |
| | | | 0.2 × $V_{DDP}$ | 0.65 × $V_{DDP}$ | V | CMOS Mode(2.2 V), Large Hysteresis |
| Pin capacitance (digital inputs/outputs) | $C_{IO}$ | CC | – | 10 | pF | |
| Pull-up resistor on port pins | $R_{PUP}$ | CC | 20 | 50 | kohm | $V_{IN} = V_{SSP}$ |
| Pull-down resistor on port pins | $R_{PDP}$ | CC | 20 | 50 | kohm | $V_{IN} = V_{DDP}$ |
| Input leakage current[9] | $I_{OZP}$ | CC | -1 | 1 | µA | $0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | [10] |
| Maximum current per pin (excluding P1, $V_{DDP}$ and $V_{SS}$) | $I_{MP}$ | SR | -10 | 11 | mA | – |
| Maximum current per high currrent pins | $I_{MP1A}$ | SR | -10 | 50 | mA | – |
| Maximum current into $V_{DDP}$ (TSSOP16, VQFN24) | $I_{MVDD1}$ | SR | – | 130 | mA | [18] |
| Maximum current into $V_{DDP}$ (TSSOP38, VQFN40) | $I_{MVDD2}$ | SR | – | 260 | mA | [18] |

### 3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

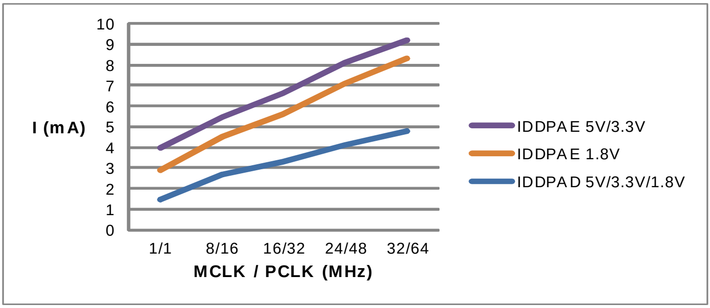
Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 21 Power Supply Parameters; $V_{DDP}$ = 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Active mode current<br>Peripherals enabled<br>$f_{MCLK}$ / $f_{PCLK}$ in MHz[2] | $I_{DDPAE}$ CC | – | 9.2 | 12 | mA | 32 / 64 |
| | | – | 8.1 | - | mA | 24 / 48 |
| | | – | 6.6 | - | mA | 16 / 32 |
| | | – | 5.5 | - | mA | 8 / 16 |
| | | – | 4 | - | mA | 1 / 1 |
| Active mode current<br>Peripherals disabled<br>$f_{MCLK}$ / $f_{PCLK}$ in MHz[3] | $I_{DDPAD}$ CC | – | 4.8 | - | mA | 32 / 64 |
| | | – | 4.1 | - | mA | 24 / 48 |
| | | – | 3.3 | - | mA | 16 / 32 |
| | | – | 2.7 | - | mA | 8 / 16 |
| | | – | 1.5 | - | mA | 1 / 1 |
| Active mode current<br>Code execution from RAM<br>Flash is powered down<br>$f_{MCLK}$ / $f_{PCLK}$ in MHz | $I_{DDPAR}$ CC | – | 7.3 | - | mA | 32 / 64 |
| | | – | 6.3 | - | mA | 24 / 48 |
| | | – | 5.2 | - | mA | 16 / 32 |
| | | – | 4.2 | - | mA | 8 / 16 |
| | | – | 3.3 | - | mA | 1 / 1 |
| Sleep mode current<br>Peripherals clock enabled<br>$f_{MCLK}$ / $f_{PCLK}$ in MHz[4] | $I_{DDPSE}$ CC | – | 6.6 | - | mA | 32 / 64 |
| | | | 5.8 | - | mA | 24 / 48 |
| | | | 5.1 | - | mA | 16 / 32 |
| | | | 4.4 | - | mA | 8 / 16 |
| | | | 3.7 | - | mA | 1 / 1 |

**Figure 14** shows typical graphs for active mode supply current for $V_{DDP}$ = 5V, $V_{DDP}$ = 3.3V, $V_{DDP}$ = 1.8V across different clock frequencies.



Condition:
1. TA = +25° C

**Figure 14** Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current $I_{DDPA}$ over supply voltage $V_{DDP}$ for different clock frequencies

## 3.2.7 Flash Memory Parameters

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 23 Flash Memory Parameters**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Erase Time per page / sector | $t_{ERASE}$ CC | 6.8 | 7.1 | 7.6 | ms | |
| Program time per block | $t_{PSER}$ CC | 102 | 152 | 204 | µs | |
| Wake-Up time | $t_{WU}$ CC | – | 32.2 | – | µs | |
| Read time per word | $t_a$ CC | – | 50 | – | ns | |
| Data Retention Time | $t_{RET}$ CC | 10 | – | – | years | Max. 100 erase / program cycles |
| Flash Wait States 1) | $N_{WSFLASH}$ CC | 0 | 0 | 0 | | $f_{MCLK}$ = 8 MHz |
| | | 0 | 1 | 1 | | $f_{MCLK}$ = 16 MHz |
| | | 1 | 1.3 | 2 | | $f_{MCLK}$ = 32 MHz |
| Fixed Flash Wait States configured in bit NVM_NVMCONF.WS | $N_{FWSFLASH}$ SR | 0 | 0 | 1 | | NVM_CONFIG1.FIXWS = $1_B$, $f_{MCLK} \le$ 16 MHz |
| | | 1 | 1 | 1 | | NVM_CONFIG1.FIXWS = $1_B$, 16 MHz < $f_{MCLK} \le$ 32 MHz |
| Erase Cycles | $N_{ECYC}$ CC | – | – | $5*10^4$ | cycles | Sum of page and sector erase cycles |
| Total Erase Cycles | $N_{TECYC}$ CC | – | – | $2*10^6$ | cycles | |

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

### 3.3.5 SPD Timing Requirements

The optimum SPD decision time between $0_B$ and $1_B$ is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

**Table 28 Optimum Number of Sample Clocks for SPD**

| Sample Freq. | Sampling Factor | Sample Clocks $0_B$ | Sample Clocks $1_B$ | Effective Decision Time[1] | Remark |
|---|---|---|---|---|---|
| 8 MHz | 4 | 1 to 5 | 6 to 12 | 0.69 µs | The other closest option (0.81 µs) for the effective decision time is less robust. |

[1] Nominal sample frequency period multiplied with 0.5 + (max. number of $0_B$ sample clocks)

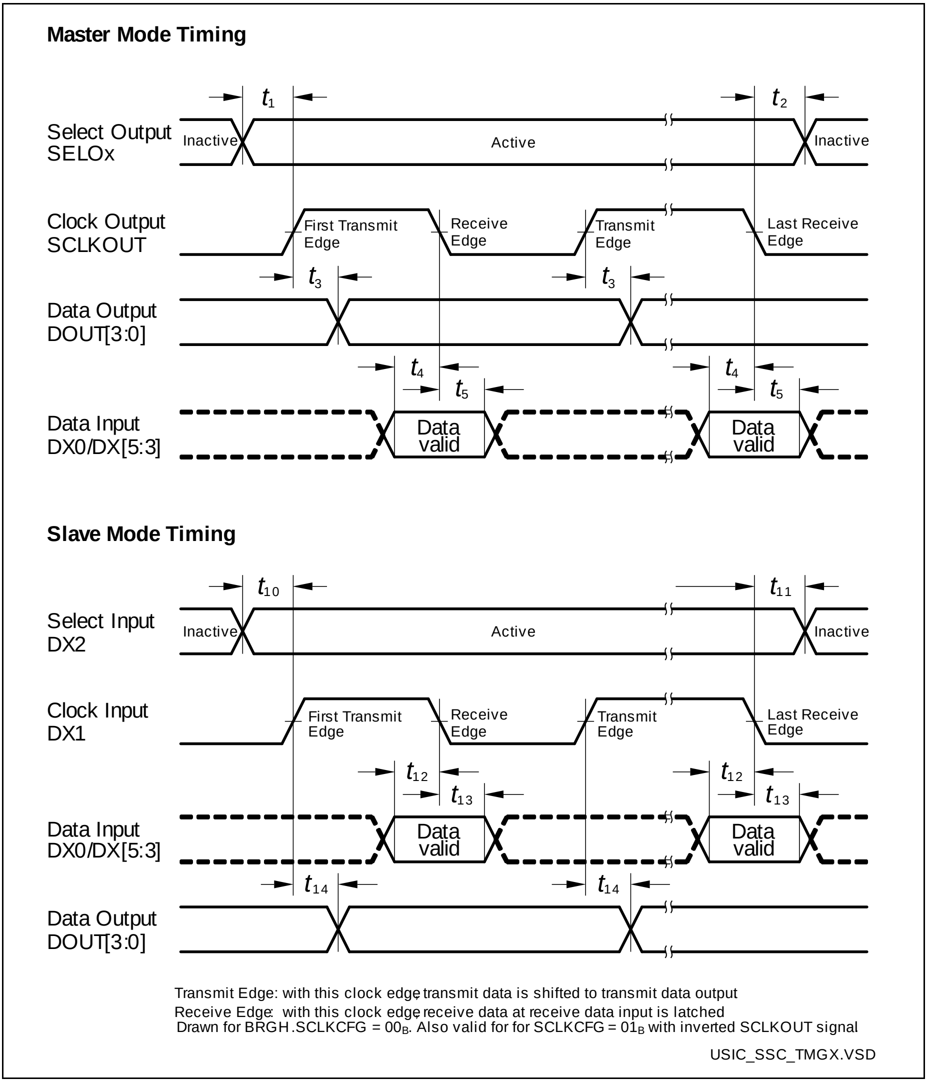
For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

**Table 30 USIC SSC Slave Mode Timing**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| DX1 slave clock period | $t_{\mathrm{CLK}}$ | SR | 125 | – | – | ns | |
| Select input DX2 setup to first clock input DX1 transmit edge[1] | $t_{10}$ | SR | 10 | – | – | ns | |
| Select input DX2 hold after last clock input DX1 receive edge[1] | $t_{11}$ | SR | 10 | – | – | ns | |
| Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1] | $t_{12}$ | SR | 10 | – | – | ns | |
| Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1] | $t_{13}$ | SR | 10 | – | – | ns | |
| Data output DOUT[3:0] valid time | $t_{14}$ | CC | - | – | 80 | ns | |

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).



Transmit Edge: with this clock edge transmit data is shifted to transmit data output
Receive Edge: with this clock edge receive data at receive data input is latched
Drawn for BRGH.SCLKCFG = $00_B$. Also valid for for SCLKCFG = $01_B$ with inverted SCLKOUT signal

**Figure 22 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

**Table 32 USIC IIC Fast Mode Timing**[1)]

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Fall time of both SDA and SCL | $t_1$ CC/SR | 20 + 0.1*$C_b$ [2)] | - | 300 | ns | |
| Rise time of both SDA and SCL | $t_2$ CC/SR | 20 + 0.1*$C_b$ | - | 300 | ns | |
| Data hold time | $t_3$ CC/SR | 0 | - | - | µs | |
| Data set-up time | $t_4$ CC/SR | 100 | - | - | ns | |
| LOW period of SCL clock | $t_5$ CC/SR | 1.3 | - | - | µs | |
| HIGH period of SCL clock | $t_6$ CC/SR | 0.6 | - | - | µs | |
| Hold time for (repeated) START condition | $t_7$ CC/SR | 0.6 | - | - | µs | |
| Set-up time for repeated START condition | $t_8$ CC/SR | 0.6 | - | - | µs | |
| Set-up time for STOP condition | $t_9$ CC/SR | 0.6 | - | - | µs | |
| Bus free time between a STOP and START condition | $t_{10}$ CC/SR | 1.3 | - | - | µs | |
| Capacitive load for each bus line | $C_b$ SR | - | - | 400 | pF | |

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximalely 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) $C_b$ refers to the total capacitance of one bus line in pF.

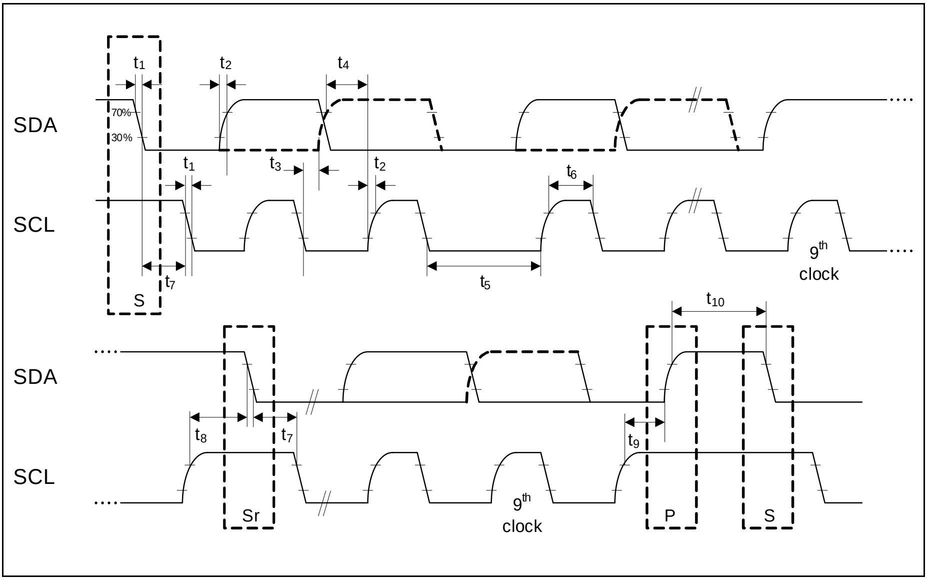


**Figure 23** USIC IIC Stand and Fast Mode Timing

### 3.3.6.3 Inter-IC Sound (IIS) Interface Timing

The following parameters are applicable for a USIC channel operated in IIS mode.

*Note: Operating Conditions apply.*

**Table 33** USIC IIS Master Transmitter Timing

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Clock period | $t_1$ CC | $2/f_{\mathrm{MCLK}}$ | - | - | ns | $V_{\mathrm{DDP}} \geq 3$ V |
| | | $4/f_{\mathrm{MCLK}}$ | - | - | ns | $V_{\mathrm{DDP}} < 3$ V |
| Clock HIGH | $t_2$ CC | 0.35 x $t_{\mathrm{1min}}$ | - | - | ns | |
| Clock Low | $t_3$ CC | 0.35 x $t_{\mathrm{1min}}$ | - | - | ns | |
| Hold time | $t_4$ CC | 0 | - | - | ns | |
| Clock rise time | $t_5$ CC | - | - | 0.15 x $t_{\mathrm{1min}}$ | ns | |