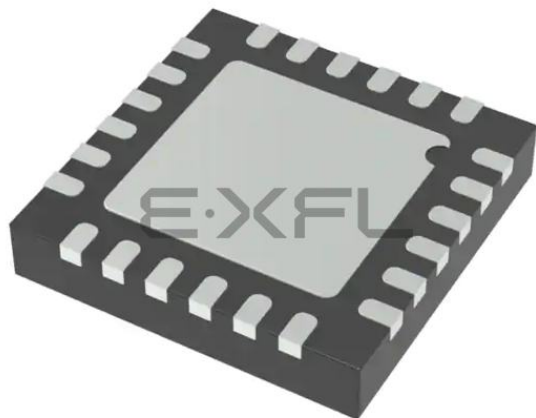




Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	18
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 13x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-24-19
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302q024f0032abxuma1

5	Quality Declaration	77
----------	----------------------------	-----------

Table 4 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 _H	AB
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1301-T016F0032	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 _H	AB
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00003000 201ED083 _H	AB
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1302-T028X0016	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 _H	AB
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1301-T038X0032	00013013 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1301-T038F0064	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00011000 201ED083 _H	AB
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 _H	AB

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

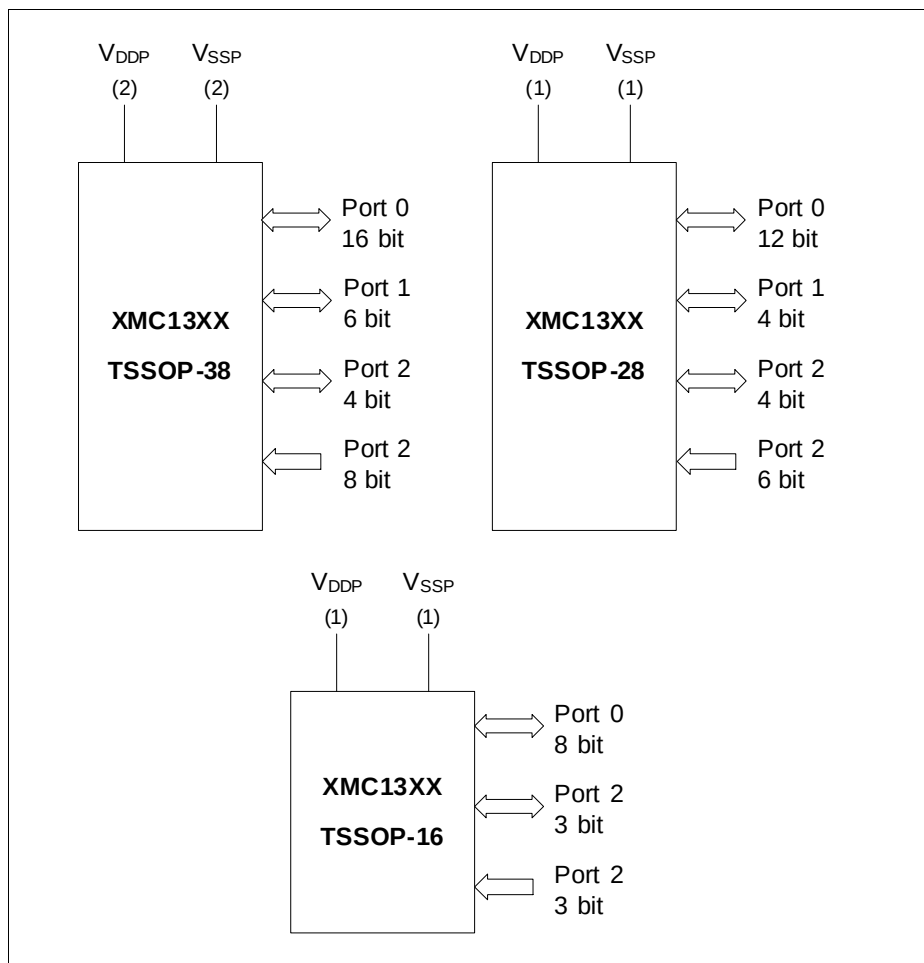


Figure 2 XMC1300 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

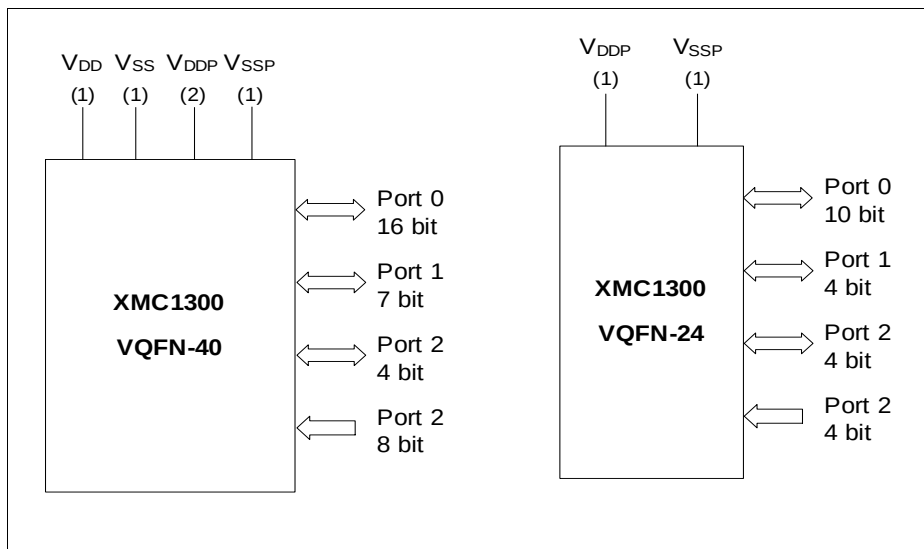


Figure 3 XMC1300 Logic Symbol for VQFN-24 and VQFN-40

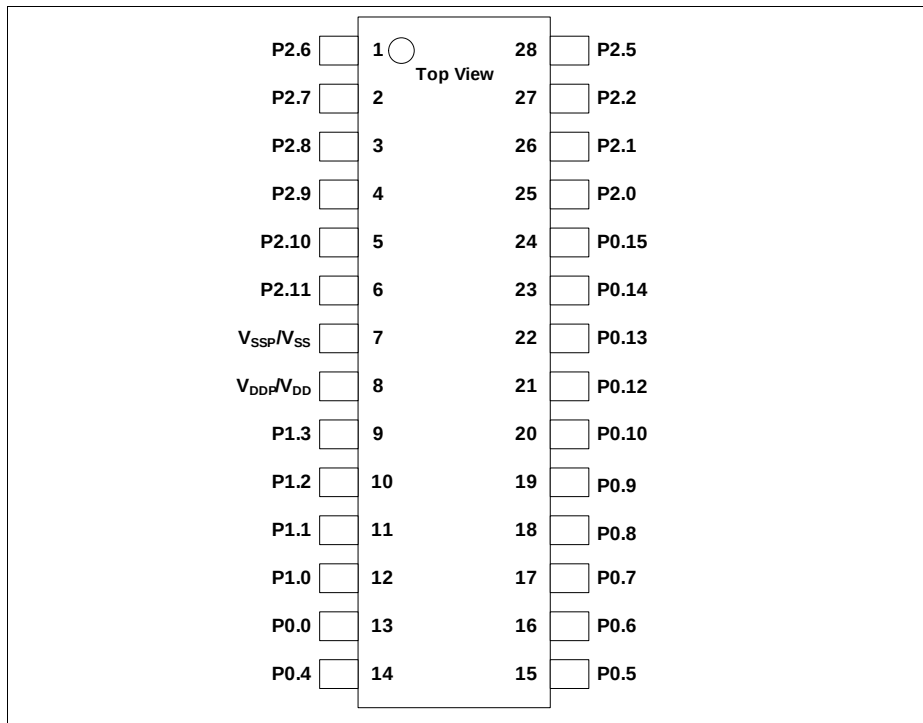


Figure 5 XMC1300 PG-TSSOP-28 Pin Configuration (top view)

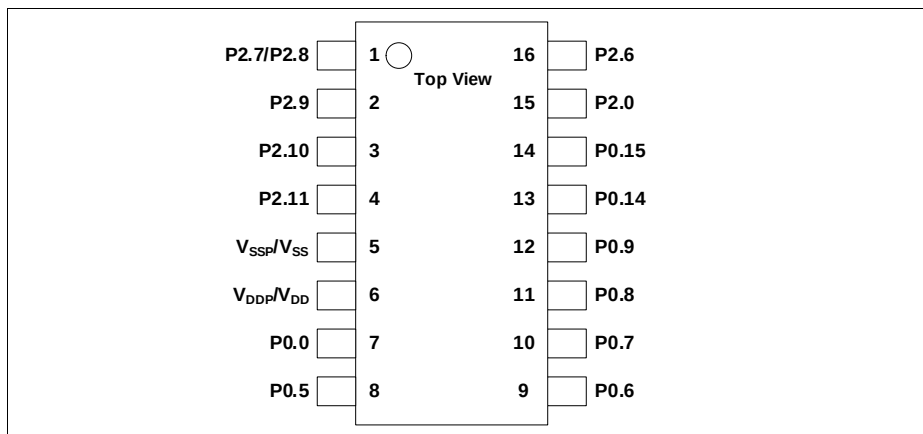


Figure 6 XMC1300 PG-TSSOP-16 Pin Configuration (top view)

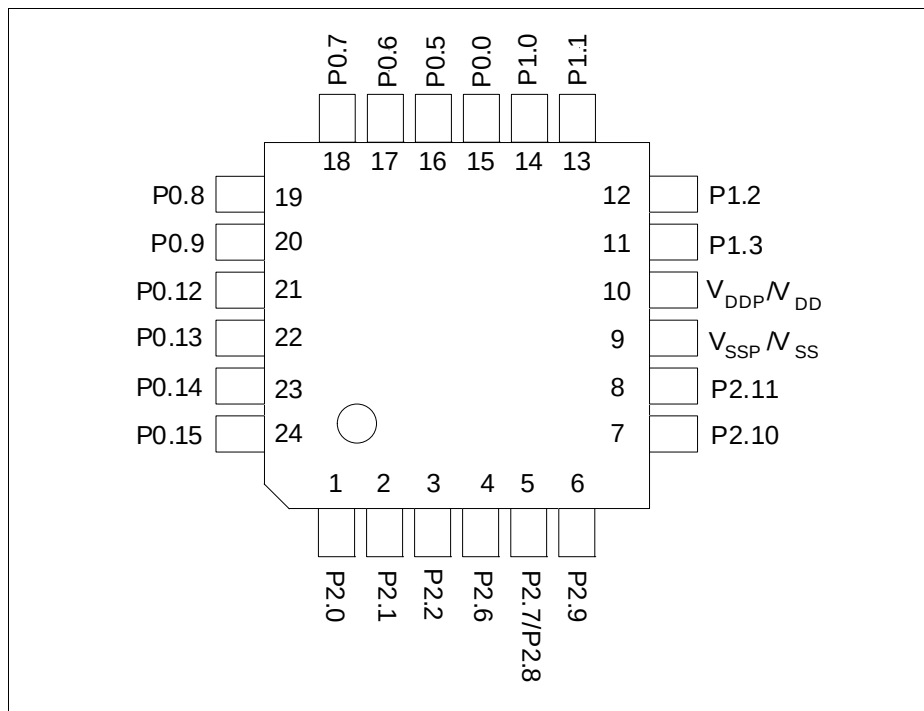


Figure 7 XMC1300 PG-VQFN-24 Pin Configuration (top view)

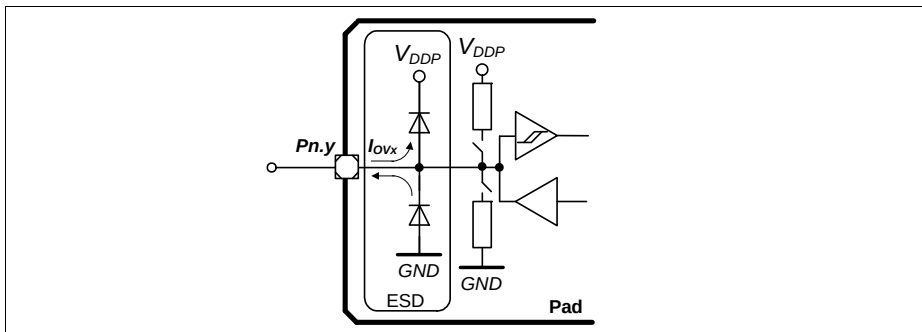


Figure 10 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characteristics for positive Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5 \text{ V}$ $V_{AIN} = V_{DDP} + 0.5 \text{ V}$ $V_{AREF} = V_{DDP} + 0.5 \text{ V}$
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP} + 0.3 \text{ V}$

Table 14 PN-Junction Characteristics for negative Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5 \text{ V}$ $V_{AIN} = V_{SS} - 0.5 \text{ V}$ $V_{AREF} = V_{SS} - 0.5 \text{ V}$
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS} - 0.3 \text{ V}$

Electrical Parameters
Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	—	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	—	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ¹⁸⁾
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	$0.85 \times V_{DDP}$	—	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ¹⁸⁾
Rise time on High Current Pad ¹⁾	t_{HCPR}	CC	—	9	ns	50 pF @ 5 V ²⁾
			—	12	ns	50 pF @ 3.3 V ³⁾
			—	25	ns	50 pF @ 1.8 V ⁴⁾
Fall time on High Current Pad ¹⁾	t_{HCPF}	CC	—	9	ns	50 pF @ 5 V ²⁾
			—	12	ns	50 pF @ 3.3 V ³⁾
			—	25	ns	50 pF @ 1.8 V ⁴⁾
Rise time on Standard Pad ¹⁾	t_R	CC	—	12	ns	50 pF @ 5 V ⁵⁾
			—	15	ns	50 pF @ 3.3 V ⁶⁾
			—	31	ns	50 pF @ 1.8 V ⁷⁾
Fall time on Standard Pad ¹⁾	t_F	CC	—	12	ns	50 pF @ 5 V ⁵⁾
			—	15	ns	50 pF @ 3.3 V ⁶⁾
			—	31	ns	50 pF @ 1.8 V ⁷⁾

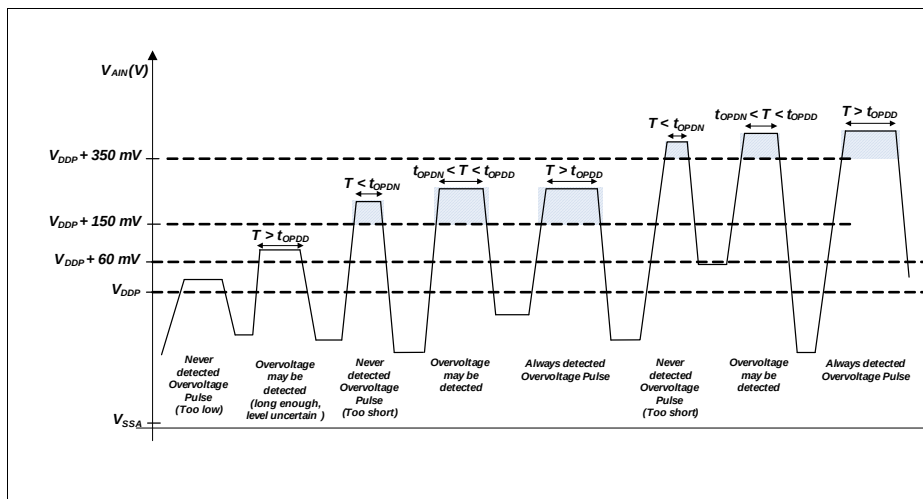


Figure 13 ORC Detection Ranges

Electrical Parameters

Figure 15 shows typical graphs for sleep mode current for $V_{DDP} = 5V$, $V_{DDP} = 3.3V$, $V_{DDP} = 1.8V$ across different clock frequencies.

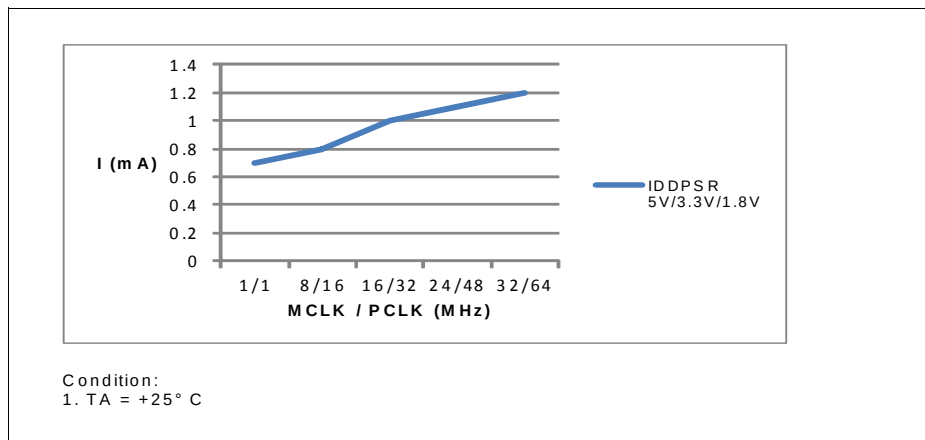


Figure 15 Sleep mode, peripherals clocks disabled, Flash powered down:
Supply current I_{DDPSR} over supply voltage V_{DDP} for different clock frequencies

Electrical Parameters

Table 22 provides the active current consumption of some modules operating at 5 V power supply at 25° C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 22 Typical Active Current Consumption

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP ¹⁾
VADC and SHS	I_{ADCDDC}	3.4	mA	Set CGATCLR0.VADC to 1 ²⁾
USIC0	$I_{USIC0DDC}$	0.87	mA	Set CGATCLR0.USIC0 to 1 ³⁾
CCU40	$I_{CCU40DDC}$	0.94	mA	Set CGATCLR0.CCU40 to 1 ⁴⁾
CCU80	$I_{CCU80DDC}$	0.42	mA	Set CGATCLR0.CCU80 to 1 ⁵⁾
POSIF0	$I_{PIF0DDC}$	0.26	mA	Set CGATCLR0.POSIF0 to 1 ⁶⁾
BCCU0	$I_{BCCU0DDC}$	0.24	mA	Set CGATCLR0.BCCU0 to 1 ⁷⁾
MATH	$I_{MATHDDC}$	0.35	mA	Set CGATCLR0.MATH to 1 ⁸⁾
WDT	I_{WDTDDC}	0.03	mA	Set CGATCLR0.WDT to 1 ⁹⁾
RTC	I_{RTCDDC}	0.01	mA	Set CGATCLR0.RTC to 1 ¹⁰⁾

- 1) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
- 2) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode
- 3) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms
- 4) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle
- 5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU8 slice with PWM frequency at 1500Hz and a period match interrupt used to toggle duty cycle between 10% and 90%
- 6) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, hall sensor mode
- 7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s
- 8) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11
- 9) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s
- 10) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page / sector	$t_{\text{ERASE CC}}$	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSER CC}}$	102	152	204	μs	
Wake-Up time	$t_{\text{WU CC}}$	–	32.2	–	μs	
Read time per word	$t_{\text{a CC}}$	–	50	–	ns	
Data Retention Time	$t_{\text{RET CC}}$	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States ¹⁾	$N_{\text{WSFLASH CC}}$	0	0	0		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1	1		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	1.3	2		$f_{\text{MCLK}} = 32 \text{ MHz}$
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{\text{FWSFLASH SR}}$	0	0	1		NVM_CONFIG1.FI XWS = 1 _B , $f_{\text{MCLK}} \leq 16 \text{ MHz}$
		1	1	1		NVM_CONFIG1.FI XWS = 1 _B , $16 \text{ MHz} < f_{\text{MCLK}} \leq 32 \text{ MHz}$
Erase Cycles	$N_{\text{ECCY CC}}$	–	–	$5 \cdot 10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	$N_{\text{TECCY CC}}$	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.3 On-Chip Oscillator Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	–	64	–	MHz	under nominal conditions ¹⁾ after trimming
Accuracy ²⁾	Δf_{LT} CC	-1.7	–	3.4	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature ($T_A = 0\text{ °C}$ to 85 °C)
		-3.9	–	4.0	%	with respect to $f_{\text{NOM}}(\text{typ})$, over temperature ($T_A = -40\text{ °C}$ to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and $T_A = +25\text{ °C}$.

2) The accuracy can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

3.3.6 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 29 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK} CC	62.5	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3 CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	0	–	–	ns	

Table 30 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	125	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge ¹⁾	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge ¹⁾	t_{11}	SR	10	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge ¹⁾	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge ¹⁾	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

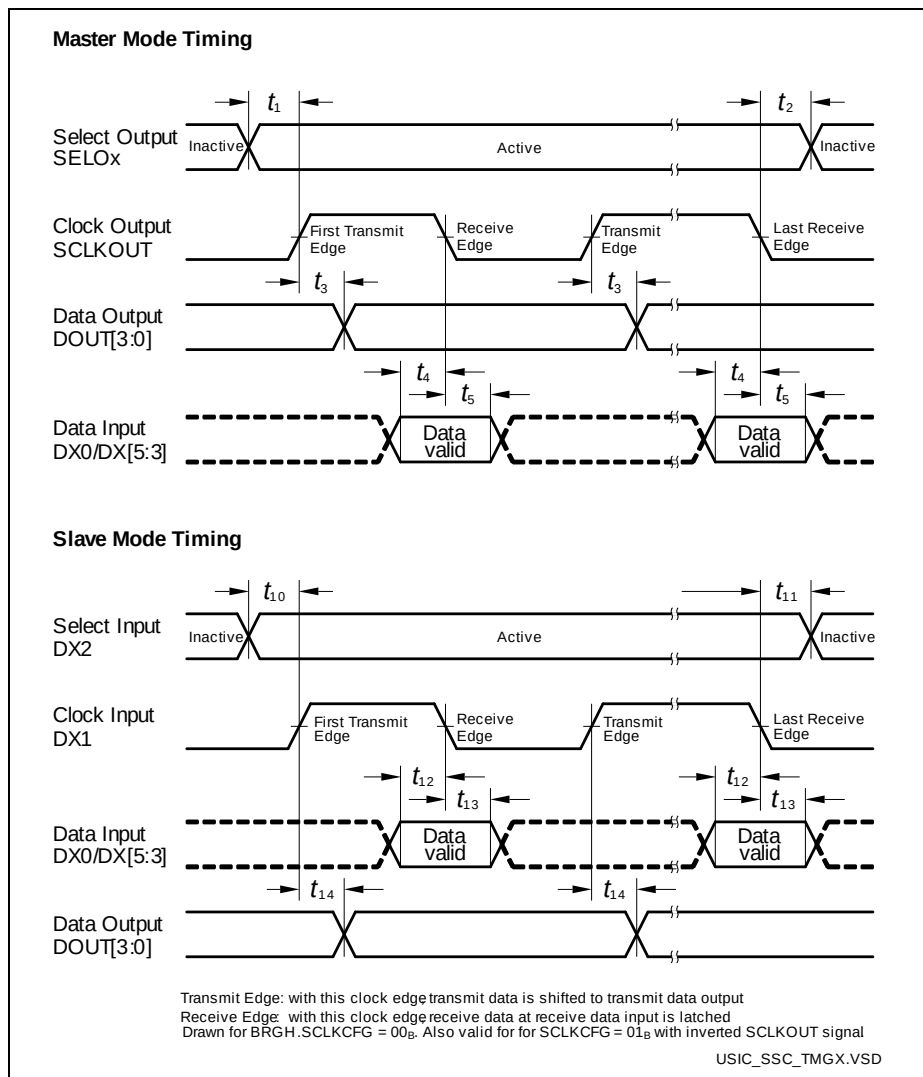


Figure 22 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

3.3.6.2 Inter-IC (IIC) Interface Timing

The following parameters are applicable for a USIC channel operated in IIC mode.

Note: Operating Conditions apply.

Table 31 USIC IIC Standard Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	-	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	-	-	1000	ns	
Data hold time	t_3 CC/SR	0	-	-	μs	
Data set-up time	t_4 CC/SR	250	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	4.7	-	-	μs	
HIGH period of SCL clock	t_6 CC/SR	4.0	-	-	μs	
Hold time for (repeated) START condition	t_7 CC/SR	4.0	-	-	μs	
Set-up time for repeated START condition	t_8 CC/SR	4.7	-	-	μs	
Set-up time for STOP condition	t_9 CC/SR	4.0	-	-	μs	
Bus free time between a STOP and START condition	t_{10} CC/SR	4.7	-	-	μs	
Capacitive load for each bus line	C_b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

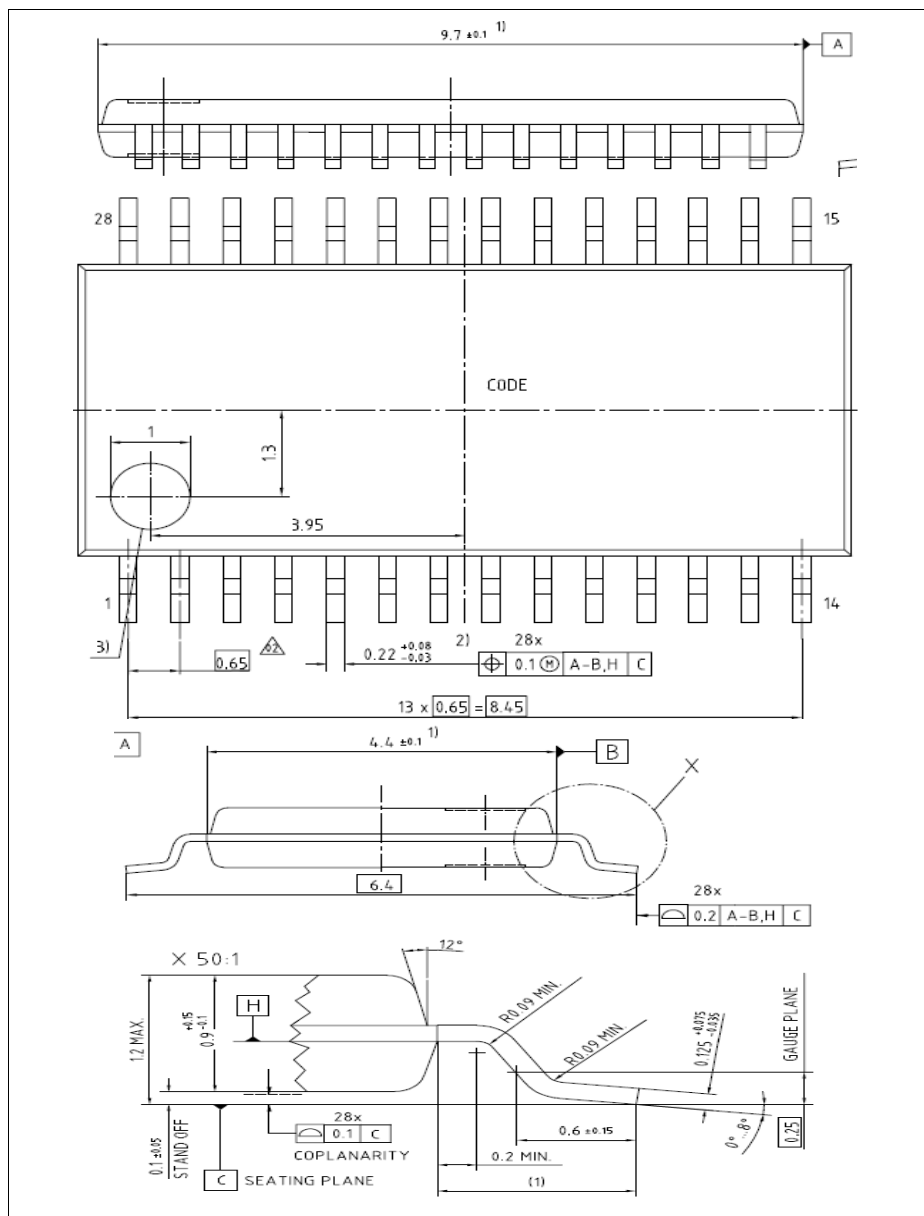


Figure 27 PG-TSSOP-28-16

5 Quality Declaration

Table 36 shows the characteristics of the quality parameters in the XMC1300.

Table 36 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D

www.infineon.com