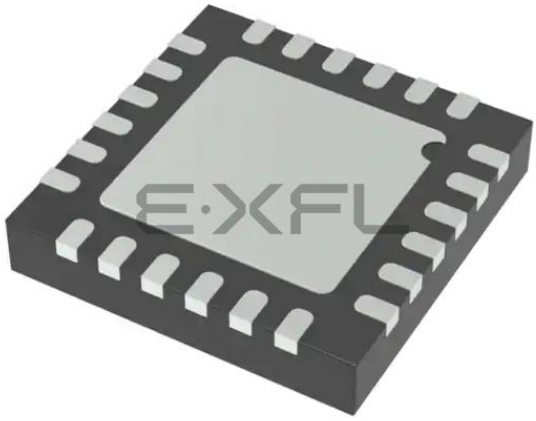
# Infineon Technologies - XMC1302Q024X0064ABXUMA1 Datasheet



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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0 |
| Core Size | 32-Bit Single-Core |
| Speed | 32MHz |
| Connectivity | I²C, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 18 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 16K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 5.5V |
| Data Converters | A/D 13x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 105°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-VFQFN Exposed Pad |
| Supplier Device Package | PG-VQFN-24-19 |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302q024x0064abxuma1 |

# XMC1300 AB-Step

Microcontroller Series
for Industrial Applications

XMC1000 Family

ARM® Cortex®-M0
32-bit processor core

## Data Sheet

V1.9 2017-03

Microcontrollers

**XMC1300 Data Sheet**

**Revision History: V1.9 2017-03**

| Previous Version: V1.8 2016-09 | |
|---|---|
| Page | Subjects |
| **Page 10**, **Page 12** | Add marking option for XMC1301-T038X0032. |

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**mcdocu.comments@infineon.com**

- Configurable pad hysteresis

**On-Chip Debug Support**

- Support for debug features: 4 breakpoints, 2 watchpoints
- Various interfaces: ARM serial wire debug (SWD), single pin debug (SPD)

## 1.1 Ordering Information

The ordering code for an Infineon microcontroller provides an exact reference to a specific product. The code “XMC1<DDD>-<Z><PPP><T><FFFF>” identifies:

- <DDD> the derivatives function set
- <Z> the package variant
  - T: TSSOP
  - Q: VQFN
- <PPP> package pin count
- <T> the temperature range:
  - F: -40°C to 85°C
  - X: -40°C to 105°C
- <FFFF> the Flash memory size.

For ordering codes for the XMC1300 please contact your sales representative or local distributor.

This document describes several derivatives of the XMC1300 series, some descriptions may not apply to a specific product. Please see **Table 1**.

For simplicity the term **XMC1300** is used for all derivatives throughout this document.

## 1.2 Device Types

These device types are available and can be ordered through Infineon’s direct and/or distribution channels.

**Table 1 Synopsis of XMC1300 Device Types**

| Derivative | Package | Flash Kbytes | SRAM Kbytes |
|---|---|---|---|
| XMC1301-T016F0008 | PG-TSSOP-16-8 | 8 | 16 |
| XMC1301-T016F0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1301-T016F0032 | PG-TSSOP-16-8 | 32 | 16 |
| XMC1301-T016X0008 | PG-TSSOP-16-8 | 8 | 16 |
| XMC1301-T016X0016 | PG-TSSOP-16-8 | 16 | 16 |
| XMC1302-T016X0008 | PG-TSSOP-16-8 | 8 | 16 |

## Table 9 Port I/O Functions (cont'd)

| Function | Outputs | | | | | | | Inputs | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | ALT1 | ALT2 | ALT3 | ALT4 | ALT5 | ALT6 | ALT7 | Input | Input | Input | Input | Input | Input | Input | Input | Input | Input |
| P0.14 | BCCU0.OUT7 | | | | CCU80.OUT31 | USIC0_CH0.DOUT0 | USIC0_CH0.SCLKOUT | | | POSIF0.IN1B | | USIC0_CH0.DX0A | USIC0_CH0.DX1A | | | | |
| P0.15 | BCCU0.OUT8 | | | | CCU80.OUT30 | USIC0_CH0.DOUT0 | USIC0_CH1.MCLKOUT | | | POSIF0.IN2B | | USIC0_CH0.DX0B | | | | | |
| P1.0 | BCCU0.OUT0 | CCU40.OUT0 | | | CCU80.OUT00 | ACMP1.OUT | USIC0_CH0.DOUT0 | | | POSIF0.IN2A | | USIC0_CH0.DX0C | | | | | |
| P1.1 | VADC0.EMUX00 | CCU40.OUT1 | | | CCU80.OUT01 | USIC0_CH0.DOUT0 | USIC0_CH1.SELO0 | | | POSIF0.IN1A | | USIC0_CH0.DX0D | USIC0_CH0.DX1D | USIC0_CH1.DX2E | | | |
| P1.2 | VADC0.EMUX01 | CCU40.OUT2 | | | CCU80.OUT10 | ACMP2.OUT | USIC0_CH1.DOUT0 | | | POSIF0.IN0A | | USIC0_CH1.DX0B | | | | | |
| P1.3 | VADC0.EMUX02 | CCU40.OUT3 | | | CCU80.OUT11 | USIC0_CH1.SCLKOUT | USIC0_CH1.DOUT0 | | | | | USIC0_CH1.DX0A | USIC0_CH1.DX1A | | | | |
| P1.4 | VADC0.EMUX10 | USIC0_CH1.SCLKOUT | | | CCU80.OUT20 | USIC0_CH0.SELO0 | USIC0_CH1.SELO1 | | | | | USIC0_CH0.DX5E | USIC0_CH1.DX5E | | | | |
| P1.5 | VADC0.EMUX11 | USIC0_CH0.DOUT0 | | BCCU0.OUT1 | CCU80.OUT21 | USIC0_CH0.SELO1 | USIC0_CH1.SELO2 | | | | | USIC0_CH1.DX5F | | | | | |
| P1.6 | VADC0.EMUX12 | USIC0_CH1.DOUT0 | | USIC0_CH0.SCLKOUT | BCCU0.OUT2 | USIC0_CH0.SELO2 | USIC0_CH1.SELO3 | | | USIC0_CH0.DX5F | | | | | | | |
| P2.0 | ERU0.PDOUT3 | CCU40.OUT0 | ERU0.GOUT3 | | CCU80.OUT20 | USIC0_CH0.DOUT0 | USIC0_CH0.SCLKOUT | | VADC0.G0CH5 | | ERU0.0B0 | USIC0_CH0.DX0E | USIC0_CH0.DX1E | USIC0_CH1.DX2F | | | |
| P2.1 | ERU0.PDOUT2 | CCU40.OUT1 | ERU0.GOUT2 | | CCU80.OUT21 | USIC0_CH0.DOUT0 | USIC0_CH1.SCLKOUT | ACMP2.INP | VADC0.G0CH6 | | ERU0.1B0 | USIC0_CH0.DX0F | USIC0_CH1.DX3A | USIC0_CH1.DX4A | | | |
| P2.2 | | | | | | | | ACMP2.INN | VADC0.G0CH7 | | ERU0.0B1 | USIC0_CH0.DX3A | USIC0_CH0.DX4A | USIC0_CH1.DX5A | ORC0.AIN | | |
| P2.3 | | | | | | | | | VADC0.G1CH5 | | ERU0.1B1 | USIC0_CH0.DX5B | USIC0_CH1.DX3C | USIC0_CH1.DX4C | ORC1.AIN | | |
| P2.4 | | | | | | | | | VADC0.G1CH6 | | ERU0.0A1 | USIC0_CH0.DX3B | USIC0_CH0.DX4B | USIC0_CH1.DX5B | ORC2.AIN | | |
| P2.5 | | | | | | | | | VADC0.G1CH7 | | ERU0.1A1 | USIC0_CH0.DX5D | USIC0_CH1.DX3E | USIC0_CH1.DX4E | ORC3.AIN | | |

## Table 10 Hardware Controlled I/O Functions

| Function | Outputs | | Inputs | | Pull Control | | | |
|---|---|---|---|---|---|---|---|---|
| | HWO0 | HWO1 | HWI0 | HWI1 | HW0_PD | HW0_PU | HW1_PD | HW1_PU |
| P0.0 | | | | | | | | |
| P0.1 | | | | | | | | |
| P0.2 | | | | | | | | |
| P0.3 | | | | | | | | |
| P0.4 | | | | | | | | |
| P0.5 | | | | | | | | |
| P0.6 | | | | | | | | |
| P0.7 | | | | | | | | |
| P0.8 | | | | | | | | |
| P0.9 | | | | | | | | |
| P0.10 | | | | | | | | |
| P0.11 | | | | | | | | |
| P0.12 | | | | | | | | |
| P0.13 | | | | | | | | |
| P0.14 | | | | | | | | |
| P0.15 | | | | | | | | |
| P1.0 | | USIC0_CH0.DOUT0 | | USIC0_CH0.HWIN0 | $\overline{\text{BCCU0.OUT2}}$ | BCCU0.OUT2 | | |
| P1.1 | | USIC0_CH0.DOUT1 | | USIC0_CH0.HWIN1 | $\overline{\text{BCCU0.OUT3}}$ | BCCU0.OUT3 | | |
| P1.2 | | USIC0_CH0.DOUT2 | | USIC0_CH0.HWIN2 | $\overline{\text{BCCU0.OUT4}}$ | BCCU0.OUT4 | | |
| P1.3 | | USIC0_CH0.DOUT3 | | USIC0_CH0.HWIN3 | $\overline{\text{BCCU0.OUT5}}$ | BCCU0.OUT5 | | |
| P1.4 | | | | | $\overline{\text{BCCU0.OUT6}}$ | BCCU0.OUT6 | | |
| P1.5 | | | | | $\overline{\text{BCCU0.OUT7}}$ | BCCU0.OUT7 | | |
| P1.6 | | | | | $\overline{\text{BCCU0.OUT8}}$ | BCCU0.OUT8 | | |
| P2.0 | | | | | $\overline{\text{BCCU0.OUT1}}$ | BCCU0.OUT1 | | |
| P2.1 | | | | | $\overline{\text{BCCU0.OUT6}}$ | BCCU0.OUT6 | | |
| P2.2 | | | | | $\overline{\text{BCCU0.OUT0}}$ | BCCU0.OUT0 | $\overline{\text{CCU40.OUT3}}$ | CCU40.OUT3 |
| P2.3 | | | | | $\overline{\text{ACMP2.OUT}}$ | ACMP2.OUT | | |
| P2.4 | | | | | $\overline{\text{BCCU0.OUT8}}$ | BCCU0.OUT8 | | |
| P2.5 | | | | | $\overline{\text{ACMP1.OUT}}$ | ACMP1.OUT | | |

# 3 Electrical Parameters

This section provides the electrical parameters which are implementation-specific for the XMC1300.

## 3.1 General Parameters

### 3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the “Symbol” column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1300 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1300 is designed in.

**Table 16 Input/Output Characteristics (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | | Limit Values | | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| | | | Min. | Max. | | |
| Input Hysteresis[8)] | $HYS$ | CC | 0.08 × $V_{DDP}$ | – | V | CMOS Mode (5 V), Standard Hysteresis |
| | | | 0.03 × $V_{DDP}$ | – | V | CMOS Mode (3.3 V), Standard Hysteresis |
| | | | 0.02 × $V_{DDP}$ | – | V | CMOS Mode (2.2 V), Standard Hysteresis |
| | | | 0.5 × $V_{DDP}$ | 0.75 × $V_{DDP}$ | V | CMOS Mode(5 V), Large Hysteresis |
| | | | 0.4 × $V_{DDP}$ | 0.75 × $V_{DDP}$ | V | CMOS Mode(3.3 V), Large Hysteresis |
| | | | 0.2 × $V_{DDP}$ | 0.65 × $V_{DDP}$ | V | CMOS Mode(2.2 V), Large Hysteresis |
| Pin capacitance (digital inputs/outputs) | $C_{IO}$ | CC | – | 10 | pF | |
| Pull-up resistor on port pins | $R_{PUP}$ | CC | 20 | 50 | kohm | $V_{IN} = V_{SSP}$ |
| Pull-down resistor on port pins | $R_{PDP}$ | CC | 20 | 50 | kohm | $V_{IN} = V_{DDP}$ |
| Input leakage current[9)] | $I_{OZP}$ | CC | -1 | 1 | µA | $0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C |
| Voltage on any pin during $V_{DDP}$ power off | $V_{PO}$ | SR | – | 0.3 | V | [10)] |
| Maximum current per pin (excluding P1, $V_{DDP}$ and $V_{SS}$) | $I_{MP}$ | SR | -10 | 11 | mA | – |
| Maximum current per high currrent pins | $I_{MP1A}$ | SR | -10 | 50 | mA | – |
| Maximum current into $V_{DDP}$ (TSSOP16, VQFN24) | $I_{MVDD1}$ | SR | – | 130 | mA | [18)] |
| Maximum current into $V_{DDP}$ (TSSOP38, VQFN40) | $I_{MVDD2}$ | SR | – | 260 | mA | [18)] |

**Table 17 ADC Characteristics (Operating Conditions apply)[1)]** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Gain settings | $G_{IN}$ CC | 1 | | | – | GNCTRxz.GAINy = $00_B$ (unity gain) |
| | | 3 | | | – | GNCTRxz.GAINy = $01_B$ (gain g1) |
| | | 6 | | | – | GNCTRxz.GAINy = $10_B$ (gain g2) |
| | | 12 | | | – | GNCTRxz.GAINy = $11_B$ (gain g3) |
| Sample Time | $t_{sample}$ CC | 3 | – | – | 1 / $f_{ADC}$ | $V_{DD}$ = 5.0 V |
| | | 3 | – | – | 1 / $f_{ADC}$ | $V_{DD}$ = 3.3 V |
| | | 30 | – | – | 1 / $f_{ADC}$ | $V_{DD}$ = 2.0 V |
| Sigma delta loop hold time | $t_{SD\_hold}$ CC | 20 | – | – | µs | Residual charge stored in an active sigma delta loop remains available |
| Conversion time in fast compare mode | $t_{CF}$ CC | 9 | | | 1 / $f_{ADC}$ | 2) |
| Conversion time in 12-bit mode | $t_{C12}$ CC | 20 | | | 1 / $f_{ADC}$ | 2) |
| Maximum sample rate in 12-bit mode 3) | $f_{C12}$ CC | – | – | $f_{ADC}$ / 42.5 | – | 1 sample pending |
| | | – | – | $f_{ADC}$ / 62.5 | – | 2 samples pending |
| Conversion time in 10-bit mode | $t_{C10}$ CC | 18 | | | 1 / $f_{ADC}$ | 2) |
| Maximum sample rate in 10-bit mode 3) | $f_{C10}$ CC | – | – | $f_{ADC}$ / 40.5 | – | 1 sample pending |
| | | – | – | $f_{ADC}$ / 58.5 | – | 2 samples pending |
| Conversion time in 8-bit mode | $t_{C8}$ CC | 16 | | | 1 / $f_{ADC}$ | 2) |

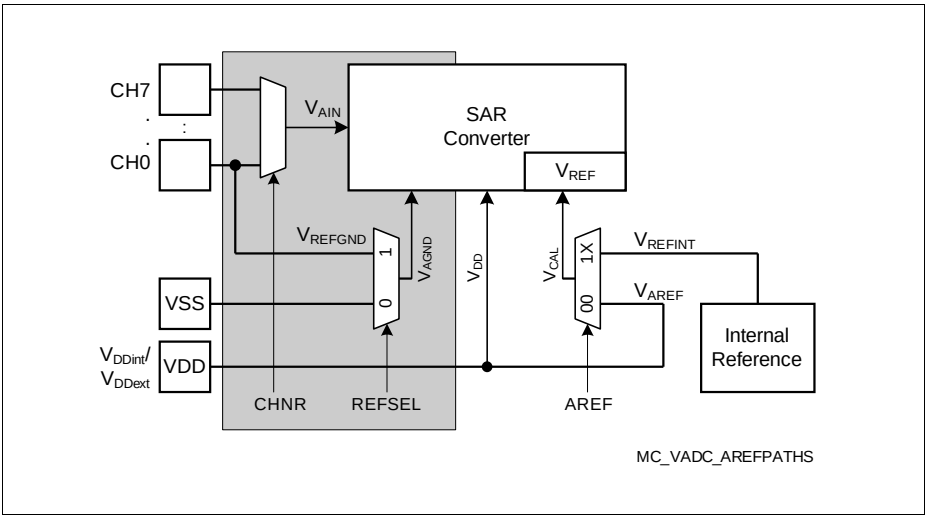


**Figure 11 ADC Voltage Supply**

### 3.2.5 Temperature Sensor Characteristics

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 20 Temperature Sensor Characteristics**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Measurement time | $t_M$ CC | – | – | 10 | ms | |
| Temperature sensor range | $T_{SR}$ SR | -40 | – | 115 | °C | |
| Sensor Accuracy[1)] | $T_{TSAL}$ CC | -6 | – | 6 | °C | $T_J$ > 20°C |
| | | -10 | – | 10 | °C | 0°C ≤ $T_J$ ≤ 20°C |
| | | – | -/+8 | – | °C | $T_J$ < 0°C |
| Start-up time after enabling | $t_{TSSTE}$ SR | – | – | 15 | µs | |

1) The temperature sensor accuracy is independent of the supply voltage.

**Table 21 Power Supply Parameters; $V_{DDP}$ = 5V**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ.[1] | Max. | | |
| Sleep mode current Peripherals clock disabled Flash active $f_{MCLK}$ / $f_{PCLK}$ in MHz[5] | $I_{DDPSD}$ CC | – | 1.8 | - | mA | 32 / 64 |
| | | | 1.7 | - | mA | 24 / 48 |
| | | | 1.6 | - | mA | 16 / 32 |
| | | | 1.5 | - | mA | 8 / 16 |
| | | | 1.4 | - | mA | 1 / 1 |
| Sleep mode current Peripherals clock disabled Flash powered down $f_{MCLK}$ / $f_{PCLK}$ in MHz[6] | $I_{DDPSR}$ CC | – | 1.2 | - | mA | 32 / 64 |
| | | | 1.1 | - | mA | 24 / 48 |
| | | | 1.0 | - | mA | 16 / 32 |
| | | | 0.8 | - | mA | 8 / 16 |
| | | | 0.7 | - | mA | 1 / 1 |
| Deep Sleep mode current[7] | $I_{DDPDS}$ CC | – | 0.24 | - | mA | |
| Wake-up time from Sleep to Active mode[8] | $t_{SSA}$ CC | – | 6 | - | cycles | |
| Wake-up time from Deep Sleep to Active mode[9] | $t_{DSA}$ CC | – | 280 | - | µsec | |

1) The typical values are measured at $T_A$ = + 25 °C and VDDP = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Table 22 provides the active current consumption of some modules operating at 5 V power supply at 25° C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

**Table 22 Typical Active Current Consumption**

| Active Current Consumption | Symbol | Limit Values | Unit | Test Condition |
|---|---|---|---|---|
| | | Typ. | | |
| Baseload current | $I_{CPUDDC}$ | 5.04 | mA | Modules including Core, SCU, PORT, memories, ANATOP[1)] |
| VADC and SHS | $I_{ADCDDC}$ | 3.4 | mA | Set CGATCLR0.VADC to 1[2)] |
| USIC0 | $I_{USIC0DDC}$ | 0.87 | mA | Set CGATCLR0.USIC0 to 1[3)] |
| CCU40 | $I_{CCU40DDC}$ | 0.94 | mA | Set CGATCLR0.CCU40 to 1[4)] |
| CCU80 | $I_{CCU80DDC}$ | 0.42 | mA | Set CGATCLR0.CCU80 to 1[5)] |
| POSIF0 | $I_{PIF0DDC}$ | 0.26 | mA | Set CGATCLR0.POSIF0 to 1[6)] |
| BCCU0 | $I_{BCCU0DDC}$ | 0.24 | mA | Set CGATCLR0.BCCU0 to 1[7)] |
| MATH | $I_{MATHDDC}$ | 0.35 | mA | Set CGATCLR0.MATH to 1[8)] |
| WDT | $I_{WDTDDC}$ | 0.03 | mA | Set CGATCLR0.WDT to 1[9)] |
| RTC | $I_{RTCDDC}$ | 0.01 | mA | Set CGATCLR0.RTC to 1[10)] |

1) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.

2) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode

3) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms

4) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle

5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU8 slice with PWM frequency at 1500Hz and a period match interrupt used to toggle duty cycle between 10% and 90%

6) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, hall sensor mode

7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s

8) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11

9) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s

10) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

### 3.3.2 Power-Up and Supply Monitoring Characteristics

**Table 24** provides the characteristics of the power-up and supply monitoring in XMC1300.

The guard band between the lowest valid operating voltage and the brownout reset threshold provides a margin for noise immunity and hysteresis. The electrical parameters may be violated while $V_{DDP}$ is outside its operating range.

The brownout detection triggers a reset within the defined range. The prewarning detection can be used to trigger an early warning and issue corrective and/or fail-safe actions in case of a critical supply voltage drop.

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

**Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)**

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DDP}$ ramp-up time | $t_{RAMPUP}$ SR | $V_{DDP}$/ $S_{VDDPrise}$ | – | $10^7$ | µs | |
| $V_{DDP}$ slew rate | $S_{VDDPOP}$ SR | 0 | – | 0.1 | V/µs | Slope during normal operation |
| | $S_{VDDP10}$ SR | 0 | – | 10 | V/µs | Slope during fast transient within +/- 10% of $V_{DDP}$ |
| | $S_{VDDPrise}$ SR | 0 | – | 10 | V/µs | Slope during power-on or restart after brownout event |
| | $S_{VDDPfall}$ [1] SR | 0 | – | 0.25 | V/µs | Slope during supply falling out of the +/-10% limits[2] |
| $V_{DDP}$ prewarning voltage | $V_{DDPPW}$ CC | 2.1 | 2.25 | 2.4 | V | ANAVDEL.VDEL_SELECT = $00_B$ |
| | | 2.85 | 3 | 3.15 | V | ANAVDEL.VDEL_SELECT = $01_B$ |
| | | 4.2 | 4.4 | 4.6 | V | ANAVDEL.VDEL_SELECT = $10_B$ |

**Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply)** (cont'd)

| Parameter | Symbol | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{DDP}$ brownout reset voltage | $V_{DDPBO}$ CC | 1.55 | 1.62 | 1.75 | V | calibrated, before user code starts running |
| $V_{DDP}$ voltage to ensure defined pad states | $V_{DDPPA}$ CC | – | 1.0 | – | V | |
| Start-up time from power-on reset | $t_{SSW}$ SR | – | 320 | – | µs | Time to the first user code instruction[3)] |
| BMI program time | $t_{BMI}$ SR | – | 8.25 | – | ms | Time taken from a user-triggered system reset after BMI installation is is requested |

1) A capacitor of at least 100 nF has to be added between VDDP and VSSP to fulfill the requirement as stated for this parameter.

2) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

3) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

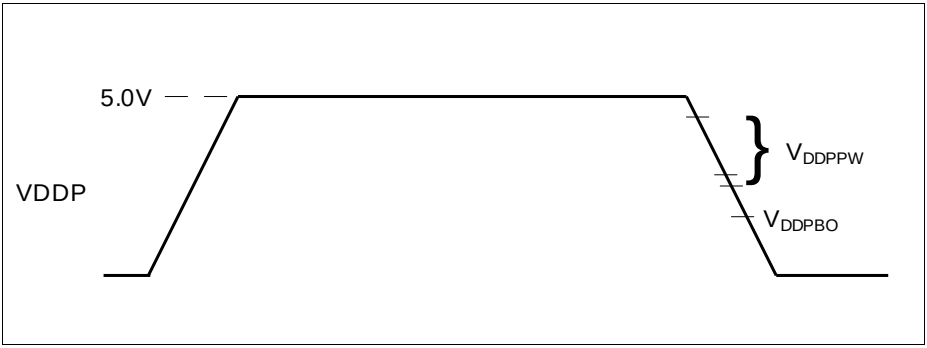


**Figure 19 Supply Threshold Parameters**

### 3.3.5 SPD Timing Requirements

The optimum SPD decision time between $0_B$ and $1_B$ is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

**Table 28 Optimum Number of Sample Clocks for SPD**

| Sample Freq. | Sampling Factor | Sample Clocks $0_B$ | Sample Clocks $1_B$ | Effective Decision Time[1)] | Remark |
|---|---|---|---|---|---|
| 8 MHz | 4 | 1 to 5 | 6 to 12 | 0.69 µs | The other closest option (0.81 µs) for the effective decision time is less robust. |

1) Nominal sample frequency period multiplied with 0.5 + (max. number of $0_B$ sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

### 3.3.6 Peripheral Timings

*Note: These parameters are not subject to production test, but verified by design and/or characterization.*

#### 3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

*Note: Operating Conditions apply.*

**Table 29 USIC SSC Master Mode Timing**

| Parameter | Symbol | | Values | | | Unit | Note / Test Condition |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| SCLKOUT master clock period | $t_{CLK}$ | CC | 62.5 | – | – | ns | |
| Slave select output SELO active to first SCLKOUT transmit edge | $t_1$ | CC | 80 | – | – | ns | |
| Slave select output SELO inactive after last SCLKOUT receive edge | $t_2$ | CC | 0 | – | – | ns | |
| Data output DOUT[3:0] valid time | $t_3$ | CC | -10 | – | 10 | ns | |
| Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge | $t_4$ | SR | 80 | – | – | ns | |
| Data input DX0/DX[5:3] hold time from SCLKOUT receive edge | $t_5$ | SR | 0 | – | – | ns | |

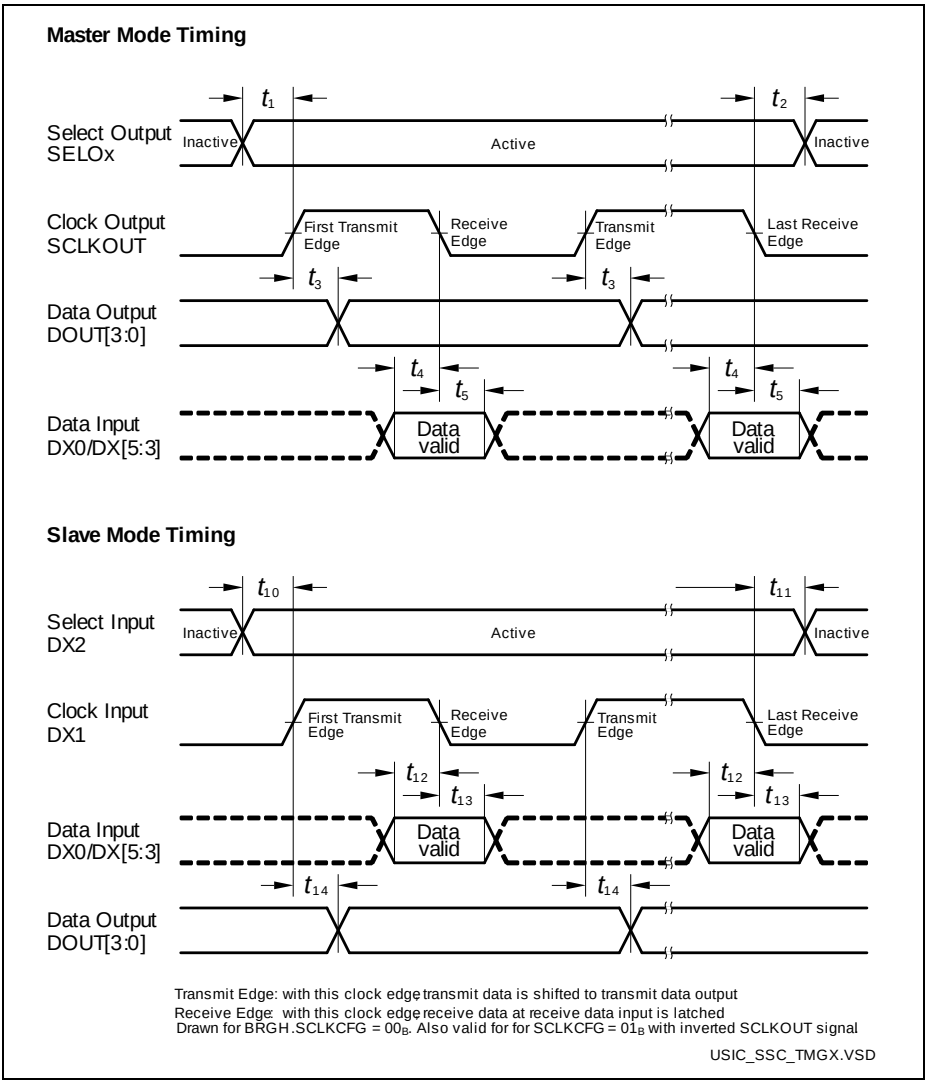


**Figure 22 USIC - SSC Master/Slave Mode Timing**

*Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.*

# 4 Package and Reliability

The XMC1300 is a member of the XMC1000 Family of microcontrollers. It is also compatible to a certain extent with members of similar families or subfamilies.

Each package is optimized for the device it houses. Therefore, there may be slight differences between packages of the same pin-count but for different device types. In particular, the size of the exposed die pad may vary.

If different device types are considered or planned for an application, it must be ensured that the board layout fits all packages under consideration.

## 4.1 Package Parameters

**Table 35** provides the thermal characteristics of the packages used in XMC1300.

**Table 35 Thermal Characteristics of the Packages**

| Parameter | Symbol | Limit Values | | Unit | Package Types |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| Exposed Die Pad Dimensions | Ex × Ey CC | - | 2.7 × 2.7 | mm | PG-VQFN-24-19 |
| | | - | 3.7 × 3.7 | mm | PG-VQFN-40-13 |
| Thermal resistance Junction-Ambient | $R_{\Theta JA}$ CC | - | 104.6 | K/W | PG-TSSOP-16-8[1)] |
| | | - | 83.2 | K/W | PG-TSSOP-28-16[1)] |
| | | - | 70.3 | K/W | PG-TSSOP-38-9[1)] |
| | | - | 46.0 | K/W | PG-VQFN-24-19[1)] |
| | | - | 38.4 | K/W | PG-VQFN-40-13[1)] |

1) Device mounted on a 4-layer JEDEC board (JESD 51-5); exposed pad soldered.

*Note: For electrical reasons, it is required to connect the exposed pad to the board ground $V_{SSP}$, independent of EMC and thermal requirements.*

### 4.1.1 Thermal Considerations

When operating the XMC1300 in a system, the total heat generated in the chip must be dissipated to the ambient environment to prevent overheating and the resulting thermal damage.

The maximum heat that can be dissipated depends on the package and its integration into the target board. The “Thermal resistance $R_{\Theta JA}$” quantifies these parameters. The power dissipation must be limited so that the average junction temperature does not exceed 115 °C.

The difference between junction temperature and ambient temperature is determined by $\Delta T = (P_{INT} + P_{IOSTAT} + P_{IODYN}) \times R_{\Theta JA}$

The internal power consumption is defined as
$P_{INT} = V_{DDP} \times I_{DDP}$ (switching current and leakage current).

The static external power consumption caused by the output drivers is defined as
$P_{IOSTAT} = \Sigma((V_{DDP}-V_{OH}) \times I_{OH}) + \Sigma(V_{OL} \times I_{OL})$

The dynamic external power consumption caused by the output drivers ($P_{IODYN}$) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce $V_{DDP}$, if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

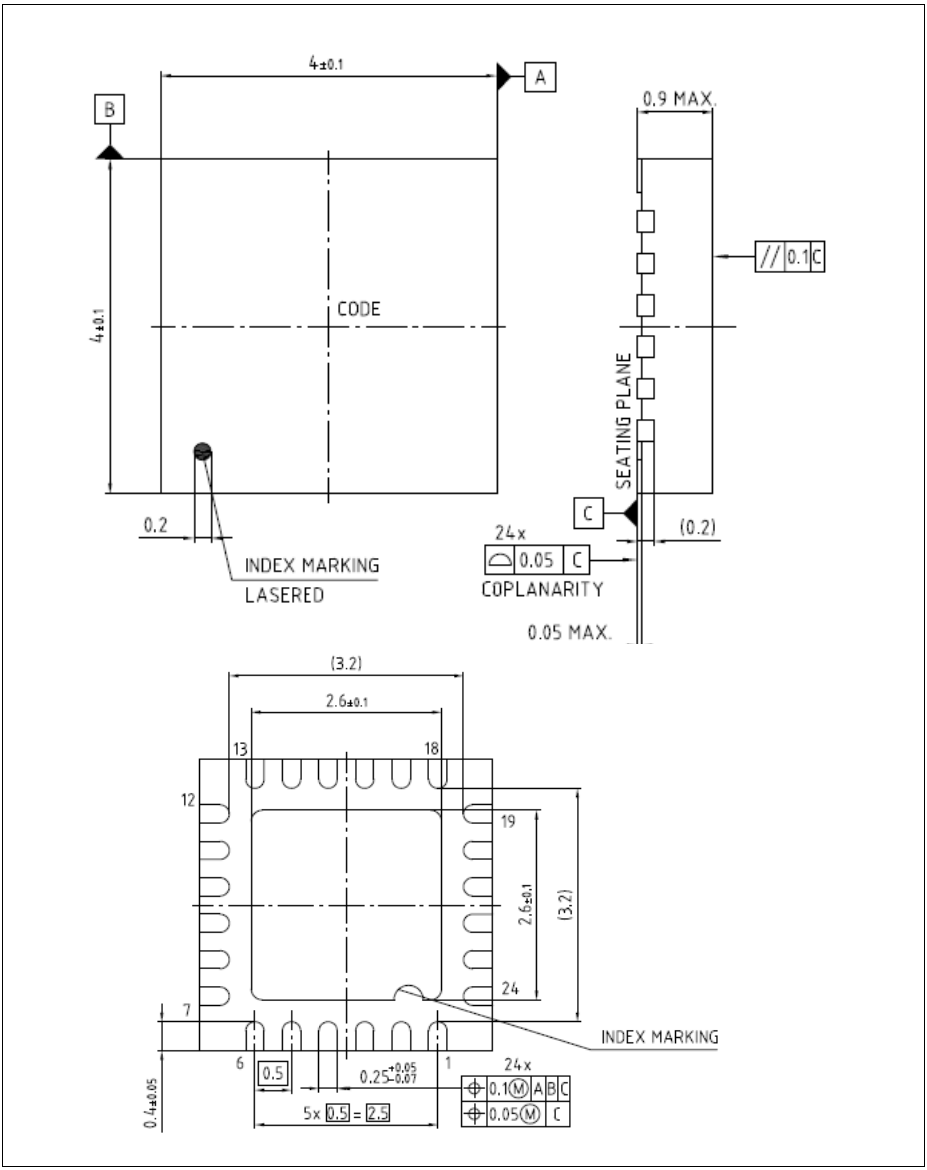


**Figure 29 PG-VQFN-24-19**