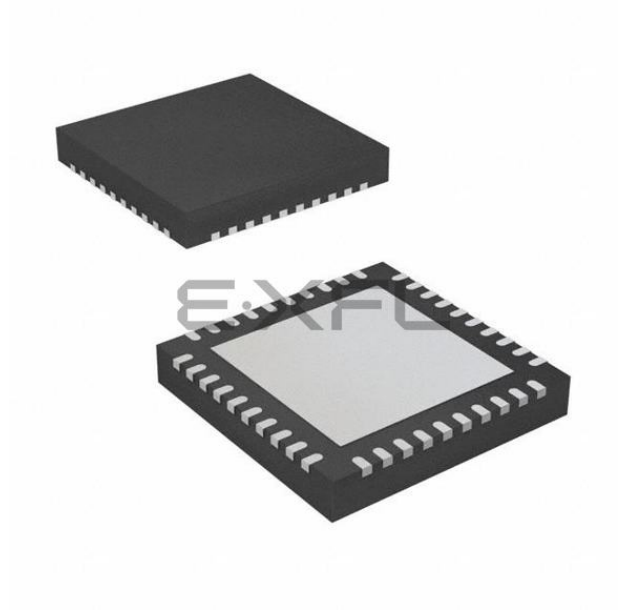
Infineon Technologies - XMC1302Q040X0032ABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302q040x0032abxuma1

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XMC1300 Data Sheet

Revision History: V1.9 2017-03

Previous Version: V1.8 2016-09	
Page	Subjects
Page 10, **Page 12**	Add marking option for XMC1301-T038X0032.

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About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC1300 series devices.

The document describes the characteristics of a superset of the XMC1300 series devices. For simplicity, the various device types are referred to by the collective term XMC1300 throughout this document.

XMC1000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  – decribes the functionality of the superset of devices.
- **Data Sheets**
  – list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  – list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc1000** to get access to the latest versions of those documents.

  - Ultra low power consumption
- Nested Vectored Interrupt Controller (NVIC)
- Event Request Unit (ERU) for processing of external and internal service requests
- MATH Co-processor (MATH)
  - CORDIC unit for trigonometric calculation
  - division unit

On-Chip Memories

- 8 kbytes on-chip ROM
- 16 kbytes on-chip high-speed SRAM
- up to 200 kbytes on-chip Flash program and data memory

Communication Peripherals

- Two Universal Serial Interface Channels (USIC), usable as UART, double-SPI, quad-SPI, IIC, IIS and LIN interfaces

Analog Frontend Peripherals

- A/D Converters
  - up to 12 analog input pins
  - 2 sample and hold stages with 8 analog input channels each
  - fast 12-bit analog to digital converter with adjustable gain
- Up to 8 channels of out of range comparators (ORC)
- Up to 3 fast analog comparators (ACMP)
- Temperature Sensor (TSE)

Industrial Control Peripherals

- Capture/Compare Units 4 (CCU4) as general purpose timers
- Capture/Compare Units 8 (CCU8) for motor control and power conversion
- Position Interfaces (POSIF) for hall and quadrature encoders and motor positioning
- Brightness and Colour Control Unit (BCCU), for LED color and dimming application

System Control

- Window Watchdog Timer (WDT) for safety sensitive applications
- Real Time Clock module with alarm support (RTC)
- System Control Unit (SCU) for system configuration and control
- Pseudo random number generator (PRNG) for fast random data generation

Input/Output Lines

- Tri-stated in input mode
- Push/pull or open drain output mode

Table 4 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T016F0032	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T028X0016	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038X0032	00013013 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038F0064	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083$_H$	AB

Table 4 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1302-Q040X0128	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 $201ED083_H$	AB
XMC1302-Q040X0200	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 $201ED083_H$	AB

2.2.1 Package Pin Summary

The following general building block is used to describe each pin:

Table 5 Package Pin Mapping Description

Function	Package A	Package B	...	Pad Type
Px.y	N	N		Pad Class

The table is sorted by the “Function” column, starting with the regular Port pins (Px.y), followed by the supply pins.

The following columns, titled with the supported package variants, lists the package pin number to which the respective function is mapped in that package.

The “Pad Type” indicates the employed pad type:

- STD_INOUT(standard bi-directional pads)
- STD_INOUT/AN (standard bi-directional pads with analog input)
- High Current (high current bi-directional pads)
- STD_IN/AN (standard input pads with analog input)
- Power (power supply)

Details about the pad properties are defined in the Electrical Parameters.

Table 6 Package Pin Mapping

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.0	23	17	13	15	7	STD_INOUT	
P0.1	24	18	-	-	-	STD_INOUT	
P0.2	25	19	-	-	-	STD_INOUT	
P0.3	26	20	-	-	-	STD_INOUT	
P0.4	27	21	14	-	-	STD_INOUT	
P0.5	28	22	15	16	8	STD_INOUT	
P0.6	29	23	16	17	9	STD_INOUT	

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P2.1	2	36	26	2	-	STD_IN OUT/AN	
P2.2	3	37	27	3	-	STD_IN/ AN	
P2.3	4	38	-	-	-	STD_IN/ AN	
P2.4	5	1	-	-	-	STD_IN/ AN	
P2.5	6	2	28	-	-	STD_IN/ AN	
P2.6	7	3	1	4	16	STD_IN/ AN	
P2.7	8	4	2	5	1	STD_IN/ AN	
P2.8	9	5	3	5	1	STD_IN/ AN	
P2.9	10	6	4	6	2	STD_IN/ AN	
P2.10	11	7	5	7	3	STD_IN OUT/AN	
P2.11	12	8	6	8	4	STD_IN OUT/AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	8	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	15	10	8	10	6	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
VSSP	31	25	-	-	-	Power	I/O port ground
VDDP	32	26	-	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	-	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.2 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

2.2.3 Hardware Controlled I/O Function Description

The following general building block is used to describe the hardware I/O and pull control functions of each PORT pin:

Table 8 Hardware Controlled I/O Function Description

Function	Outputs	Inputs	Pull Control	
	HWO0	**HWI0**	**HW0_PD**	**HW0_PU**
P0.0	MODB.OUT	MODB.INA		
Pn.y			$\overline{\text{MODC.OUT}}$	MODC.OUT

By Pn_HWSEL, it is possible to select between different hardware “masters” (HWO0/HWI0, HWO1/HWI1). The selected peripheral can take control of the pin(s). Hardware control overrules settings in the respective port pin registers. Additional hardware signals HW0_PD/HW1_PD and HW0_PU/HW1_PU controlled by the peripherals can be used to control the pull devices of the pin.

Please refer to the **Hardware Controlled I/O Functions** table for the complete hardware I/O and pull control function mapping.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 11 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Junction temperature	T_J	SR	-40	–	115	°C	–
Storage temperature	T_{ST}	SR	-40	–	125	°C	–
Voltage on power supply pin with respect to V_{SSP}	V_{DDP}	SR	-0.3	–	6	V	–
Voltage on digital pins with respect to V_{SSP} [1]	V_{IN}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Voltage on P2 pins with respect to V_{SSP} [2]	V_{INP2}	SR	-0.3	–	V_{DDP} + 0.3	V	–
Voltage on analog input pins with respect to V_{SSP}	V_{AIN} V_{AREF}	SR	-0.5	–	V_{DDP} + 0.5 or max. 6	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	10	mA	–
Absolute maximum sum of all input currents during overload condition	ΣI_{IN}	SR	-50	–	+50	mA	–

1) Excluding port pins P2.[1,2,6,7,8,9,11].

2) Applicable to port pins P2.[1,2,6,7,8,9,11].

3.2 DC Parameters

3.2.1 Input/Output Characteristics

Table 16 provides the characteristics of the input/output pins of the XMC1300.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Note: Unless otherwise stated, input DC and AC characteristics, including peripheral timings, assume that the input pads operate with the standard hysteresis.

Table 16 Input/Output Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Output low voltage on port pins (with standard pads)	V_{OLP}	CC	–	1.0	V	I_{OL} = 11 mA (5 V) I_{OL} = 7 mA (3.3 V)
			–	0.4	V	I_{OL} = 5 mA (5 V) I_{OL} = 3.5 mA (3.3 V)
Output low voltage on high current pads	V_{OLP1}	CC	–	1.0	V	I_{OL} = 50 mA (5 V) I_{OL} = 25 mA (3.3 V)
			–	0.32	V	I_{OL} = 10 mA (5 V)
			–	0.4	V	I_{OL} = 5 mA (3.3 V)
Output high voltage on port pins (with standard pads)	V_{OHP}	CC	V_{DDP} - 1.0	–	V	I_{OH} = -10 mA (5 V) I_{OH} = -7 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4.5 mA (5 V) I_{OH} = -2.5 mA (3.3 V)
Output high voltage on high current pads	V_{OHP1}	CC	V_{DDP} - 0.32	–	V	I_{OH} = -6 mA (5 V)
			V_{DDP} - 1.0	–	V	I_{OH} = -8 mA (3.3 V)
			V_{DDP} - 0.4	–	V	I_{OH} = -4 mA (3.3 V)
Input low voltage on port pins (Standard Hysteresis)	V_{ILPS}	SR	–	0.19 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input Hysteresis[8)]	HYS	CC	0.08 × V_{DDP}	–	V	CMOS Mode (5 V), Standard Hysteresis
			0.03 × V_{DDP}	–	V	CMOS Mode (3.3 V), Standard Hysteresis
			0.02 × V_{DDP}	–	V	CMOS Mode (2.2 V), Standard Hysteresis
			0.5 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(5 V), Large Hysteresis
			0.4 × V_{DDP}	0.75 × V_{DDP}	V	CMOS Mode(3.3 V), Large Hysteresis
			0.2 × V_{DDP}	0.65 × V_{DDP}	V	CMOS Mode(2.2 V), Large Hysteresis
Pin capacitance (digital inputs/outputs)	C_{IO}	CC	–	10	pF	
Pull-up resistor on port pins	R_{PUP}	CC	20	50	kohm	$V_{IN} = V_{SSP}$
Pull-down resistor on port pins	R_{PDP}	CC	20	50	kohm	$V_{IN} = V_{DDP}$
Input leakage current[9)]	I_{OZP}	CC	-1	1	µA	$0 < V_{IN} < V_{DDP}$, $T_A \leq 105$ °C
Voltage on any pin during V_{DDP} power off	V_{PO}	SR	–	0.3	V	[10)]
Maximum current per pin (excluding P1, V_{DDP} and V_{SS})	I_{MP}	SR	-10	11	mA	–
Maximum current per high currrent pins	I_{MP1A}	SR	-10	50	mA	–
Maximum current into V_{DDP} (TSSOP16, VQFN24)	I_{MVDD1}	SR	–	130	mA	[18)]
Maximum current into V_{DDP} (TSSOP38, VQFN40)	I_{MVDD2}	SR	–	260	mA	[18)]

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Maximum current out of V_{SS} (TSSOP16, VQFN24)	I_{MVSS1}	SR	–	130	mA	18)
Maximum current out of V_{SS} (TSSOP38, VQFN40)	I_{MVSS2}	SR	–	260	mA	18)

1) Rise/Fall time parameters are taken with 10% - 90% of supply.
2) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.150 ns/pF at 5 V supply voltage.
3) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.205 ns/pF at 3.3 V supply voltage.
4) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.445 ns/pF at 1.8 V supply voltage.
5) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.225 ns/pF at 5 V supply voltage.
6) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.288 ns/pF at 3.3 V supply voltage.
7) Additional rise/fall time valid for CL = 50 pF - CL = 100 pF @ 0.588 ns/pF at 1.8 V supply voltage.
8) Hysteresis is implemented to avoid meta stable states and switching due to internal ground bounce. It cannot be guaranteed that it suppresses switching due to external system noise.
9) An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin.
10) However, for applications with strict low power-down current requirements, it is mandatory that no active voltage source is supplied at any GPIO pin when V_{DDP} is powered off.

Table 17 ADC Characteristics (Operating Conditions apply)[1)] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00_B (unity gain)
		3			–	GNCTRxz.GAINy = 01_B (gain g1)
		6			–	GNCTRxz.GAINy = 10_B (gain g2)
		12			–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DD} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DD} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DD} = 2.0 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	2)
Conversion time in 12-bit mode	t_{C12} CC	20			1 / f_{ADC}	2)
Maximum sample rate in 12-bit mode 3)	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			1 / f_{ADC}	2)
Maximum sample rate in 10-bit mode 3)	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			1 / f_{ADC}	2)

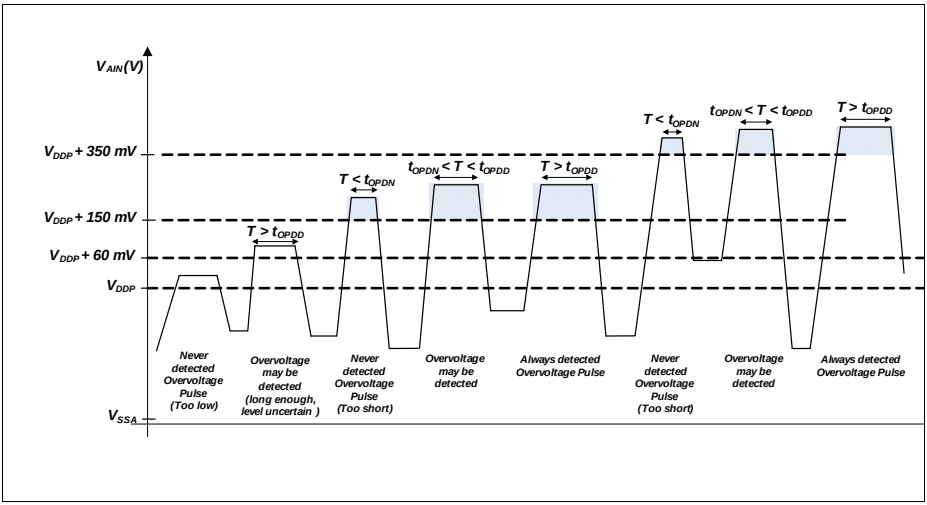

Figure 13 ORC Detection Ranges

Table 21 Power Supply Parameters; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	1.8	-	mA	32 / 64
			1.7	-	mA	24 / 48
			1.6	-	mA	16 / 32
			1.5	-	mA	8 / 16
			1.4	-	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	1.2	-	mA	32 / 64
			1.1	-	mA	24 / 48
			1.0	-	mA	16 / 32
			0.8	-	mA	8 / 16
			0.7	-	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.24	-	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	-	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	280	-	µsec	

1) The typical values are measured at T_A = + 25 °C and VDDP = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 28 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

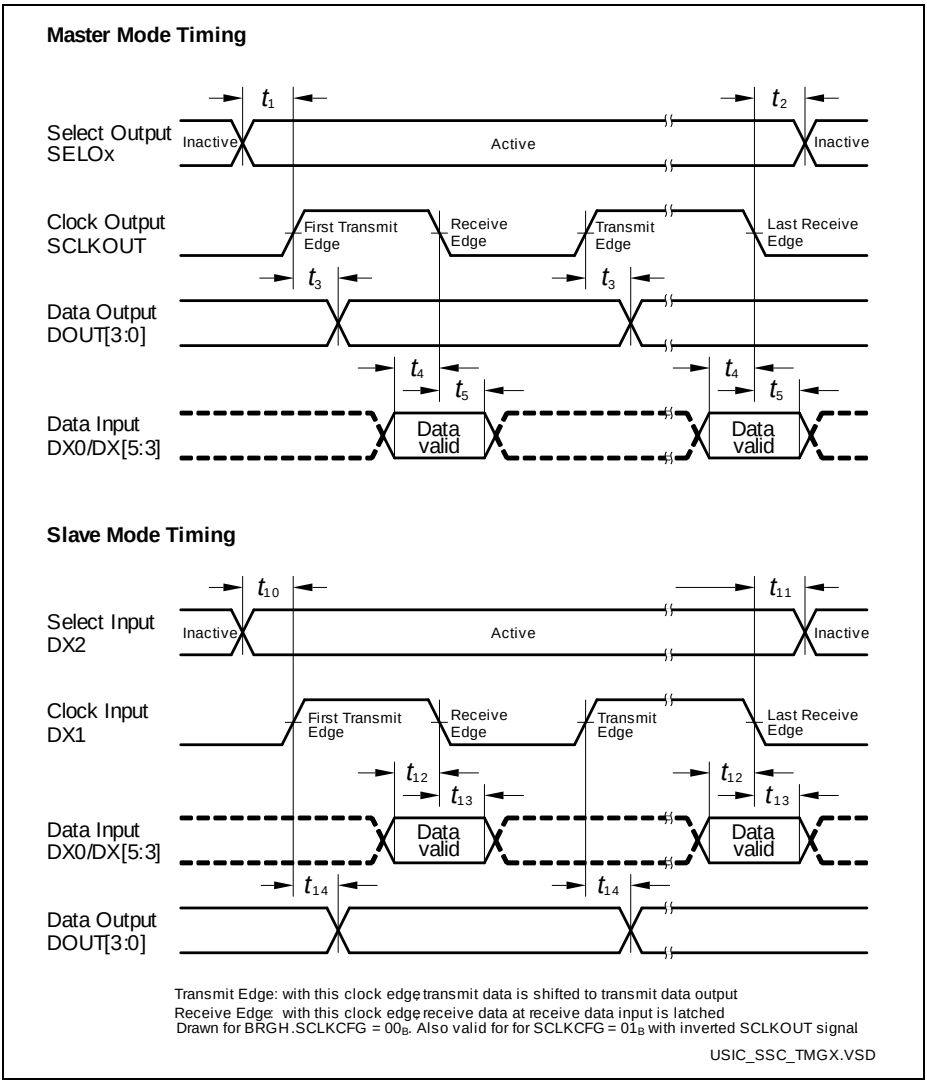

Figure 22 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration, for which the slave select signal is low-active, and the serial clock signal is not shifted and not inverted.

5 Quality Declaration

Table 36 shows the characteristics of the quality parameters in the XMC1300.

Table 36 Quality Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
ESD susceptibility according to Human Body Model (HBM)	V_{HBM} SR	-	2000	V	Conforming to EIA/JESD22-A114-B
ESD susceptibility according to Charged Device Model (CDM) pins	V_{CDM} SR	-	500	V	Conforming to JESD22-C101-C
Moisture sensitivity level	MSL CC	-	3	-	JEDEC J-STD-020D
Soldering temperature	T_{SDR} SR	-	260	°C	Profile according to JEDEC J-STD-020D