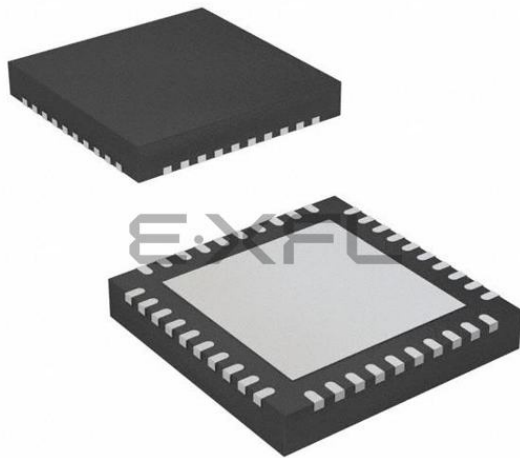




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302q040x0064abxuma1

Summary of Features
Table 4 XMC1300 Chip Identification Number (cont'd)

Derivative	Value	Marking
XMC1302-T038X0128	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00021000 201ED083 _H	AB
XMC1302-T038X0200	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00033000 201ED083 _H	AB
XMC1301-Q024F0008	00013062 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 _H	AB
XMC1301-Q024F0016	00013062 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1302-Q024F0016	00013062 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1302-Q024F0032	00013062 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1302-Q024F0064	00013062 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 _H	AB
XMC1302-Q024X0016	00013063 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1302-Q024X0032	00013063 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1302-Q024X0064	00013063 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 _H	AB
XMC1301-Q040F0008	00013042 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083 _H	AB
XMC1301-Q040F0016	00013042 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1301-Q040F0032	00013042 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1302-Q040X0016	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083 _H	AB
XMC1302-Q040X0032	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083 _H	AB
XMC1302-Q040X0064	00013043 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083 _H	AB

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

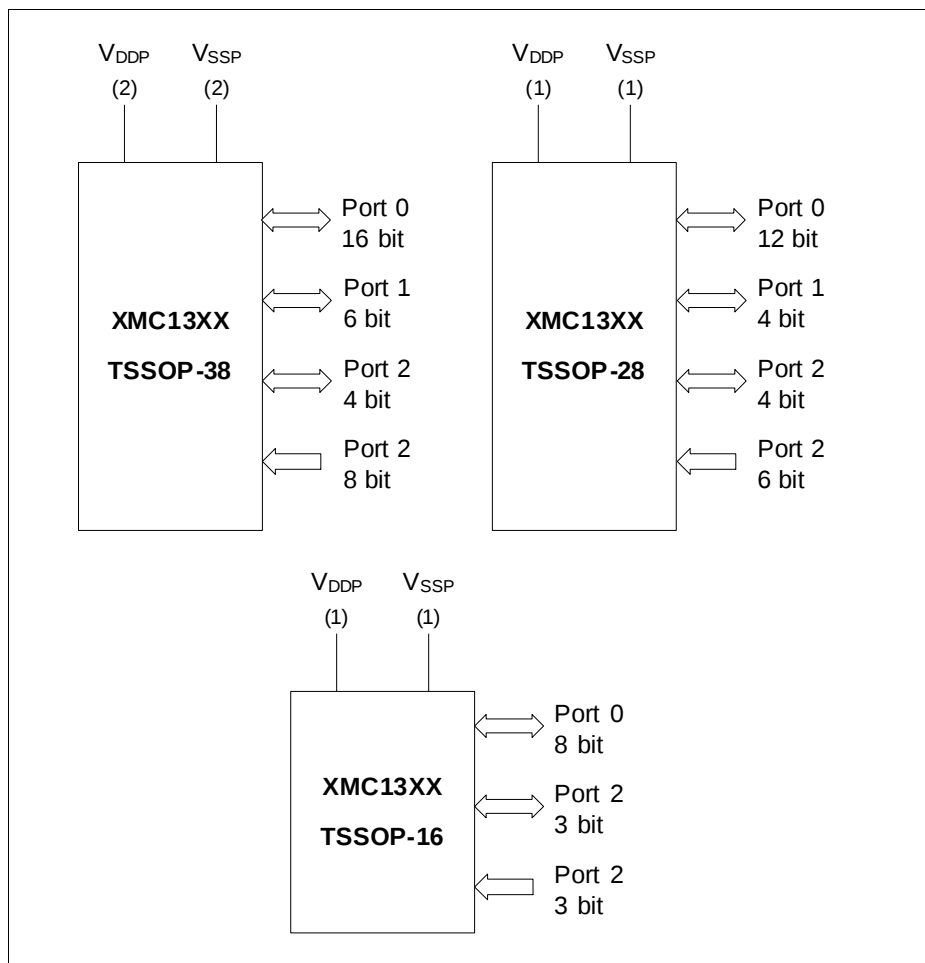


Figure 2 XMC1300 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16

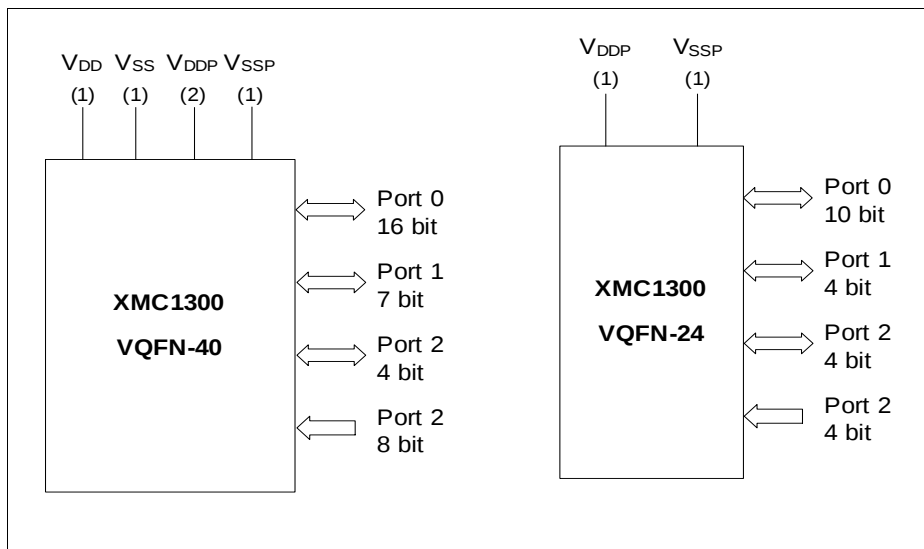


Figure 3 XMC1300 Logic Symbol for VQFN-24 and VQFN-40

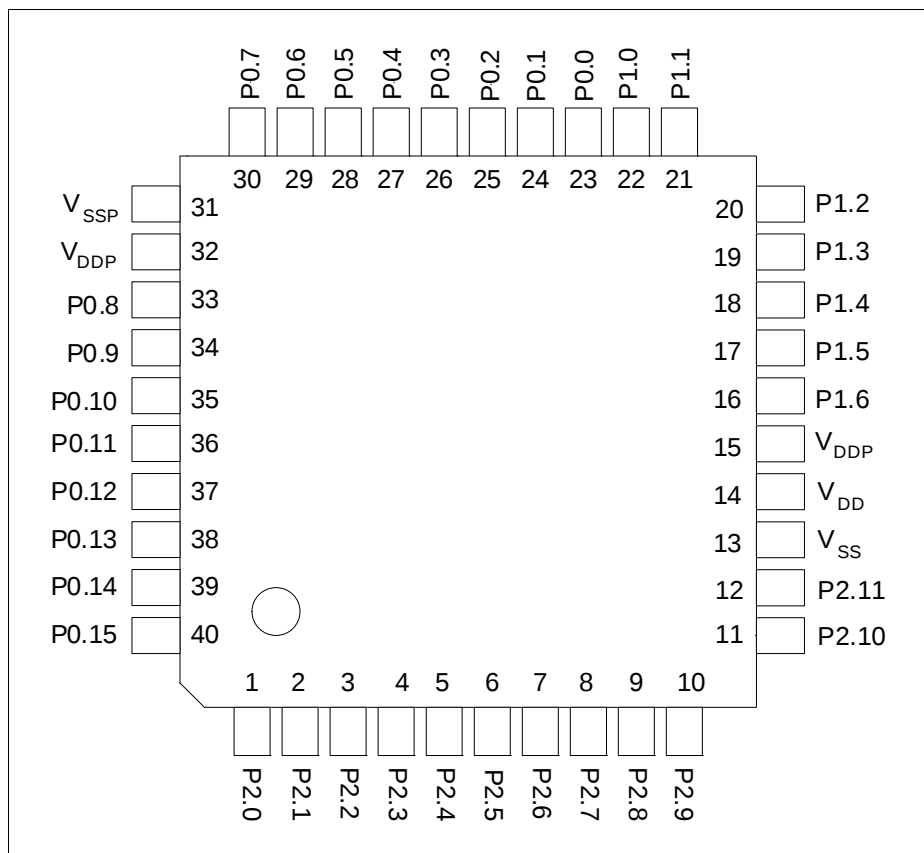


Figure 8 XMC1300 PG-VQFN-40 Pin Configuration (top view)

General Device Information
Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P0.7	30	24	17	18	10	STD_IN OUT	
P0.8	33	27	18	19	11	STD_IN OUT	
P0.9	34	28	19	20	12	STD_IN OUT	
P0.10	35	29	20	-	-	STD_IN OUT	
P0.11	36	30	-	-	-	STD_IN OUT	
P0.12	37	31	21	21	-	STD_IN OUT	
P0.13	38	32	22	22	-	STD_IN OUT	
P0.14	39	33	23	23	13	STD_IN OUT	
P0.15	40	34	24	24	14	STD_IN OUT	
P1.0	22	16	12	14	-	High Current	
P1.1	21	15	11	13	-	High Current	
P1.2	20	14	10	12	-	High Current	
P1.3	19	13	9	11	-	High Current	
P1.4	18	12	-	-	-	High Current	
P1.5	17	11	-	-	-	High Current	
P1.6	16	-	-	-	-	STD_IN OUT	
P2.0	1	35	25	1	15	STD_IN OUT/AN	

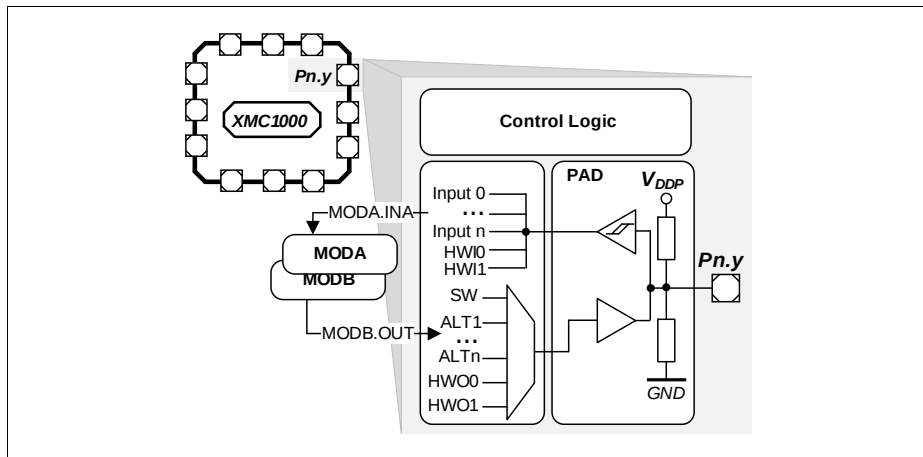


Figure 9 Simplified Port Structure

Pn.y is the port pin name, defining the control and data bits/registers associated with it. As GPIO, the port is under software control. Its input value is read via Pn_IN.y, Pn_OUT defines the output value.

Up to seven alternate output functions (ALT1/2/3/4/5/6/7) can be mapped to a single port pin, selected by Pn_IOC.R.PC. The output value is directly driven by the respective module, with the pin characteristics controlled by the port registers (within the limits of the connected pad).

The port pin input can be connected to multiple peripherals. Most peripherals have an input multiplexer to select between different possible input sources.

The input path is also active while the pin is configured as output. This allows to feedback an output to on-chip resources without wasting an additional external pin.

Please refer to the [Port I/O Functions](#) table for the complete Port I/O function mapping.

Table 9 Port I/O Functions (cont'd)

Function	Outputs							Inputs								
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.14	BCCU0. OUT7				CCU0. OUT31	USIC0_C H0.DOUT 0	USIC0_C H0.SCLK OUT			POSIF0. IN1B		USIC0_C H0.DX0A	USIC0_C H0.DX1A			
P0.15	BCCU0. OUT8				CCU0. OUT30	USIC0_C H0.DOUT 0	USIC0_C H1.MCLK OUT			POSIF0. IN2B		USIC0_C H0.DX0B				
P1.0	BCCU0. OUT0	CCU40. OUT0			CCU0. OUT00	ACMP1. OUT	USIC0_C H0.DOUT 0			POSIF0. IN2A		USIC0_C H0.DX0C				
P1.1	VADC0. EMUX00	CCU40. OUT1			CCU0. OUT01	USIC0_C H0.DOUT 0	USIC0_C H1.SELO 0			POSIF0. IN1A		USIC0_C H0.DX0D	USIC0_C H0.DX1D	USIC0_C H1.DX2E		
P1.2	VADC0. EMUX01	CCU40. OUT2			CCU0. OUT10	ACMP2. OUT	USIC0_C H1.DOUT 0			POSIF0. IN0A		USIC0_C H1.DX0B				
P1.3	VADC0. EMUX02	CCU40. OUT3			CCU0. OUT11	USIC0_C H1.SCLK OUT	USIC0_C H1.DOUT 0					USIC0_C H1.DX0A	USIC0_C H1.DX1A			
P1.4	VADC0. EMUX10	USIC0_C H1.SCLK OUT			CCU0. OUT20	USIC0_C H0.SELO 0	USIC0_C H1.SELO 1					USIC0_C H0.DX5E	USIC0_C H1.DX5E			
P1.5	VADC0. EMUX11	USIC0_C H0.DOUT 0		BCCU0. OUT1	CCU0. OUT21	USIC0_C H0.SELO 1	USIC0_C H1.SELO 2					USIC0_C H1.DX5F				
P1.6	VADC0. EMUX12	USIC0_C H1.DOUT 0		USIC0_C H0.SCLK OUT	BCCU0. OUT2	USIC0_C H0.SELO 2	USIC0_C H1.SELO 3			USIC0_C H0.DX5F						
P2.0	ERU0. PDOUT3	CCU40. OUT0	ERU0. GOUT3		CCU0. OUT20	USIC0_C H0.DOUT 0	USIC0_C H0.SCLK OUT		VADC0. G0CH5		ERU0.0B 0	USIC0_C H0.DX0E	USIC0_C H0.DX1E	USIC0_C H1.DX2F		
P2.1	ERU0. PDOUT2	CCU40. OUT1	ERU0. GOUT2		CCU0. OUT21	USIC0_C H0.DOUT 0	USIC0_C H1.SCLK OUT	ACMP2.I NP	VADC0. G0CH6		ERU0.1B 0	USIC0_C H0.DX0F	USIC0_C H1.DX3A	USIC0_C H1.DX4A		
P2.2								ACMP2.I NN	VADC0. G0CH7		ERU0.0B 1	USIC0_C H0.DX3A	USIC0_C H0.DX4A	USIC0_C H1.DX5A	ORC0.AI N	
P2.3									VADC0. G1CH5		ERU0.1B 1	USIC0_C H0.DX5B	USIC0_C H1.DX3C	USIC0_C H1.DX4C	ORC1.AI N	
P2.4									VADC0. G1CH6		ERU0.0A 1	USIC0_C H0.DX3B	USIC0_C H0.DX4B	USIC0_C H1.DX5B	ORC2.AI N	
P2.5									VADC0. G1CH7		ERU0.1A 1	USIC0_C H0.DX5D	USIC0_C H1.DX3E	USIC0_C H1.DX4E	ORC3.AI N	

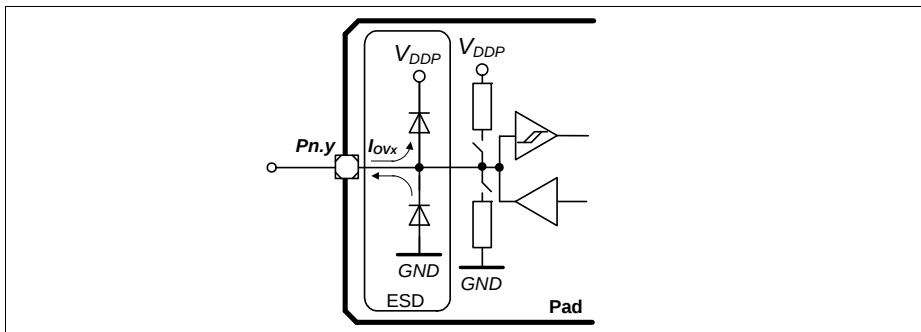


Figure 10 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characteristics for positive Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5 \text{ V}$ $V_{AIN} = V_{DDP} + 0.5 \text{ V}$ $V_{AREF} = V_{DDP} + 0.5 \text{ V}$
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP} + 0.3 \text{ V}$

Table 14 PN-Junction Characteristics for negative Overload

Pad Type	$I_{OV} = 5 \text{ mA}$
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5 \text{ V}$ $V_{AIN} = V_{SS} - 0.5 \text{ V}$ $V_{AREF} = V_{SS} - 0.5 \text{ V}$
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS} - 0.3 \text{ V}$

Electrical Parameters
Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	Symbol		Limit Values		Unit	Test Conditions
			Min.	Max.		
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	$0.7 \times V_{DDP}$	—	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	—	$0.08 \times V_{DDP}$	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ¹⁸⁾
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	$0.85 \times V_{DDP}$	—	V	CMOS Mode (5 V, 3.3 V & 2.2 V) ¹⁸⁾
Rise time on High Current Pad ¹⁾	t_{HCPR}	CC	—	9	ns	50 pF @ 5 V ²⁾
			—	12	ns	50 pF @ 3.3 V ³⁾
			—	25	ns	50 pF @ 1.8 V ⁴⁾
Fall time on High Current Pad ¹⁾	t_{HCPF}	CC	—	9	ns	50 pF @ 5 V ²⁾
			—	12	ns	50 pF @ 3.3 V ³⁾
			—	25	ns	50 pF @ 1.8 V ⁴⁾
Rise time on Standard Pad ¹⁾	t_R	CC	—	12	ns	50 pF @ 5 V ⁵⁾
			—	15	ns	50 pF @ 3.3 V ⁶⁾
			—	31	ns	50 pF @ 1.8 V ⁷⁾
Fall time on Standard Pad ¹⁾	t_F	CC	—	12	ns	50 pF @ 5 V ⁵⁾
			—	15	ns	50 pF @ 3.3 V ⁶⁾
			—	31	ns	50 pF @ 1.8 V ⁷⁾

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	—	3.0	V	SHSCFG.AREF = 11 _B CALCTR.CALGNSTC = 0C _H
		3.0	—	5.5	V	SHSCFG.AREF = 10 _B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	—	5.5	V	SHSCFG.AREF = 00 _B
Analog input voltage range	V_{AIN} SR	$V_{SSP} - 0.05$	—	$V_{DDP} + 0.05$	V	
Auxiliary analog reference ground	V_{REFGND} SR	$V_{SSP} - 0.05$	—	1.0	V	G0CH0
		$V_{SSP} - 0.05$	—	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	—	1.2	2	pF	GNCTRxz.GAINy = 00 _B (unity gain)
		—	1.2	2	pF	GNCTRxz.GAINy = 01 _B (gain g1)
		—	4.5	6	pF	GNCTRxz.GAINy = 10 _B (gain g2)
		—	4.5	6	pF	GNCTRxz.GAINy = 11 _B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	—	—	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	—	—	10	pF	

Electrical Parameters
Table 17 ADC Characteristics (Operating Conditions apply)¹⁾ (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00 _B (unity gain)
		3			–	GNCTRxz.GAINy = 01 _B (gain g1)
		6			–	GNCTRxz.GAINy = 10 _B (gain g2)
		12			–	GNCTRxz.GAINy = 11 _B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	$V_{DD} = 5.0$ V
		3	–	–	1 / f_{ADC}	$V_{DD} = 3.3$ V
		30	–	–	1 / f_{ADC}	$V_{DD} = 2.0$ V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	μs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	²⁾
Conversion time in 12-bit mode	t_{C12} CC	20			1 / f_{ADC}	²⁾
Maximum sample rate in 12-bit mode ³⁾	f_{C12} CC	–	–	$f_{ADC} / 42.5$	–	1 sample pending
		–	–	$f_{ADC} / 62.5$	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			1 / f_{ADC}	²⁾
Maximum sample rate in 10-bit mode ³⁾	f_{C10} CC	–	–	$f_{ADC} / 40.5$	–	1 sample pending
		–	–	$f_{ADC} / 58.5$	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			1 / f_{ADC}	²⁾

Electrical Parameters

Figure 14 shows typical graphs for active mode supply current for $V_{DDP} = 5V$, $V_{DDP} = 3.3V$, $V_{DDP} = 1.8V$ across different clock frequencies.

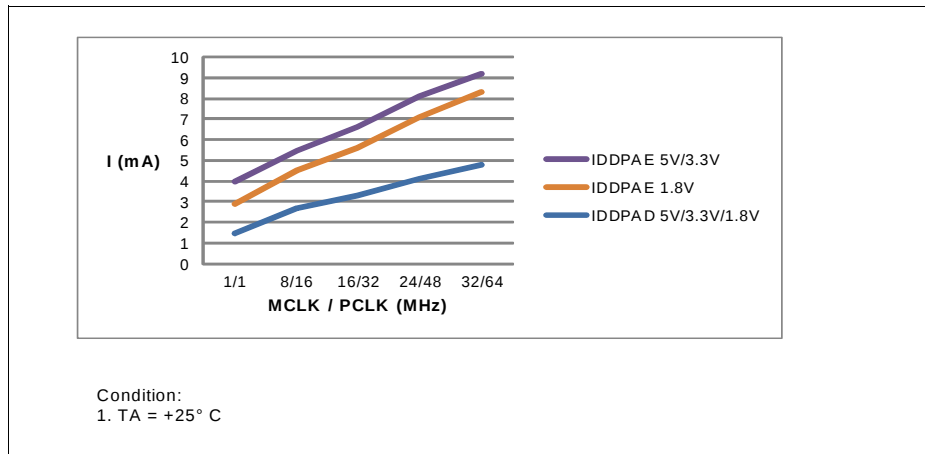


Figure 14 Active mode, a) peripherals clocks enabled, b) peripherals clocks disabled: Supply current I_{DDPA} over supply voltage V_{DDP} for different clock frequencies

Electrical Parameters

Table 22 provides the active current consumption of some modules operating at 5 V power supply at 25° C. The typical values shown are used as a reference guide on the current consumption when these modules are enabled.

Table 22 Typical Active Current Consumption

Active Current Consumption	Symbol	Limit Values	Unit	Test Condition
		Typ.		
Baseload current	I_{CPUDDC}	5.04	mA	Modules including Core, SCU, PORT, memories, ANATOP ¹⁾
VADC and SHS	$I_{\text{ADCD DDC}}$	3.4	mA	Set CGATCLR0.VADC to 1 ²⁾
USIC0	$I_{\text{USIC0 DDC}}$	0.87	mA	Set CGATCLR0.USIC0 to 1 ³⁾
CCU40	$I_{\text{CCU40 DDC}}$	0.94	mA	Set CGATCLR0.CCU40 to 1 ⁴⁾
CCU80	$I_{\text{CCU80 DDC}}$	0.42	mA	Set CGATCLR0.CCU80 to 1 ⁵⁾
POSIF0	$I_{\text{PIF0 DDC}}$	0.26	mA	Set CGATCLR0.POSIF0 to 1 ⁶⁾
BCCU0	$I_{\text{BCCU0 DDC}}$	0.24	mA	Set CGATCLR0.BCCU0 to 1 ⁷⁾
MATH	$I_{\text{MATH DDC}}$	0.35	mA	Set CGATCLR0.MATH to 1 ⁸⁾
WDT	$I_{\text{WDT DDC}}$	0.03	mA	Set CGATCLR0.WDT to 1 ⁹⁾
RTC	$I_{\text{RTC DDC}}$	0.01	mA	Set CGATCLR0.RTC to 1 ¹⁰⁾

- 1) Baseload current is measured with device running in user mode, MCLK=PCLK=32 MHz, with an endless loop in the flash memory. The clock to the modules stated in CGATSTAT0 are gated.
- 2) Active current is measured with: module enabled, MCLK=32 MHz, running in auto-scan conversion mode
- 3) Active current is measured with: module enabled, alternating messages sent to PC at 57.6kbaud every 200ms
- 4) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU4 slice for PWM switching from 1500Hz and 1000Hz at regular intervals, 1 CCU4 slice in capture mode for reading period and duty cycle
- 5) Active current is measured with: module enabled, MCLK=PCLK=32 MHz, 1 CCU8 slice with PWM frequency at 1500Hz and a period match interrupt used to toggle duty cycle between 10% and 90%
- 6) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, hall sensor mode
- 7) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, FCLK=0.8MHz, Normal mode (BCCU Clk = FCLK/4), 3 BCCU Channels and 1 Dimming Engine, change color or dim every 1s
- 8) Active current is measured with: module enabled, MCLK=32 MHz, PCLK=64MHz, tangent calculation in while loop; CORDIC circular rotation, no keep, autostart; 32-by-32 bit signed DIV, autostart, DVS right shift by 11
- 9) Active current is measured with: module enabled, MCLK=32 MHz, time-out mode; WLB = 0, WUB = 0x00008000; WDT serviced every 1s
- 10) Active current is measured with: module enabled, MCLK=32 MHz, Periodic interrupt enabled

3.2.7 Flash Memory Parameters

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 23 Flash Memory Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Erase Time per page / sector	$t_{\text{ERASE CC}}$	6.8	7.1	7.6	ms	
Program time per block	$t_{\text{PSER CC}}$	102	152	204	μs	
Wake-Up time	$t_{\text{WU CC}}$	–	32.2	–	μs	
Read time per word	$t_{\text{a CC}}$	–	50	–	ns	
Data Retention Time	$t_{\text{RET CC}}$	10	–	–	years	Max. 100 erase / program cycles
Flash Wait States ¹⁾	$N_{\text{WSFLASH CC}}$	0	0	0		$f_{\text{MCLK}} = 8 \text{ MHz}$
		0	1	1		$f_{\text{MCLK}} = 16 \text{ MHz}$
		1	1.3	2		$f_{\text{MCLK}} = 32 \text{ MHz}$
Fixed Flash Wait States configured in bit NVM_NVMCONF.WS	$N_{\text{FWSFLASH SR}}$	0	0	1		NVM_CONFIG1.FI XWS = 1 _B , $f_{\text{MCLK}} \leq 16 \text{ MHz}$
		1	1	1		NVM_CONFIG1.FI XWS = 1 _B , $16 \text{ MHz} < f_{\text{MCLK}} \leq 32 \text{ MHz}$
Erase Cycles	$N_{\text{ECCY CC}}$	–	–	$5 \cdot 10^4$	cycles	Sum of page and sector erase cycles
Total Erase Cycles	$N_{\text{TECCY CC}}$	–	–	$2 \cdot 10^6$	cycles	

1) Flash wait states are automatically inserted by the Flash module during memory read when needed. Typical values are calculated from the execution of the Dhrystone benchmark program.

3.3.4 Serial Wire Debug Port (SW-DP) Timing

The following parameters are applicable for communication through the SW-DP interface.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 27 SWD Interface Timing Parameters(Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SWDCLK high time	t_1 SR	50	—	500000	ns	—
SWDCLK low time	t_2 SR	50	—	500000	ns	—
SWDIO input setup to SWDCLK rising edge	t_3 SR	10	—	—	ns	—
SWDIO input hold after SWDCLK rising edge	t_4 SR	10	—	—	ns	—
SWDIO output valid time after SWDCLK rising edge	t_5 CC	—	—	68	ns	$C_L = 50$ pF
		—	—	62	ns	$C_L = 30$ pF
SWDIO output hold time from SWDCLK rising edge	t_6 CC	4	—	—	ns	

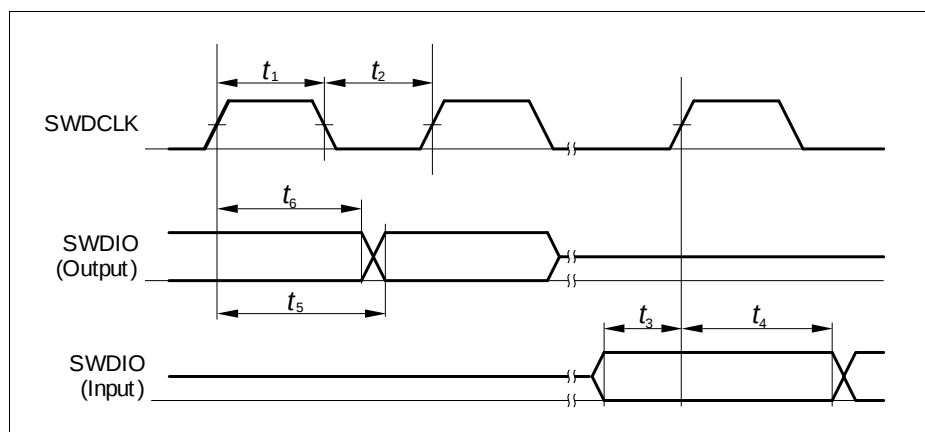


Figure 21 SWD Timing

3.3.6 Peripheral Timings

Note: These parameters are not subject to production test, but verified by design and/or characterization.

3.3.6.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: Operating Conditions apply.

Table 29 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK} CC	62.5	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	80	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	0	–	–	ns	
Data output DOUT[3:0] valid time	t_3 CC	-10	–	10	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	80	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	0	–	–	ns	

Table 32 USIC IIC Fast Mode Timing¹⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Fall time of both SDA and SCL	t_1 CC/SR	20 + 0.1 * C _b 2)	-	300	ns	
Rise time of both SDA and SCL	t_2 CC/SR	20 + 0.1 * C _b	-	300	ns	
Data hold time	t_3 CC/SR	0	-	-	µs	
Data set-up time	t_4 CC/SR	100	-	-	ns	
LOW period of SCL clock	t_5 CC/SR	1.3	-	-	µs	
HIGH period of SCL clock	t_6 CC/SR	0.6	-	-	µs	
Hold time for (repeated) START condition	t_7 CC/SR	0.6	-	-	µs	
Set-up time for repeated START condition	t_8 CC/SR	0.6	-	-	µs	
Set-up time for STOP condition	t_9 CC/SR	0.6	-	-	µs	
Bus free time between a STOP and START condition	t_{10} CC/SR	1.3	-	-	µs	
Capacitive load for each bus line	C _b SR	-	-	400	pF	

1) Due to the wired-AND configuration of an IIC bus system, the port drivers of the SCL and SDA signal lines need to operate in open-drain mode. The high level on these lines must be held by an external pull-up device, approximately 10 kOhm for operation at 100 kbit/s, approximately 2 kOhm for operation at 400 kbit/s.

2) C_b refers to the total capacitance of one bus line in pF.

Package and Reliability

The difference between junction temperature and ambient temperature is determined by

$$\Delta T = (P_{\text{INT}} + P_{\text{IOSTAT}} + P_{\text{IODYN}}) \times R_{\Theta JA}$$

The internal power consumption is defined as

$$P_{\text{INT}} = V_{\text{DDP}} \times I_{\text{DDP}} \text{ (switching current and leakage current).}$$

The static external power consumption caused by the output drivers is defined as

$$P_{\text{IOSTAT}} = \Sigma((V_{\text{DDP}} - V_{\text{OH}}) \times I_{\text{OH}}) + \Sigma(V_{\text{OL}} \times I_{\text{OL}})$$

The dynamic external power consumption caused by the output drivers (P_{IODYN}) depends on the capacitive load connected to the respective pins and their switching frequencies.

If the total power dissipation for a given system configuration exceeds the defined limit, countermeasures must be taken to ensure proper system operation:

- Reduce V_{DDP} , if possible in the system
- Reduce the system frequency
- Reduce the number of output pins
- Reduce the load on active output drivers

4.2 Package Outlines

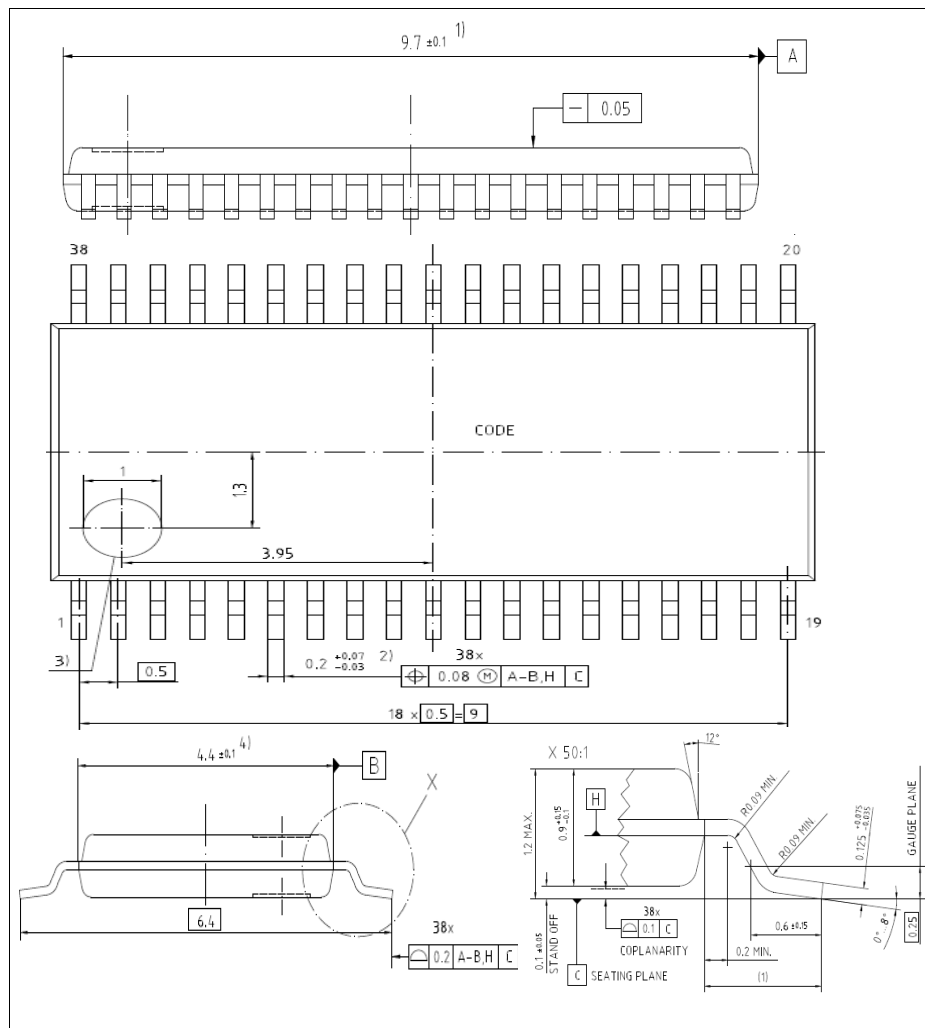


Figure 26 PG-TSSOP-38-9

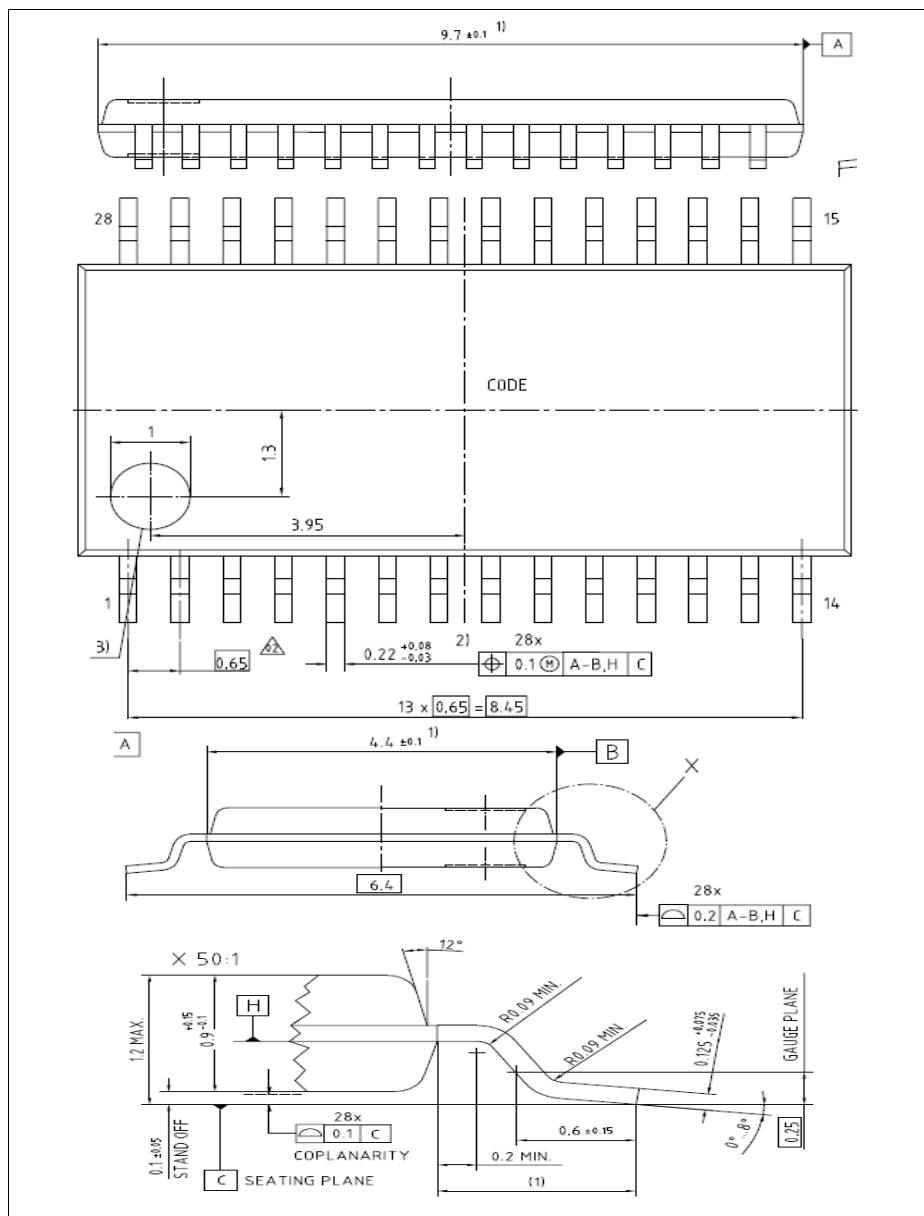


Figure 27 PG-TSSOP-28-16