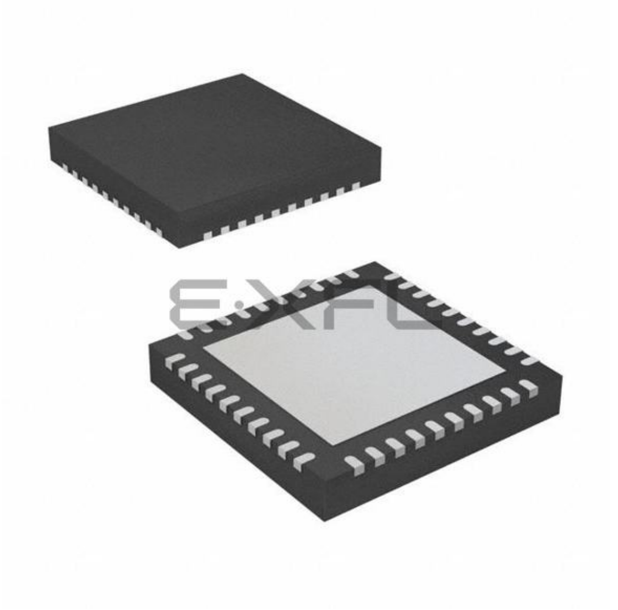
Infineon Technologies - XMC1302Q040X0200ABXUMA1 Datasheet



Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	27
Program Memory Size	200KB (200K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	PG-VQFN-40-13
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302q040x0200abxuma1

XMC1300 Data Sheet

Revision History: V1.9 2017-03

Previous Version: V1.8 2016-09

Page	Subjects
Page 10, **Page 12**	Add marking option for XMC1301-T038X0032.

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Table 1 Synopsis of XMC1300 Device Types (cont'd)

Derivative	Package	Flash Kbytes	SRAM Kbytes
XMC1302-T016X0016	PG-TSSOP-16-8	16	16
XMC1302-T016X0032	PG-TSSOP-16-8	32	16
XMC1302-T028X0016	PG-TSSOP-28-8	16	16
XMC1301-T038F0008	PG-TSSOP-38-9	8	16
XMC1301-T038F0016	PG-TSSOP-38-9	16	16
XMC1301-T038F0032	PG-TSSOP-38-9	32	16
XMC1301-T038X0032	PG-TSSOP-38-9	32	16
XMC1301-T038F0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0016	PG-TSSOP-38-9	16	16
XMC1302-T038X0032	PG-TSSOP-38-9	32	16
XMC1302-T038X0064	PG-TSSOP-38-9	64	16
XMC1302-T038X0128	PG-TSSOP-38-9	128	16
XMC1302-T038X0200	PG-TSSOP-38-9	200	16
XMC1301-Q024F0008	PG-VQFN-24-19	8	16
XMC1301-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0016	PG-VQFN-24-19	16	16
XMC1302-Q024F0032	PG-VQFN-24-19	32	16
XMC1302-Q024F0064	PG-VQFN-24-19	64	16
XMC1302-Q024X0016	PG-VQFN-24-19	16	16
XMC1302-Q024X0032	PG-VQFN-24-19	32	16
XMC1302-Q024X0064	PG-VQFN-24-19	64	16
XMC1301-Q040F0008	PG-VQFN-40-13	8	16
XMC1301-Q040F0016	PG-VQFN-40-13	16	16
XMC1301-Q040F0032	PG-VQFN-40-13	32	16
XMC1302-Q040X0016	PG-VQFN-40-13	16	16
XMC1302-Q040X0032	PG-VQFN-40-13	32	16
XMC1302-Q040X0064	PG-VQFN-40-13	64	16
XMC1302-Q040X0128	PG-VQFN-40-13	128	16
XMC1302-Q040X0200	PG-VQFN-40-13	200	16

Table 4 XMC1300 Chip Identification Number

Derivative	Value	Marking
XMC1301-T016F0008	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016F0016	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T016F0032	00013032 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T016X0008	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T016X0016	00013033 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0008	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1302-T016X0016	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T016X0032	00013033 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T028X0016	00013023 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0008	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00003000 201ED083$_H$	AB
XMC1301-T038F0016	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1301-T038F0032	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038X0032	00013013 01CF00FF 00001FF7 0000100F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1301-T038F0064	00013012 01CF00FF 00001FF7 0000100F 00000C00 00001000 00011000 201ED083$_H$	AB
XMC1302-T038X0016	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00005000 201ED083$_H$	AB
XMC1302-T038X0032	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00009000 201ED083$_H$	AB
XMC1302-T038X0064	00013013 01FF00FF 00001FF7 0000900F 00000C00 00001000 00011000 201ED083$_H$	AB

2 General Device Information

This section summarizes the logic symbols and package pin configurations with a detailed list of the functional I/O mapping.

2.1 Logic Symbols

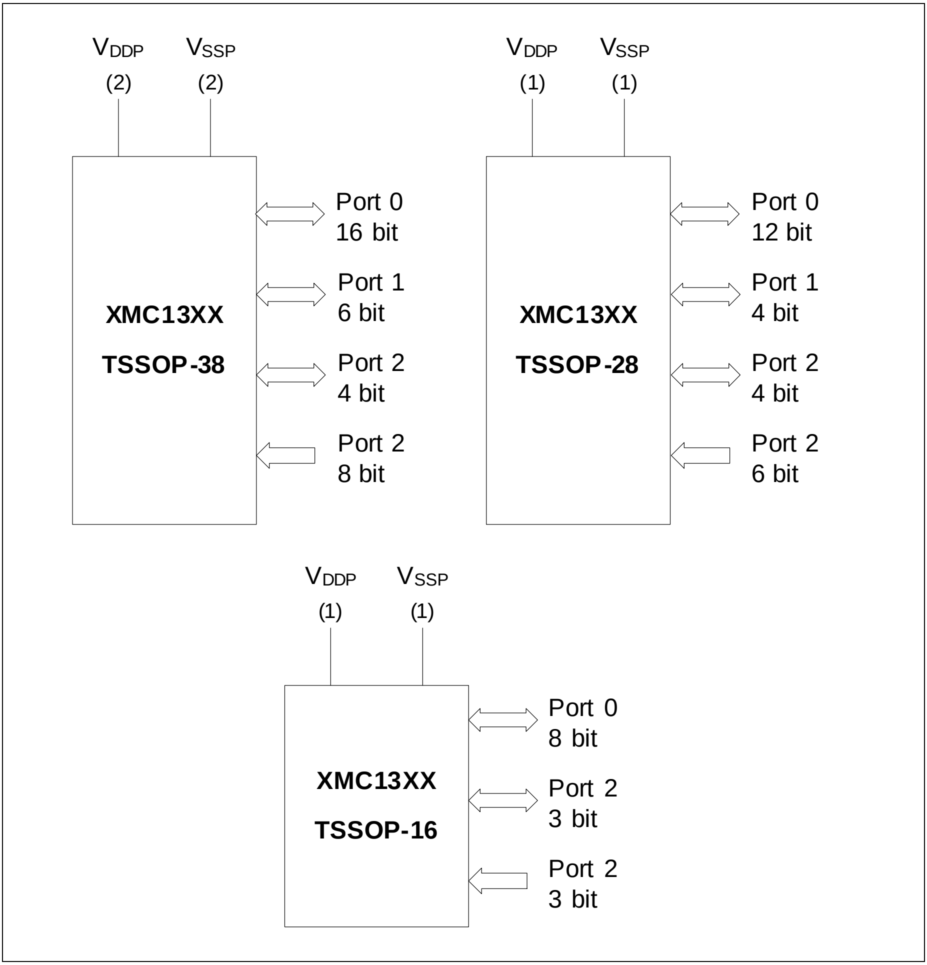

Figure 2 **XMC1300 Logic Symbol for TSSOP-38, TSSOP-28 and TSSOP-16**

2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

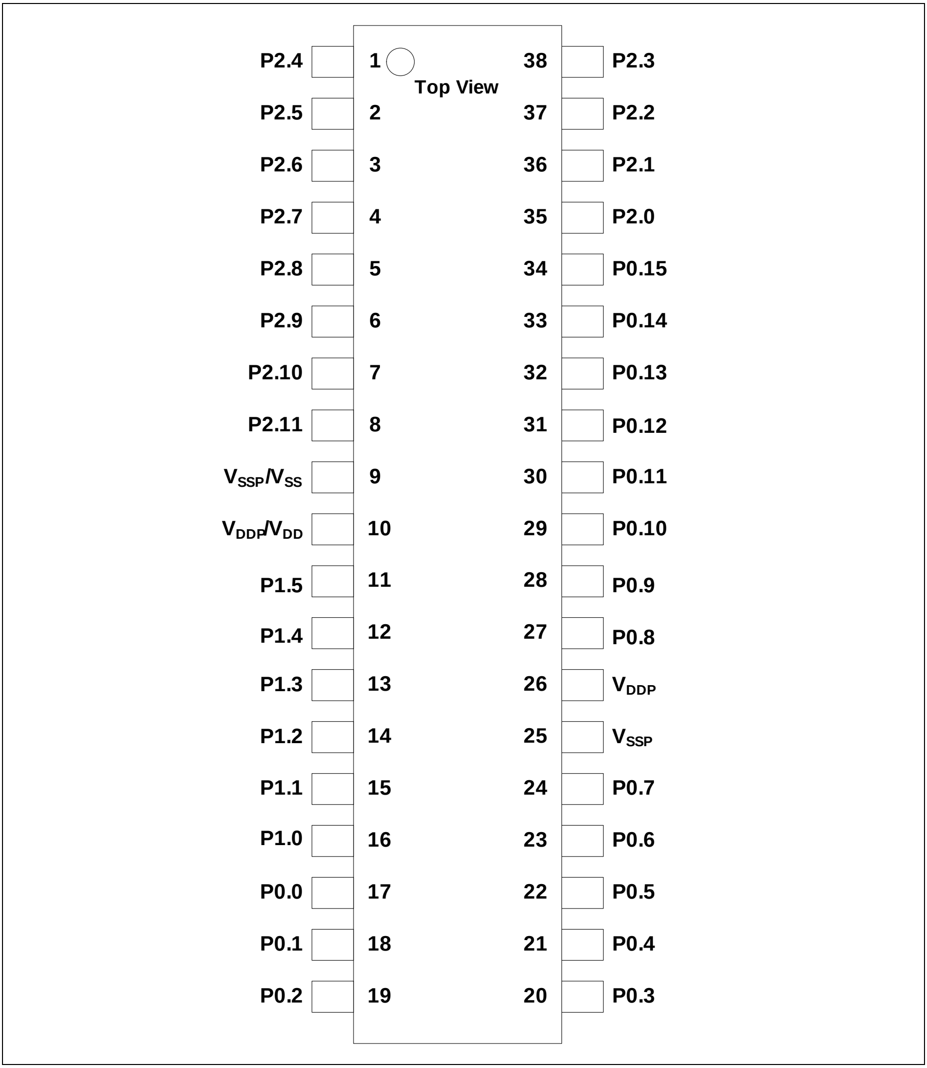

Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration (top view)

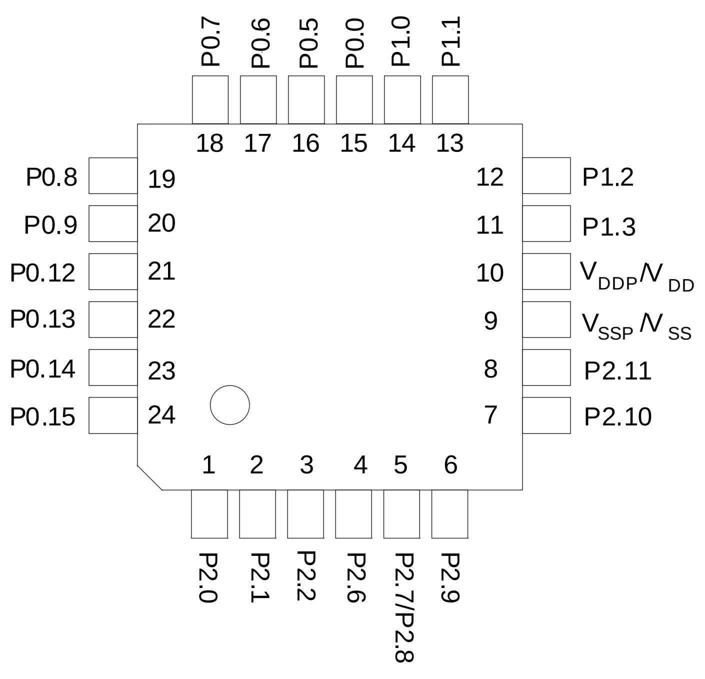

Figure 7 **XMC1300 PG-VQFN-24 Pin Configuration** (top view)

Table 9 Port I/O Functions

Function	Outputs							Inputs									
	ALT1	**ALT2**	**ALT3**	**ALT4**	**ALT5**	**ALT6**	**ALT7**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**	**Input**
P0.0	ERU0.PDOUT0		ERU0.GOUT0	CCU40.OUT0	CCU80.OUT00	USIC0_CH0.SELO0	USIC0_CH1.SELO0	BCCU0.TRAPINB	CCU40.IN0C			USIC0_CH0.DX2A	USIC0_CH1.DX2A				
P0.1	ERU0.PDOUT1		ERU0.GOUT1	CCU40.OUT1	CCU80.OUT01	BCCU0.OUT8	SCU.VDROP		CCU40.IN1C								
P0.2	ERU0.PDOUT2		ERU0.GOUT2	CCU40.OUT2	CCU80.OUT02	VADC0.EMUX02	CCU80.OUT10		CCU40.IN2C								
P0.3	ERU0.PDOUT3		ERU0.GOUT3	CCU40.OUT3	CCU80.OUT03	VADC0.EMUX01	CCU80.OUT11		CCU40.IN3C								
P0.4	BCCU0.OUT0			CCU40.OUT1	CCU80.OUT13	VADC0.EMUX00	WWDT.SERVICE_OUT		CCU80.IN0B								
P0.5	BCCU0.OUT1			CCU40.OUT0	CCU80.OUT12	ACMP2.OUT	CCU80.OUT01		CCU80.IN1B								
P0.6	BCCU0.OUT2			CCU40.OUT0	CCU80.OUT11	USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0		CCU40.IN0B			USIC0_CH1.DX0C					
P0.7	BCCU0.OUT3			CCU40.OUT1	CCU80.OUT10	USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0		CCU40.IN1B			USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C			
P0.8	BCCU0.OUT4			CCU40.OUT2	CCU80.OUT20	USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT		CCU40.IN2B			USIC0_CH0.DX1B	USIC0_CH1.DX1B				
P0.9	BCCU0.OUT5			CCU40.OUT3	CCU80.OUT21	USIC0_CH0.SELO0	USIC0_CH1.SELO0		CCU40.IN3B			USIC0_CH0.DX2B	USIC0_CH1.DX2B				
P0.10	BCCU0.OUT6			ACMP0.OUT	CCU80.OUT22	USIC0_CH0.SELO1	USIC0_CH1.SELO1		CCU80.IN2B			USIC0_CH0.DX2C	USIC0_CH1.DX2C				
P0.11	BCCU0.OUT7			USIC0_CH0.MCLKOUT	CCU80.OUT23	USIC0_CH0.SELO2	USIC0_CH1.SELO2					USIC0_CH0.DX2D	USIC0_CH1.DX2D				
P0.12	BCCU0.OUT6				CCU80.OUT33	USIC0_CH0.SELO3	CCU80.OUT20	BCCU0.TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A	USIC0_CH0.DX2E
P0.13	WWDT.SERVICE_OUT				CCU80.OUT32	USIC0_CH0.SELO4	CCU80.OUT21		CCU80.IN3B	POSIF0.IN0B		USIC0_CH0.DX2F					

Table 10 Hardware Controlled I/O Functions (cont'd)

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P2.6					$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.7					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.8					$\overline{\text{BCCU0.OUT1}}$	BCCU0.OUT1	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.9					$\overline{\text{BCCU0.OUT7}}$	BCCU0.OUT7	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.10					$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		
P2.11					$\overline{\text{BCCU0.OUT5}}$	BCCU0.OUT5		

3 Electrical Parameters

This section provides the electrical parameters which are implementation-specific for the XMC1300.

3.1 General Parameters

3.1.1 Parameter Interpretation

The parameters listed in this section represent partly the characteristics of the XMC1300 and partly its requirements on the system. To aid interpreting the parameters easily when evaluating them for a design, they are indicated by the abbreviations in the "Symbol" column:

- **CC**
  Such parameters indicate **C**ontroller **C**haracteristics, which are distinctive feature of the XMC1300 and must be regarded for a system design.
- **SR**
  Such parameters indicate **S**ystem **R**equirements, which must be provided by the application system in which the XMC1300 is designed in.

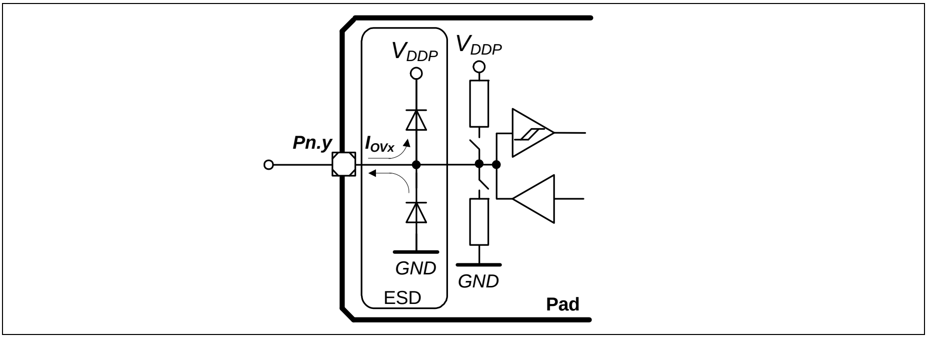

Figure 10 Input Overload Current via ESD structures

Table 13 and **Table 14** list input voltages that can be reached under overload conditions. Note that the absolute maximum input voltages as defined in the **Absolute Maximum Ratings** must not be exceeded during overload.

Table 13 PN-Junction Characterisitics for positive Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{DDP} + 0.5$ V $V_{AIN} = V_{DDP} + 0.5$ V $V_{AREF} = V_{DDP} + 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{DDP} + 0.3$ V

Table 14 PN-Junction Characterisitics for negative Overload

Pad Type	I_{OV} = 5 mA
Standard, High-current, AN/DIG_IN	$V_{IN} = V_{SS} - 0.5$ V $V_{AIN} = V_{SS} - 0.5$ V $V_{AREF} = V_{SS} - 0.5$ V
P2.[1,2,6:9,11]	$V_{INP2} = V_{SS} - 0.3$ V

Table 16 Input/Output Characteristics (Operating Conditions apply) (cont'd)

Parameter	**Symbol**		**Limit Values**		**Unit**	**Test Conditions**
			Min.	**Max.**		
Input high voltage on port pins (Standard Hysteresis)	V_{IHPS}	SR	0.7 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)
Input low voltage on port pins (Large Hysteresis)	V_{ILPL}	SR	–	0.08 × V_{DDP}	V	CMOS Mode (5 V, 3.3 V & 2.2 V)18)
Input high voltage on port pins (Large Hysteresis)	V_{IHPL}	SR	0.85 × V_{DDP}	–	V	CMOS Mode (5 V, 3.3 V & 2.2 V)18)
Rise time on High Current Pad1)	t_{HCPR}	CC	–	9	ns	50 pF @ 5 V2)
			–	12	ns	50 pF @ 3.3 V3)
			–	25	ns	50 pF @ 1.8 V4)
Fall time on High Current Pad1)	t_{HCPF}	CC	–	9	ns	50 pF @ 5 V2)
			–	12	ns	50 pF @ 3.3 V3)
			–	25	ns	50 pF @ 1.8 V4)
Rise time on Standard Pad1)	t_{R}	CC	–	12	ns	50 pF @ 5 V5)
			–	15	ns	50 pF @ 3.3 V6)
			–	31	ns	50 pF @ 1.8 V7)
Fall time on Standard Pad1)	t_{F}	CC	–	12	ns	50 pF @ 5 V5)
			–	15	ns	50 pF @ 3.3 V6)
			–	31	ns	50 pF @ 1.8 V7)

Table 17 ADC Characteristics (Operating Conditions apply)[1] (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gain settings	G_{IN} CC	1			–	GNCTRxz.GAINy = 00_B (unity gain)
		3			–	GNCTRxz.GAINy = 01_B (gain g1)
		6			–	GNCTRxz.GAINy = 10_B (gain g2)
		12			–	GNCTRxz.GAINy = 11_B (gain g3)
Sample Time	t_{sample} CC	3	–	–	1 / f_{ADC}	V_{DD} = 5.0 V
		3	–	–	1 / f_{ADC}	V_{DD} = 3.3 V
		30	–	–	1 / f_{ADC}	V_{DD} = 2.0 V
Sigma delta loop hold time	t_{SD_hold} CC	20	–	–	µs	Residual charge stored in an active sigma delta loop remains available
Conversion time in fast compare mode	t_{CF} CC	9			1 / f_{ADC}	[2]
Conversion time in 12-bit mode	t_{C12} CC	20			1 / f_{ADC}	[2]
Maximum sample rate in 12-bit mode [3]	f_{C12} CC	–	–	f_{ADC} / 42.5	–	1 sample pending
		–	–	f_{ADC} / 62.5	–	2 samples pending
Conversion time in 10-bit mode	t_{C10} CC	18			1 / f_{ADC}	[2]
Maximum sample rate in 10-bit mode [3]	f_{C10} CC	–	–	f_{ADC} / 40.5	–	1 sample pending
		–	–	f_{ADC} / 58.5	–	2 samples pending
Conversion time in 8-bit mode	t_{C8} CC	16			1 / f_{ADC}	[2]

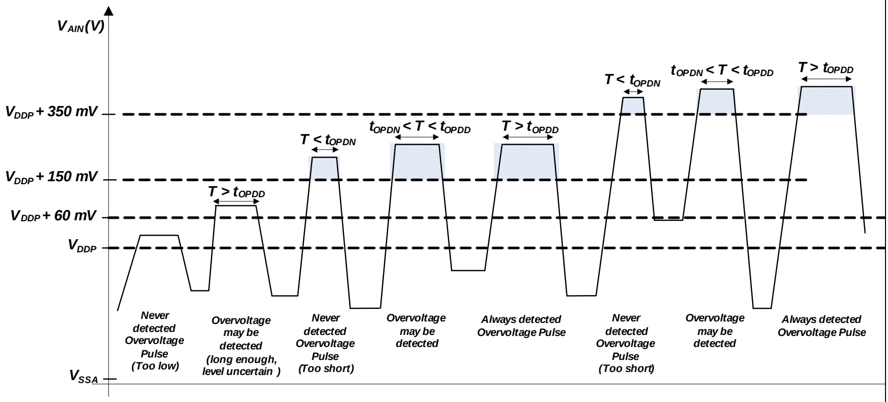

Figure 13 ORC Detection Ranges

3.2.5 Temperature Sensor Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 20 Temperature Sensor Characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Measurement time	t_M CC	–	–	10	ms	
Temperature sensor range	T_{SR} SR	-40	–	115	°C	
Sensor Accuracy[1]	T_{TSAL} CC	-6	–	6	°C	$T_J > 20°C$
		-10	–	10	°C	$0°C \leq T_J \leq 20°C$
		–	-/+8	–	°C	$T_J < 0°C$
Start-up time after enabling	t_{TSSTE} SR	–	–	15	µs	

1) The temperature sensor accuracy is independent of the supply voltage.

3.2.6 Power Supply Current

The total power supply current defined below consists of a leakage and a switching component.

Application relevant values are typically lower than those given in the following tables, and depend on the customer's system operating conditions (e.g. thermal connection or used application configurations).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 21 Power Supply Parameters; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Active mode current Peripherals enabled f_{MCLK} / f_{PCLK} in MHz[2]	I_{DDPAE} CC	–	9.2	12	mA	32 / 64
		–	8.1	-	mA	24 / 48
		–	6.6	-	mA	16 / 32
		–	5.5	-	mA	8 / 16
		–	4	-	mA	1 / 1
Active mode current Peripherals disabled f_{MCLK} / f_{PCLK} in MHz[3]	I_{DDPAD} CC	–	4.8	-	mA	32 / 64
		–	4.1	-	mA	24 / 48
		–	3.3	-	mA	16 / 32
		–	2.7	-	mA	8 / 16
		–	1.5	-	mA	1 / 1
Active mode current Code execution from RAM Flash is powered down f_{MCLK} / f_{PCLK} in MHz	I_{DDPAR} CC	–	7.3	-	mA	32 / 64
		–	6.3	-	mA	24 / 48
		–	5.2	-	mA	16 / 32
		–	4.2	-	mA	8 / 16
		–	3.3	-	mA	1 / 1
Sleep mode current Peripherals clock enabled f_{MCLK} / f_{PCLK} in MHz[4]	I_{DDPSE} CC	–	6.6	-	mA	32 / 64
			5.8	-	mA	24 / 48
			5.1	-	mA	16 / 32
			4.4	-	mA	8 / 16
			3.7	-	mA	1 / 1

3.3.3 On-Chip Oscillator Characteristics

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 25 provides the characteristics of the 64 MHz clock output from the digital controlled oscillator, DCO1 in XMC1300.

Table 25 64 MHz DCO1 Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Test Conditions
			Min.	Typ.	Max.		
Nominal frequency	f_{NOM}	CC	–	64	–	MHz	under nominal conditions[1] after trimming
Accuracy[2]	Δf_{LT}	CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (T_A = 0 °C to 85 °C)
			-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (T_A = -40 °C to 105 °C)

[1] The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

[2] The accuracy can be further improved through alternative methods, refer to XMC1000 Oscillator Handling Application Note.

Figure 20 shows the typical curves for the accuracy of DCO1, with and without calibration based on temperature sensor, respectively.

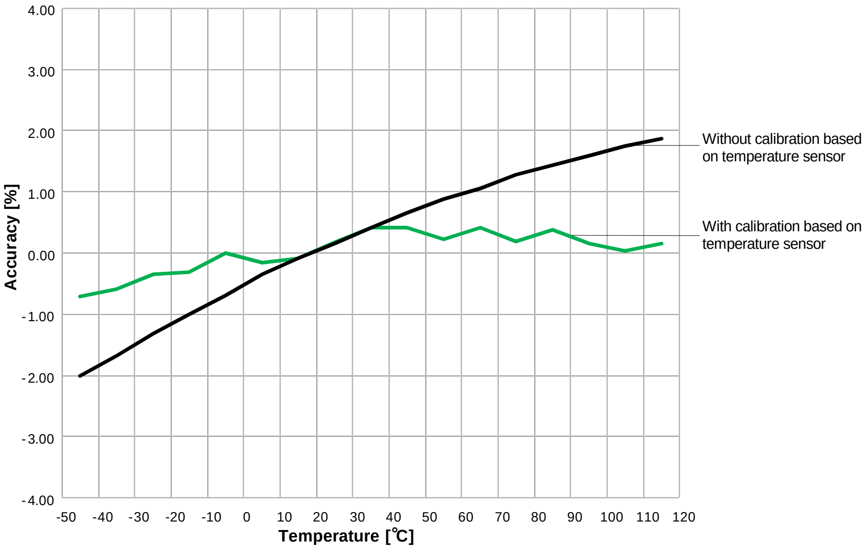

Figure 20 Typical DCO1 accuracy over temperature

Table 26 provides the characteristics of the 32 kHz clock output from digital controlled oscillators, DCO2 in XMC1300.

Table 26 32 kHz DCO2 Characteristics (Operating Conditions apply)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min.	Typ.	Max.		
Nominal frequency	f_{NOM} CC	–	32.75	–	kHz	under nominal conditions[1] after trimming
Accuracy	Δf_{LT} CC	-1.7	–	3.4	%	with respect to f_{NOM}(typ), over temperature (0 °C to 85 °C)
		-3.9	–	4.0	%	with respect to f_{NOM}(typ), over temperature (-40 °C to 105 °C)

1) The deviation is relative to the factory trimmed frequency at nominal V_{DDC} and T_A = + 25 °C.

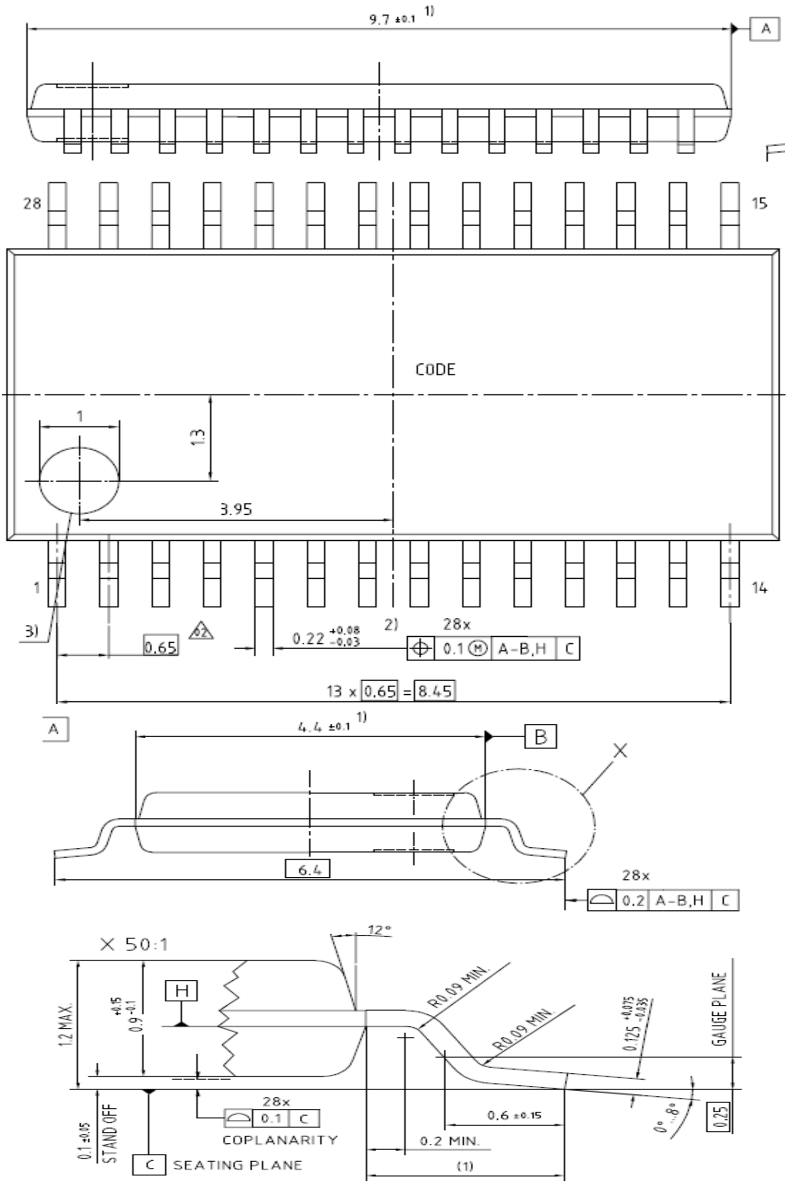

Figure 27 PG-TSSOP-28-16

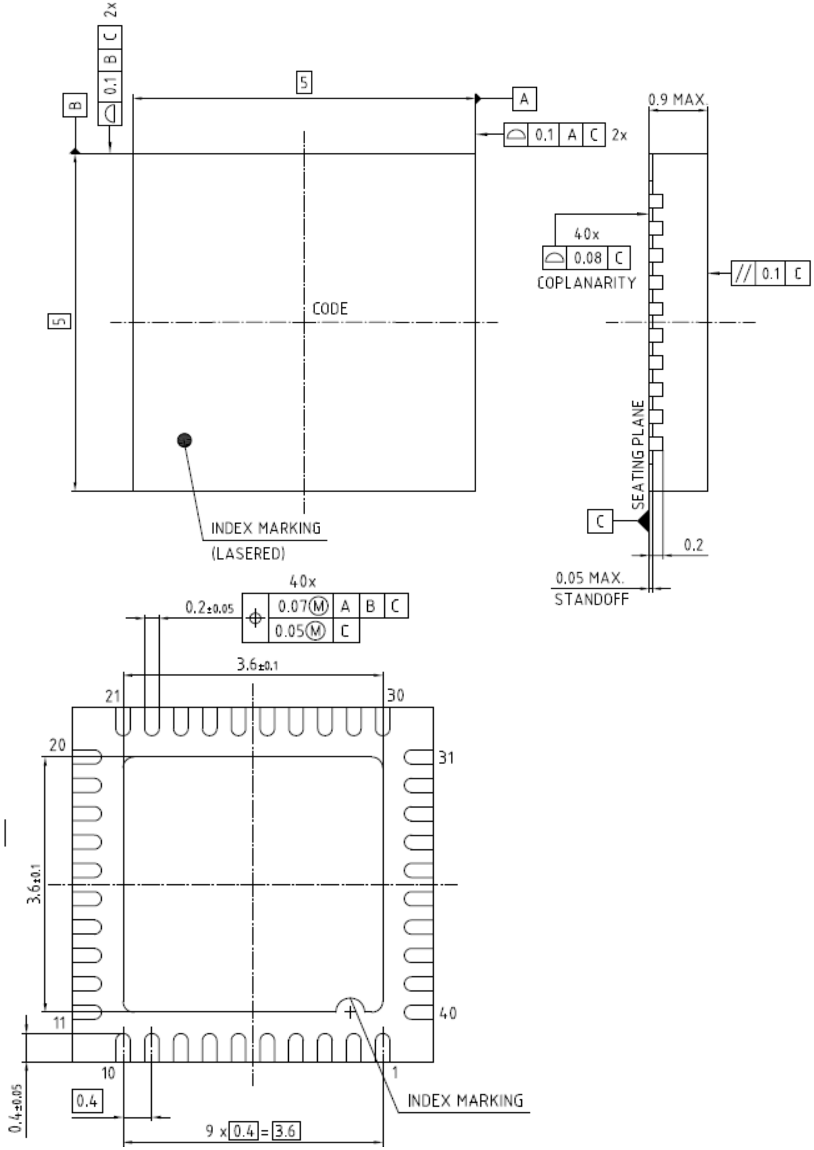

Figure 30 PG-VQFN-40-13

All dimensions in mm.

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