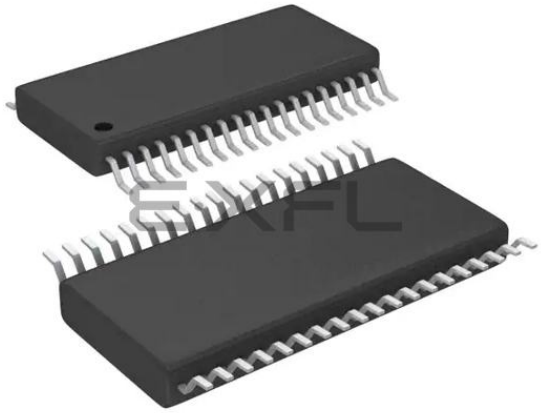
Infineon Technologies - XMC1302T038X0064ABXUMA1 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0
Core Size	32-Bit Single-Core
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	26
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	38-TFSOP (0.173", 4.40mm Width)
Supplier Device Package	PG-TSSOP-38-9
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc1302t038x0064abxuma1

Edition 2017-03

Published by
Infineon Technologies AG
81726 Munich, Germany

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2.2 Pin Configuration and Definition

The following figures summarize all pins, showing their locations on the different packages.

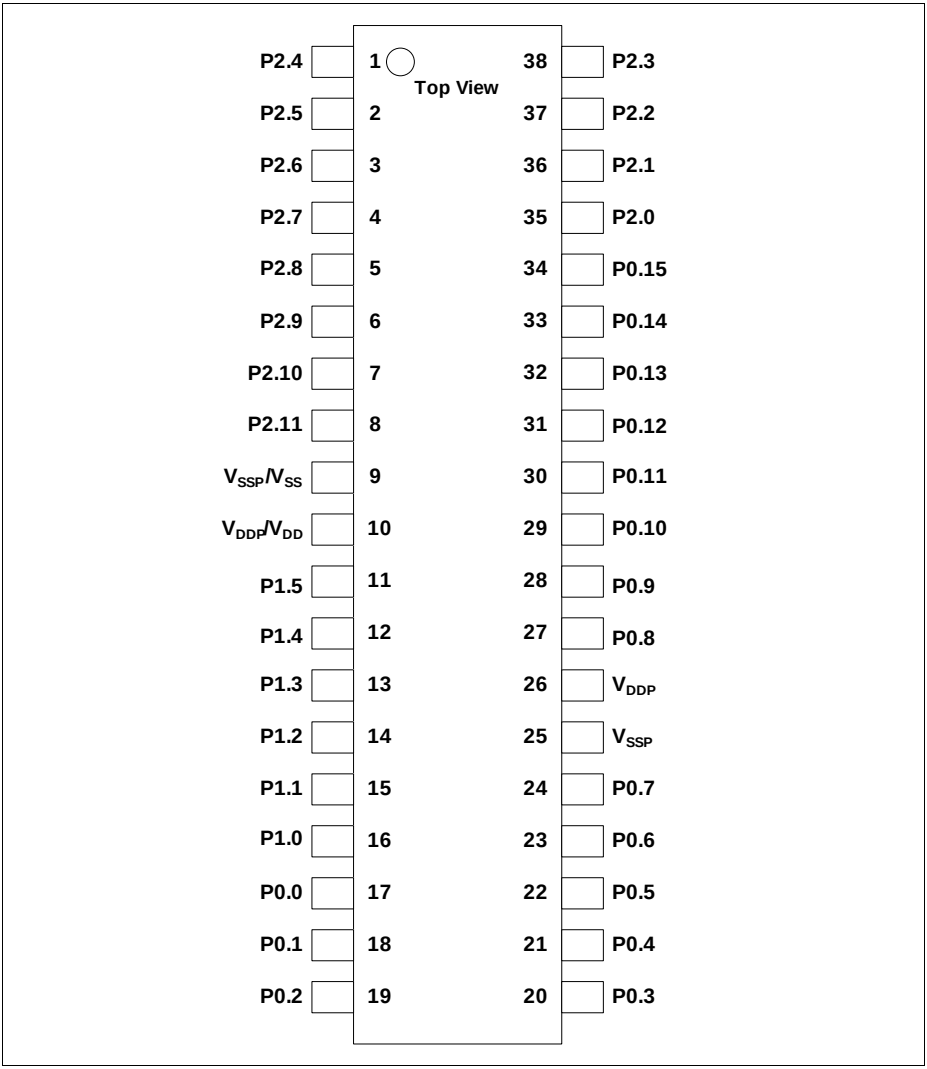

Figure 4 XMC1300 PG-TSSOP-38 Pin Configuration (top view)

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
P2.1	2	36	26	2	-	STD_IN OUT/AN	
P2.2	3	37	27	3	-	STD_IN/ AN	
P2.3	4	38	-	-	-	STD_IN/ AN	
P2.4	5	1	-	-	-	STD_IN/ AN	
P2.5	6	2	28	-	-	STD_IN/ AN	
P2.6	7	3	1	4	16	STD_IN/ AN	
P2.7	8	4	2	5	1	STD_IN/ AN	
P2.8	9	5	3	5	1	STD_IN/ AN	
P2.9	10	6	4	6	2	STD_IN/ AN	
P2.10	11	7	5	7	3	STD_IN OUT/AN	
P2.11	12	8	6	8	4	STD_IN OUT/AN	
VSS	13	9	7	9	5	Power	Supply GND, ADC reference GND
VDD	14	10	8	10	6	Power	Supply VDD, ADC reference voltage/ ORC reference voltage
VDDP	15	10	8	10	6	Power	When VDD is supplied, VDDP has to be supplied with the same voltage.

Table 6 Package Pin Mapping (cont'd)

Function	VQFN 40	TSSOP 38	TSSOP 28	VQFN 24	TSSOP 16	Pad Type	Notes
VSSP	31	25	-	-	-	Power	I/O port ground
VDDP	32	26	-	-	-	Power	I/O port supply
VSSP	Exp. Pad	-	-	Exp. Pad	-	Power	**Exposed Die Pad** The exposed die pad is connected internally to VSSP. For proper operation, it is mandatory to connect the exposed pad to the board ground. For thermal aspects, please refer to the Package and Reliability chapter.

2.2.2 Port I/O Function Description

The following general building block is used to describe the I/O functions of each PORT pin:

Table 7 Port I/O Function Description

Function	Outputs		Inputs	
	ALT1	ALTn	Input	Input
P0.0		MODA.OUT	MODC.INA	
Pn.y	MODA.OUT		MODA.INA	MODC.INB

Table 9 Port I/O Functions

Function	Outputs							Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P0.0	ERU0.PDOUT0		ERU0.GOUT0	CCU40.OUT0	CCU80.OUT00	USIC0_CH0.SELO0	USIC0_CH1.SELO0	BCCU0.TRAPINB	CCU40.IN0C			USIC0_CH0.DX2A	USIC0_CH1.DX2A				
P0.1	ERU0.PDOUT1		ERU0.GOUT1	CCU40.OUT1	CCU80.OUT01	BCCU0.OUT8	SCU.VDROP		CCU40.IN1C								
P0.2	ERU0.PDOUT2		ERU0.GOUT2	CCU40.OUT2	CCU80.OUT02	VADC0.EMUX02	CCU80.OUT10		CCU40.IN2C								
P0.3	ERU0.PDOUT3		ERU0.GOUT3	CCU40.OUT3	CCU80.OUT03	VADC0.EMUX01	CCU80.OUT11		CCU40.IN3C								
P0.4	BCCU0.OUT0			CCU40.OUT1	CCU80.OUT13	VADC0.EMUX00	WWDT.SERVICE_OUT		CCU80.IN0B								
P0.5	BCCU0.OUT1			CCU40.OUT0	CCU80.OUT12	ACMP2.OUT	CCU80.OUT01		CCU80.IN1B								
P0.6	BCCU0.OUT2			CCU40.OUT0	CCU80.OUT11	USIC0_CH1.MCLKOUT	USIC0_CH1.DOUT0		CCU40.IN0B			USIC0_CH1.DX0C					
P0.7	BCCU0.OUT3			CCU40.OUT1	CCU80.OUT10	USIC0_CH0.SCLKOUT	USIC0_CH1.DOUT0		CCU40.IN1B			USIC0_CH0.DX1C	USIC0_CH1.DX0D	USIC0_CH1.DX1C			
P0.8	BCCU0.OUT4			CCU40.OUT2	CCU80.OUT20	USIC0_CH0.SCLKOUT	USIC0_CH1.SCLKOUT		CCU40.IN2B			USIC0_CH0.DX1B	USIC0_CH1.DX1B				
P0.9	BCCU0.OUT5			CCU40.OUT3	CCU80.OUT21	USIC0_CH0.SELO0	USIC0_CH1.SELO0		CCU40.IN3B			USIC0_CH0.DX2B	USIC0_CH1.DX2B				
P0.10	BCCU0.OUT6			ACMP0.OUT	CCU80.OUT22	USIC0_CH0.SELO1	USIC0_CH1.SELO1		CCU80.IN2B			USIC0_CH0.DX2C	USIC0_CH1.DX2C				
P0.11	BCCU0.OUT7			USIC0_CH0.MCLKOUT	CCU80.OUT23	USIC0_CH0.SELO2	USIC0_CH1.SELO2					USIC0_CH0.DX2D	USIC0_CH1.DX2D				
P0.12	BCCU0.OUT6				CCU80.OUT33	USIC0_CH0.SELO3	CCU80.OUT20	BCCU0.TRAPINA	CCU40.IN0A	CCU40.IN1A	CCU40.IN2A	CCU40.IN3A	CCU80.IN0A	CCU80.IN1A	CCU80.IN2A	CCU80.IN3A	USIC0_CH0.DX2E
P0.13	WWDT.SERVICE_OUT				CCU80.OUT32	USIC0_CH0.SELO4	CCU80.OUT21		CCU80.IN3B	POSIF0.IN0B		USIC0_CH0.DX2F					

Table 9 Port I/O Functions (cont'd)

Function	Outputs							Inputs									
	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	Input	Input	Input	Input	Input	Input	Input	Input	Input	Input
P2.6								ACMP1.INN	VADC0.G0CH0		ERU0.2A1	USIC0_CH0.DX3E	USIC0_CH0.DX4E	USIC0_CH1.DX5D	ORC4.AIN		
P2.7								ACMP1.INP	VADC0.G1CH1		ERU0.3A1	USIC0_CH0.DX5C	USIC0_CH1.DX3D	USIC0_CH1.DX4D	ORC5.AIN		
P2.8								ACMP0.INN	VADC0.G0CH1	VADC0.G1CH0	ERU0.3B1	USIC0_CH0.DX3D	USIC0_CH0.DX4D	USIC0_CH1.DX5C	ORC6.AIN		
P2.9								ACMP0.INP	VADC0.G0CH2	VADC0.G1CH4	ERU0.3B0	USIC0_CH0.DX5A	USIC0_CH1.DX3B	USIC0_CH1.DX4B	ORC7.AIN		
P2.10	ERU0.PDOUT1	CCU40.OUT2	ERU0.GOUT1		CCU80.OUT30	ACMP0.OUT	USIC0_CH1.DOUT0		VADC0.G0CH3	VADC0.G1CH2	ERU0.2B0	USIC0_CH0.DX3C	USIC0_CH0.DX4C	USIC0_CH1.DX0F			
P2.11	ERU0.PDOUT0	CCU40.OUT3	ERU0.GOUT0		CCU80.OUT31	USIC0_CH1.SCLKOUT	USIC0_CH1.DOUT0	ACMP.REF	VADC0.G0CH4	VADC0.G1CH3	ERU0.2B1	USIC0_CH1.DX0E	USIC0_CH1.DX1E				

Table 10 Hardware Controlled I/O Functions (cont'd)

Function	Outputs		Inputs		Pull Control			
	HWO0	HWO1	HWI0	HWI1	HW0_PD	HW0_PU	HW1_PD	HW1_PU
P2.6					$\overline{\text{BCCU0.OUT2}}$	BCCU0.OUT2	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.7					$\overline{\text{BCCU0.OUT8}}$	BCCU0.OUT8	$\overline{\text{CCU40.OUT3}}$	CCU40.OUT3
P2.8					$\overline{\text{BCCU0.OUT1}}$	BCCU0.OUT1	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.9					$\overline{\text{BCCU0.OUT7}}$	BCCU0.OUT7	$\overline{\text{CCU40.OUT2}}$	CCU40.OUT2
P2.10					$\overline{\text{BCCU0.OUT4}}$	BCCU0.OUT4		
P2.11					$\overline{\text{BCCU0.OUT5}}$	BCCU0.OUT5		

3.1.4 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC1300. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Table 15 Operating Conditions Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Ambient Temperature	T_A	SR	-40	–	85	°C	Temp. Range F
			-40	–	105	°C	Temp. Range X
Digital supply voltage[1)]	V_{DDP}	SR	1.8	–	5.5	V	
MCLK Frequency	f_{MCLK}	CC	–	–	33.2	MHz	CPU clock
PCLK Frequency	f_{PCLK}	CC	–	–	66.4	MHz	Peripherals clock
Short circuit current of digital outputs	I_{SC}	SR	-5	–	5	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D}	SR	–	–	25	mA	

1) See also the Supply Monitoring thresholds, **Chapter 3.3.2**.

3.2.2 Analog to Digital Converters (ADC)

Table 17 shows the Analog to Digital Converter (ADC) characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 17 ADC Characteristics (Operating Conditions apply)[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Supply voltage range (internal reference)	V_{DD_int} SR	2.0	–	3.0	V	SHSCFG.AREF = 11_B CALCTR.CALGNSTC = $0C_H$
		3.0	–	5.5	V	SHSCFG.AREF = 10_B
Supply voltage range (external reference)	V_{DD_ext} SR	3.0	–	5.5	V	SHSCFG.AREF = 00_B
Analog input voltage range	V_{AIN} SR	V_{SSP} - 0.05	–	V_{DDP} + 0.05	V	
Auxiliary analog reference ground	V_{REFGND} SR	V_{SSP} - 0.05	–	1.0	V	G0CH0
		V_{SSP} - 0.05	–	0.2	V	G1CH0
Internal reference voltage (full scale value)	V_{REFINT} CC	5			V	
Switched capacitance of an analog input	C_{AINS} CC	–	1.2	2	pF	GNCTRxz.GAINy = 00_B (unity gain)
		–	1.2	2	pF	GNCTRxz.GAINy = 01_B (gain g1)
		–	4.5	6	pF	GNCTRxz.GAINy = 10_B (gain g2)
		–	4.5	6	pF	GNCTRxz.GAINy = 11_B (gain g3)
Total capacitance of an analog input	C_{AINT} CC	–	–	10	pF	
Total capacitance of the reference input	C_{AREFT} CC	–	–	10	pF	

3.2.3 Out of Range Comparator (ORC) Characteristics

The Out-of-Range Comparator (ORC) triggers on analog input voltages (V_{AIN}) above the V_{DDP} on selected input pins (ORCx.AIN) and generates a service request trigger (ORCx.OUT).

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 18 Out of Range Comparator (ORC) Characteristics (Operating Conditions apply; V_{DDP} = 3.0 V - 5.5 V; C_L = 0.25 pF)

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DC Switching Level	V_{ODC}	CC	54	–	183	mV	$VAIN \geq V_{DDP} + V_{ODC}$
Hysteresis	V_{OHYS}	CC	15	–	54	mV	
Always detected Overvoltage Pulse	t_{OPDD}	CC	103	–	-	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			88	–	-	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Never detected Overvoltage Pulse	t_{OPDN}	CC	–	–	21	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			–	–	11	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Detection Delay of a persistent Overvoltage	t_{ODD}	CC	39	–	132	ns	$V_{AIN} \geq V_{DDP}$ + 150 mV
			31	–	121	ns	$V_{AIN} \geq V_{DDP}$ + 350 mV
Release Delay	t_{ORD}	CC	44	–	240	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 5 V
			57	–	340	ns	$V_{AIN} \leq V_{DDP}$; V_{DDP} = 3.3 V
Enable Delay	t_{OED}	CC	–	–	300	ns	ORCCTRL.ENORCx = 1

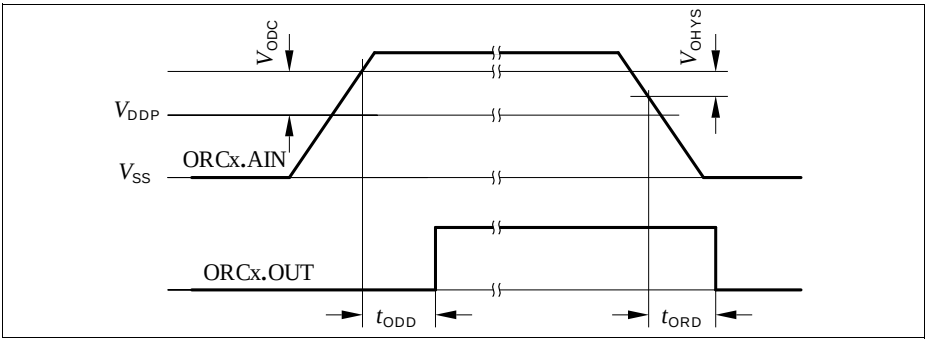

Figure 12 ORCx.OUT Trigger Generation

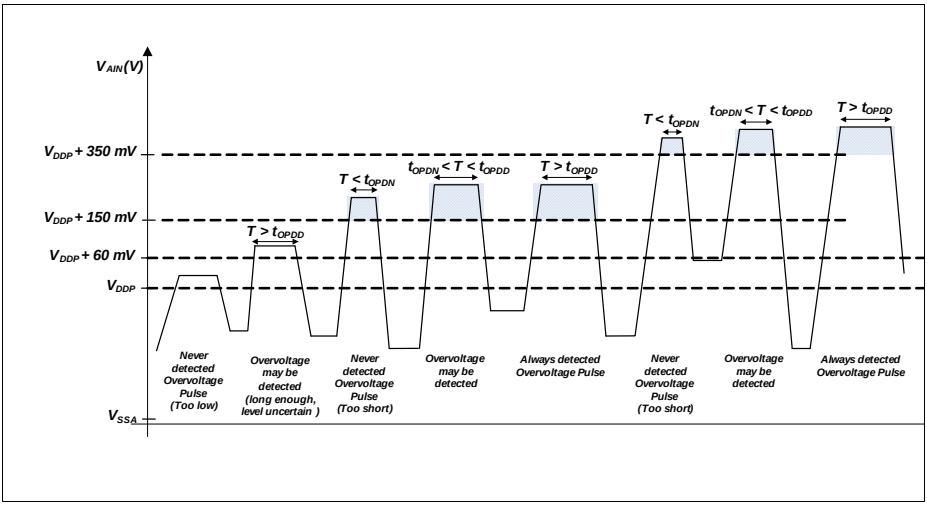

Figure 13 ORC Detection Ranges

3.2.4 Analog Comparator Characteristics

Table 19 below shows the Analog Comparator characteristics.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 19 Analog Comparator Characteristics (Operating Conditions apply)

Parameter	Symbol		Limit Values			Unit	Notes/ Test Conditions
			Min.	Typ.	Max.		
Input Voltage	V_{CMP}	SR	-0.05	–	V_{DDP} + 0.05	V	
Input Offset	V_{CMPOFF}	CC	–	+/-3	–	mV	High power mode ΔV_{CMP} < 200 mV
			–	+/-20	–	mV	Low power mode ΔV_{CMP} < 200 mV
Propagation Delay[1)]	t_{PDELAY}	CC	–	25	–	ns	High power mode, ΔV_{CMP} = 100 mV
			–	80	–	ns	High power mode, ΔV_{CMP} = 25 mV
			–	250	–	ns	Low power mode, ΔV_{CMP} = 100 mV
			–	700	–	ns	Low power mode, ΔV_{CMP} = 25 mV
Current Consumption	I_{ACMP}	CC	–	100	–	µA	First active ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	66	–	µA	Each additional ACMP in high power mode, ΔV_{CMP} > 30 mV
			–	10	–	µA	First active ACMP in low power mode
			–	6	–	µA	Each additional ACMP in low power mode
Input Hysteresis	V_{HYS}	CC	–	+/-15	–	mV	
Filter Delay[1)]	t_{FDELAY}	CC	–	5	–	ns	

1) Total Analog Comparator Delay is the sum of Propagation Delay and Filter Delay.

Table 21 Power Supply Parameters; V_{DDP} = 5V

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.[1]	Max.		
Sleep mode current Peripherals clock disabled Flash active f_{MCLK} / f_{PCLK} in MHz[5]	I_{DDPSD} CC	–	1.8	-	mA	32 / 64
			1.7	-	mA	24 / 48
			1.6	-	mA	16 / 32
			1.5	-	mA	8 / 16
			1.4	-	mA	1 / 1
Sleep mode current Peripherals clock disabled Flash powered down f_{MCLK} / f_{PCLK} in MHz[6]	I_{DDPSR} CC	–	1.2	-	mA	32 / 64
			1.1	-	mA	24 / 48
			1.0	-	mA	16 / 32
			0.8	-	mA	8 / 16
			0.7	-	mA	1 / 1
Deep Sleep mode current[7]	I_{DDPDS} CC	–	0.24	-	mA	
Wake-up time from Sleep to Active mode[8]	t_{SSA} CC	–	6	-	cycles	
Wake-up time from Deep Sleep to Active mode[9]	t_{DSA} CC	–	280	-	µsec	

1) The typical values are measured at T_A = + 25 °C and VDDP = 5 V.
2) CPU and all peripherals clock enabled, Flash is in active mode.
3) CPU enabled, all peripherals clock disabled, Flash is in active mode.
4) CPU in sleep, all peripherals clock enabled and Flash is in active mode.
5) CPU in sleep, Flash is in active mode.
6) CPU in sleep, Flash is powered down and code executed from RAM after wake-up.
7) CPU in sleep, peripherals clock disabled, Flash is powered down and code executed from RAM after wake-up.
8) CPU in sleep, Flash is in active mode during sleep mode.
9) CPU in sleep, Flash is in powered down mode during deep sleep mode.

Table 24 Power-Up and Supply Monitoring Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
V_{DDP} brownout reset voltage	V_{DDPBO} CC	1.55	1.62	1.75	V	calibrated, before user code starts running
V_{DDP} voltage to ensure defined pad states	V_{DDPPA} CC	–	1.0	–	V	
Start-up time from power-on reset	t_{SSW} SR	–	320	–	µs	Time to the first user code instruction[3)]
BMI program time	t_{BMI} SR	–	8.25	–	ms	Time taken from a user-triggered system reset after BMI installation is is requested

1) A capacitor of at least 100 nF has to be added between VDDP and VSSP to fulfill the requirement as stated for this parameter.

2) Valid for a 100 nF buffer capacitor connected to supply pin where current from capacitor is forwarded only to the chip. A larger capacitor value has to be chosen if the power source sink a current.

3) This values does not include the ramp-up time. During startup firmware execution, MCLK is running at 32 MHz and the clocks to peripheral as specified in register CGATSTAT0 are gated.

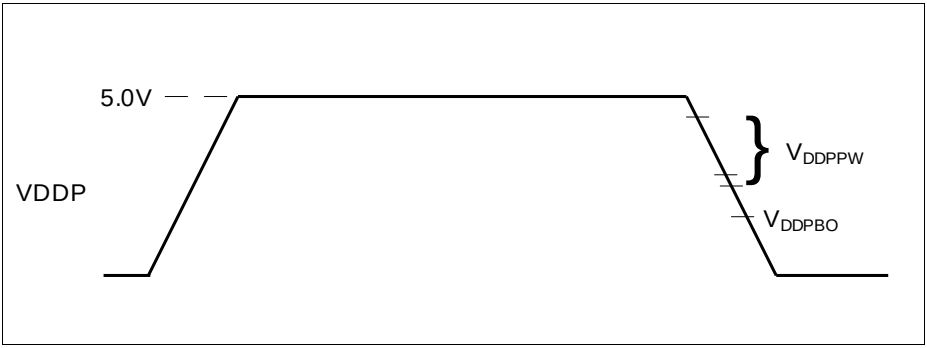

Figure 19 Supply Threshold Parameters

3.3.5 SPD Timing Requirements

The optimum SPD decision time between 0_B and 1_B is 0.75 µs. With this value the system has maximum robustness against frequency deviations of the sampling clock on tool and on device side. However it is not always possible to exactly match this value with the given constraints for the sample clock. For instance for a oversampling rate of 4, the sample clock will be 8 MHz and in this case the closest possible effective decision time is 5.5 clock cycles (0.69 µs).

Table 28 Optimum Number of Sample Clocks for SPD

Sample Freq.	Sampling Factor	Sample Clocks 0_B	Sample Clocks 1_B	Effective Decision Time[1)]	Remark
8 MHz	4	1 to 5	6 to 12	0.69 µs	The other closest option (0.81 µs) for the effective decision time is less robust.

1) Nominal sample frequency period multiplied with 0.5 + (max. number of 0_B sample clocks)

For a balanced distribution of the timing robustness of SPD between tool and device, the timing requirements for the tool are:

- Frequency deviation of the sample clock is +/- 5%
- Effective decision time is between 0.69 µs and 0.75 µs (calculated with nominal sample frequency)

Table 30 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK}	SR	125	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1)]	t_{10}	SR	10	–	–	ns	
Select input DX2 hold after last clock input DX1 receive edge[1)]	t_{11}	SR	10	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge[1)]	t_{12}	SR	10	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge[1)]	t_{13}	SR	10	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	-	–	80	ns	

1) These input timings are valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

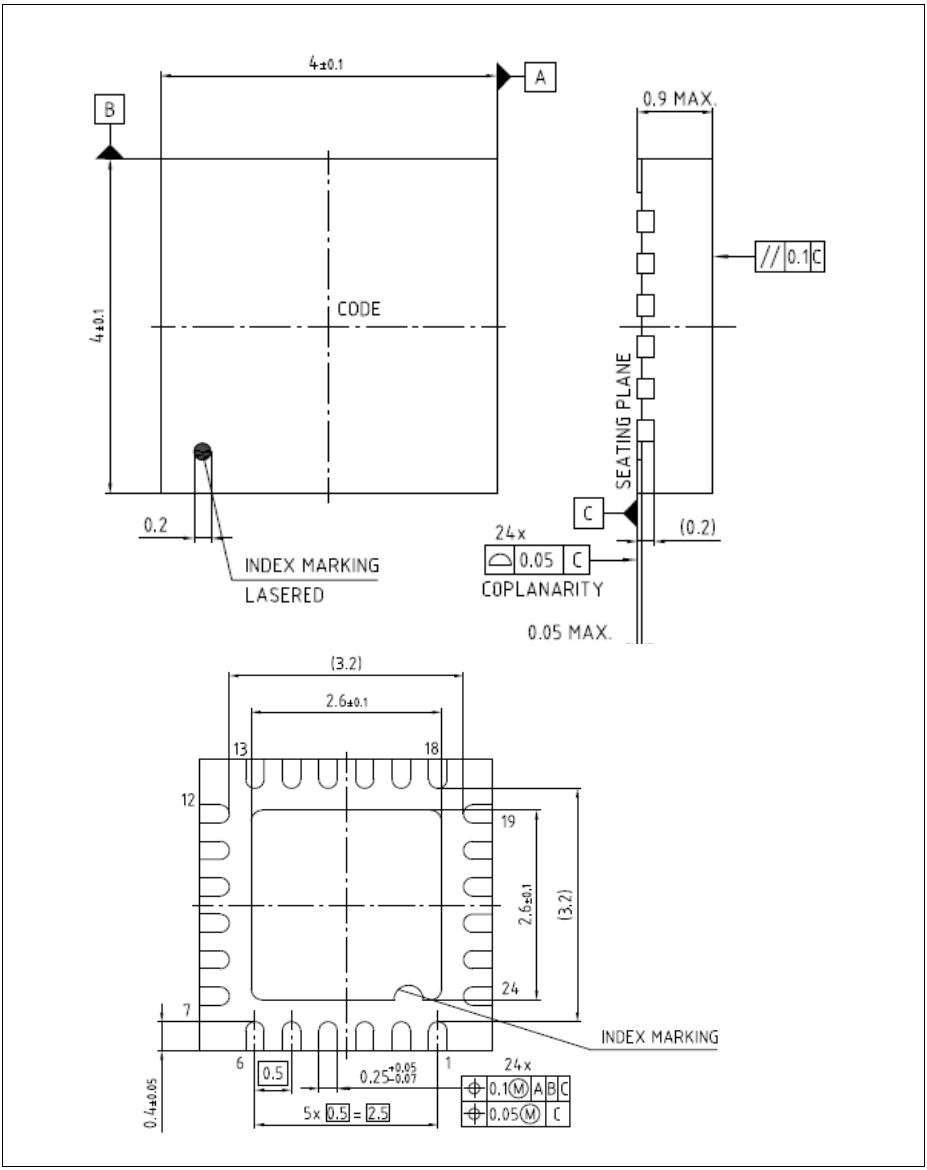

Figure 29 PG-VQFN-24-19

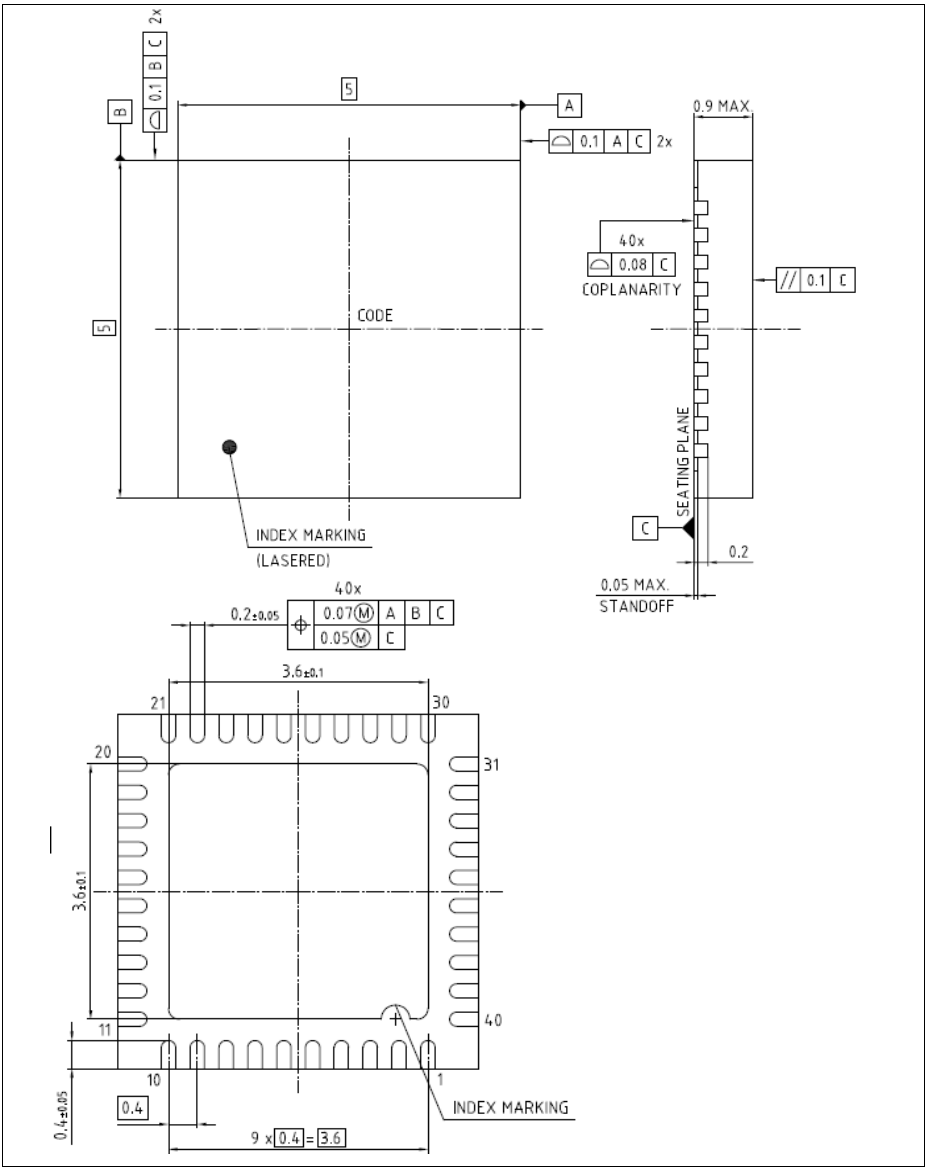

Figure 30 PG-VQFN-40-13

All dimensions in mm.