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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Details	
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-125-jne1

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



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1. Product Lineup

	Features	MB90598G	MB90V595G					
Classific	ation	Mask ROM product	Evaluation product					
ROM siz	e	128 Kbytes	128 Kbytes Boot block Hard-wired reset vector	None				
RAM size	e	4 Kbytes	4 Kbytes	6 Kbytes				
Emulator	r-specific power supply	-		None				
CPU fun	ctions	Interrupt processing time: 1.5 µs	Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz)					
UART0		Clock synchronized transmission (500 K/1 M/2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connectio						
UART1(SCI)	Clock synchronized transmission (62.5 K/125 Clock asynchronized transmission (1202/240 Transmission can be performed by bi-directio	4/4808/9615/31250 bps)	ster/slave connection.				
8/10-bit /	8/10-bit A/D converter 8/10-bit A/D converter Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)							
8/16-bit f (6 chann	PPG timers els)	ers Number of channels: 6 (8/16-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ² , fsys/2 ⁴ (fsys = system clock frequency) 128μs (fosc = 4MHz: oscillation clock frequency)						
Number of channels: 2 0peration clock frequency: fsys/2 ¹ , fsys/2 ³ , fsys/2 ⁵ (fsys = System clock frequency) Supports External Event Count function				ency)				
16-bit	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register						
I/O tim- er	Input captures	Number of channels: 4 Rewriting a register value upon a pin input (ri						



Features	MB90598G	MB90F598G	MB90V595G					
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90598G/F598G:TSEG2 ≥ RSJW							
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel	our high current outputs for each channel Synchronized two 8-bit PWM's for each channel						
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" le	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.						
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first							
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57 (at oscillation of 4 MHz, minimum value)	7.23 ms, 458.75 ms						
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics. Inc.							
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by							
Process	CMOS							
Power supply voltage for opera- tion*2	+5 V±10 %							
Package	QFP-100	QFP-100 PGA-256						

*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.

Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2: Varies with conditions such as the operating frequency. (See "Electrical Characteristics.")



Pin no.	Pin name	Circuit type	Function		
20	P50	D	General purpose IO		
28	SIN2	D	SIN Input for the Serial IO		
29 to 32	P51 to P54	D	General purpose IO		
291032	INT4 to INT7	D	External interrupt input for INT4 to INT7		
33	P55	D	General purpose IO		
	ADTG	ם	Input for the external trigger of the A/D Converter		
38 to 41	P60 to P63	E	General purpose IO		
30 10 41	AN0 to AN3	L	Inputs for the A/D Converter		
43 to 46	P64 to P67	E	General purpose IO		
43 10 40	AN4 to AN7	L	Inputs for the A/D Converter		
47	P56	D	General purpose IO		
47	TIN0	ם	TIN input for the 16-bit Reload Timer 0		
48	P57	D	General purpose IO		
40	ΤΟΤΟ	D	TOT output for the 16-bit Reload Timer 0		
	P70 to P73		General purpose IO		
54 to 57	PWM1P0 PWM1M0 PWM2P0 PWM2M0	F	Output for Stepper Motor Controller channel 0		
	P74 to P77		General purpose IO		
59 to 62	PWM1P1 PWM1M1 PWM2P1 PWM2M1	F	Output for Stepper Motor Controller channel 1		
	P80 to P83		General purpose IO		
64 to 67	PWM1P2 PWM1M2 PWM2P2 PWM2M2	F	Output for Stepper Motor Controller channel 2		
	P84 to P87		General purpose IO		
69 to 72	PWM1P3 PWM1M3 PWM2P3 PWM2M3	F	Output for Stepper Motor Controller channel 3		
74	P90	5	General purpose IO		
74	ТХ	D	TX output for CAN Interface		
75	P91	6	General purpose IO		
75	RX	D	RX input for CAN Interface		



Pin no.	Pin name	Circuit type	Function	
76	P92	D	General purpose IO	
70	INT0		External interrupt input for INT0	
78 to 80	P93 to P95	D	General purpose IO	
70 10 00	INT1 to INT3		External interrupt input for INT1 to INT3	
58, 68	DVcc	_	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)	
53, 63, 73	DVss	_	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)	
34	AVcc	Power supply	Dedicated power supply pin for the A/D Converter	
37	AVss	Power supply	Dedicated ground pin for the A/D Converter	
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter	
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter	
49, 50	MD0 MD1	С	Operating mode selection input pins. These pins should be connected to V_{CC} or $V_{SS}.$	
51	MD2	н	Operating mode selection input pin. This pin should be connected to $V_{\mbox{\scriptsize CC}}$ or $V_{\mbox{\scriptsize SS}}.$	
27	С	_	External capacitor pin. A capacitor of $0.1 \mu F$ should be connected to this pin and $V_{ss}.$	
23, 84	Vcc	Power supply	Power supply pins (5.0 V).	
11, 42, 81	Vss	Power supply	Ground pins (0.0 V).	

4. I/O Circuit Type







Circuit Type	Circuit	Remarks
		CMOS high current output
		CMOS Hysteresis input
	P-ch	
	High current	
F	N-ch	
	R	
	L _W HYS	
		■ CMOS output
	Vcc	CMOS Hysteresis input
	P-ch	■ TTL input
		(MB90F598G, only in Flash mode)
	N-ch	
G		
Ũ		
	R	
	HYS	
	R	
		 Hysteresis input
		■ Hysteresis input Pull-down Resistor: 50 kΩ approx.
		(except MB90F598G)
н		
	R	
	· · · ·	



5. Handling Devices

(1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding Vcc or an voltage below Vss is applied to input or output pins or a voltage exceeding the rating is applied across Vcc and Vss.

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AVcc, AVRH, DVcc) and analog input voltages not exceed the digital voltage (Vcc).

(2) Treatment of Unused Pins

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 k Ω resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

(3) Using external clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.



(4) Power supply pins (Vcc/Vss)

In products with multiple V_{cc} or V_{ss} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)

Make sure to connect V_{cc} and V_{ss} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μ F between V_{cc} and V_{ss} pins near the device.





(5) Pull-up/down resistors

The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (Vcc).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AVcc (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to AVcc = Vcc, AVss = AVRH = DVcc = Vss.

(9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

(10) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at

50 µs or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

■ If RST pin is "H", the outputs become indeterminate.

If \overline{RST} pin is "L", the outputs become high-impedance.





6. Block Diagram





9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Register Abbreviation Access		Initial Value	
001A60н			D 444	~~~~~	
001А61 н	DLC register 0	DLCR0	R/W	XXXXB	
001A62н			DAA		
001A63н	DLC register 1	DLCR1	R/W	ХХХХв	
001A64н			DAA	VVV-	
001A65н	DLC register 2	DLCR2	R/W	ХХХХв	
001A66н	- DLC register 3	DLCR3	R/W	ХХХХв	
001А67 н	DLC register 3	DLCR3	R/VV	XXXAB	
001A68н	DLC register 4		DAM	VVV-	
001A69н	DLC register 4	DLCR4	R/W	ХХХХв	
001А6Ан	DLC register 5	DLCR5	R/W	ХХХХв	
001A6Bн	DLC register 5	DLCRS	r./vv		
001A6Cн	DLC register 6	DLCR6	R/W	ХХХХв	
001A6DH	DLC register o	DLCRO	r./vv		
001A6Eн	DLC register 7	DLCR7	R/W	ХХХХв	
001A6Fн		DLCR7	r./vv		
001А70 н	DLC register 8	DLCR8	R/W	XXXX	
001A71 н	DLC register o	DECKO		^	
001А72 н	DLC register 9	DLCR9	R/W	XXXXB	
001А73 н	DLC register 9	DLCK9	FN/ V V		
001A74н	DLC register 10	DLCR10	R/W	XXXXB	
001A75н		DECKTO	10/00		
001A76н	DLC register 11	DLCR11	R/W	XXXXB	
001А77 н		DECKT	10/00		
001A78н	DLC register 12	DLCR12	R/W	XXXXB	
001A79н		DEORTZ	10,00		
001А7Ан	DLC register 13	DLCR13	R/W	XXXXB	
001A7Bн		DEORIG			
001A7Cн	DLC register 14	DLCR14	R/W	ХХХХв	
001A7DH		DLOR 14			
001A7Eн	DLC register 15	DLCR15	R/W	XXXXB	
001A7Fн	DLC register 15 DLCR15 R/W			/////6	
001А80н to 001А87н	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXB	

(Continued)



10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

	El ² OS	Interru	pt vector	Interrupt control register	
Interrupt source	clear	Number	Address	Number	Address
Reset	N/A	# 08	FFFFDCH		
INT9 instruction	N/A	# 09	FFFFD8H		
Exception	N/A	# 10	FFFFD4H		
CAN RX	N/A	# 11	FFFFD0H	10000	0000000
CAN TX/NS	N/A	# 12	FFFFCC _H	ICR00	0000В0н
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8 _H	10001	0000001
Time Base Timer	N/A	# 14	FFFFC4 _H	ICR01	0000B1н
16-bit Reload Timer 0	*1	# 15	FFFFC0H	ICR02	0000000
8/10-bit A/D Converter	*1	# 16	FFFFBC H	ICR02	0000В2н
16-bit Free-run Timer	N/A	# 17	FFFFB8 _H	10000	0000000
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4H	ICR03	0000ВЗн
Serial I/O	*1	# 19	FFFFB0H	ICR04	0000B4⊦
External Interrupt (INT4/INT5)	*1	# 20	FFFFAC H	ICK04	0000B4H
Input Capture 0	*1	# 21	FFFFA8H	ICR05	0000B5н
8/16-bit PPG 0/1	N/A	# 22	FFFFA4H	ICR05	0000638
Output Compare 0	*1	# 23	FFFFA0H	ICR06	0000 В6 н
8/16-bit PPG 2/3	N/A	# 24	FFFF9CH	ICRUO	0000804
External Interrupt (INT6/INT7)	*1	# 25	FFFF98н	ICR07	0000 B7 н
Input Capture 1	*1	# 26	FFFF94н		0000071
8/16-bit PPG 4/5	N/A	# 27	FFFF90н	ICR08	0000B8н
Output Compare 1	*1	# 28	FFFF8CH	101000	0000B0H
8/16-bit PPG 6/7	N/A	# 29	FFFF88 _H	ICR09	0000 В 9н
Input Capture 2	*1	# 30	FFFF84 _H	101(09	0000898
8/16-bit PPG 8/9	N/A	# 31	FFFF80н	ICR10	0000ВАн
Output Compare 2	*1	# 32	FFFF7C _H		UUUUDAH
Input Capture 3	*1	# 33	FFFF78⊦	ICR11	0000BBн
8/16-bit PPG A/B	N/A	# 34	FFFF74 _H	юкт	0000BBA
Output Compare 3	*1	# 35	FFFF70н	ICR12	0000BCH
16-bit Reload Timer 1	*1	# 36	FFFF6C _H	101(12	0000000
UART 0 RX	*2	# 37	FFFF68н	ICR13	0000BDн
UART 0 TX	*1	# 38	FFFF64⊦		
UART 1 RX	*2	# 39	FFFF60н	ICR14	0000BEн
UART 1 TX	*1	# 40	FFFF5C _H		
Flash Memory	N/A	# 41	FFFF58⊦	ICR15	0000BFн
Delayed interrupt	N/A	# 42	FFFF54н		UUUUDI'H

*1: The interrupt request flag is cleared by the El²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the El²OS interrupt clear signal. A stop request is available.

N/A:The interrupt request flag is not cleared by the EI2OS interrupt clear signal.



- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :



Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.





Parameter	ameter Symbol Pin name Condition		Condition	Value			Unit	Remarks
Farameter	Symbol	Fill fidilite	Condition	Min	Тур	Max	Unit	Reillarks
Input leak current	hı.		Vcc = 5.5 V, Vss < Vi < Vcc	-5	_	5	μA	
	lcc		Vcc = 5.0 V±10%, Internal frequency:	—	35	60	mA	MB90598G
	icc		16 MHz, At normal operating	—	40	60	mA	MB90F598G
Power supply current *	lccs		Vcc = 5.0 V±10%, Internal frequency: 16 MHz, At sleep	_	11	18	mA	
	Істѕ	Vcc	V _{CC} = 5.0 V±1%, Internal frequency: 2 MHz, At timer mode	_	0.3	0.6	mA	
	Іссн		Vcc = 5.0 V±10%, At stop, T _A = 25°C	_	—	20	μA	
	Іссн2		Vcc = 5.0 V±10%, At Hardware stand-	_	_	20	μA	MB90598G
	ICCH2		by mode, T _A = 25°C		50	100	μΑ	MB90F598G (Conti

(Continued)



Example of Oscillation circuit





11.4.2 Reset and Hardware Standby Input

			$(Vcc = 5.0 V \pm$	10%, Vss	= AVss	$= 0.0 \text{ V}, \text{ T}_{\text{A}} = -40 ^{\circ}\text{C} \text{ to } +85$
Parameter	Symbol	Pin name	Value		Unit	Remarks
Falametei	Min Max	Unit	Rellidi KS			
			16 tcp*1	—	ns	Under normal operation
Reset input time	t rstl	RST	Oscillation time of oscillator ^{*2} + 16 t_{CP} ^{*1}	—	ms	In stop mode
			16 tcp*1	—	ns	Under normal operation
Hardware standby input time	tнsт∟	HST	Oscillation time of oscillator ^{*2} + 16 t_{CP}^{*1}	—	ms	In stop mode

*1: "tcp" represents one cycle time of the machine clock.

No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.





12. Example Characteristics











Supply Current





13. Ordering Information

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

14. Package Dimensions







15. Major Changes

Spansion Publication Number: DS07-13705-7E

Section	Change Results
-	Deleted the old products, MB90598, MB90F598, and MB90V595.
-	Changed the series name; MB90595/595G series ? MB90595G series
-	Changed the following erroneous name. I/O timer \rightarrow 16-bit Free-run Timer
PRODUCT LINEUP	One of Standby mode name is changed. Clock mode \rightarrow Watch mode
I/O CIRCUIT TYPE	Changed Pull-down resistor value of circuit type H.
ELECTRICAL CHARACTERISTICS AC Characteristics	Add the "External clock input" and "Flash Read cycle time" in (1) Clock Timing
	Figure in (2) Reset and Hardware Standby Input RST/HST input level of "In Stop Mode" is changed. 0.6 Vcc 0.2 Vcc
ELECTRICAL CHARACTERISTICS 5. A/D Converter	Changed the items of "Zero transition voltage" and "Full scale transition voltage".

NOTE: Please see "Document History" about later revised information.

Document History

Document Title: MB90598G/F598G/V595G F²MC-16LX MB90595G Series CMOS 16-bit Proprietary Microcontroller Document Number: 002-07700 Orig. of Change Submission Revision ECN **Description of Change** Date ** _ AKIH 09/26/2008 Migrated to Cypress and assigned document number 002-07700. No change to document contents or format. *A 5537128 AKIH 11/30/2016 Updated to Cypress template



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