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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

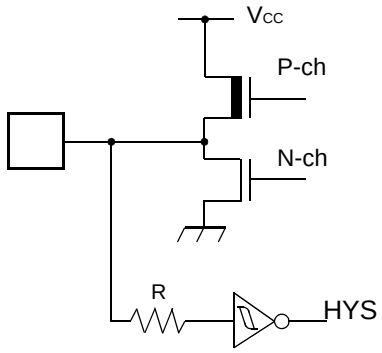
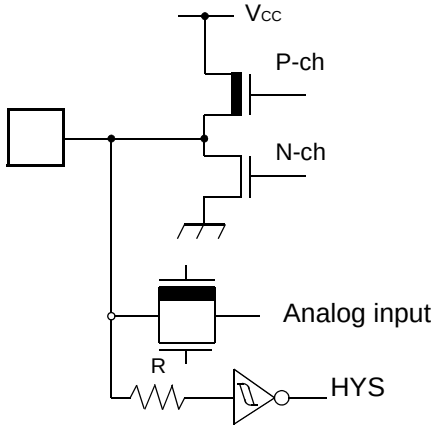
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | CANbus, EBI/EMI, SCI, Serial I/O, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 78 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-142-bnd |

## 3. Pin Description

| Pin no. | Pin name | Circuit type | Function |
|---|---|---|---|
| 82 | X0 | A | Oscillator pin |
| 83 | X1 | | |
| 77 | $\overline{\text{RST}}$ | B | Reset input |
| 52 | $\overline{\text{HST}}$ | C | Hardware standby input |
| 85 to 88 | P00 to P03 | G | General purpose IO |
| | IN0 to IN3 | | Inputs for the Input Captures |
| 89 to 92 | P04 to P07 | G | General purpose IO |
| | OUT0 to OUT3 | | Outputs for the Output Compares. |
| 93 to 98 | P10 to P15 | D | General purpose IO |
| | PPG0 to PPG5 | | Outputs for the Programmable Pulse Generators |
| 99 | P16 | D | General purpose IO |
| | TIN1 | | TIN input for the 16-bit Reload Timer 1 |
| 100 | P17 | D | General purpose IO |
| | TOT1 | | TOT output for the 16-bit Reload Timer 1 |
| 1 to 8 | P20 to P27 | G | General purpose IO |
| 9 to 10 | P30 to P31 | G | General purpose IO |
| 12 to 16 | P32 to P36 | G | General purpose IO |
| 17 | P37 | D | General purpose IO |
| 18 | P40 | G | General purpose IO |
| | SOT0 | | SOT output for UART 0 |
| 19 | P41 | G | General purpose IO |
| | SCK0 | | SCK input/output for UART 0 |
| 20 | P42 | G | General purpose IO |
| | SIN0 | | SIN input for UART 0 |
| 21 | P43 | G | General purpose IO |
| | SIN1 | | SIN input for UART 1 |
| 22 | P44 | G | General purpose IO |
| | SCK1 | | SCK input/output for UART 1 |
| 24 | P45 | G | General purpose IO |
| | SOT1 | | SOT output for UART 1 |
| 25 | P46 | G | General purpose IO |
| | SOT2 | | SOT output for the Serial IO |
| 26 | P47 | G | General purpose IO |
| | SCK2 | | SCK input/output for the Serial IO |

| Pin no. | Pin name | Circuit type | Function |
|---|---|---|---|
| 28 | P50 | D | General purpose IO |
| | SIN2 | | SIN Input for the Serial IO |
| 29 to 32 | P51 to P54 | D | General purpose IO |
| | INT4 to INT7 | | External interrupt input for INT4 to INT7 |
| 33 | P55 | D | General purpose IO |
| | ADTG | | Input for the external trigger of the A/D Converter |
| 38 to 41 | P60 to P63 | E | General purpose IO |
| | AN0 to AN3 | | Inputs for the A/D Converter |
| 43 to 46 | P64 to P67 | E | General purpose IO |
| | AN4 to AN7 | | Inputs for the A/D Converter |
| 47 | P56 | D | General purpose IO |
| | TIN0 | | TIN input for the 16-bit Reload Timer 0 |
| 48 | P57 | D | General purpose IO |
| | TOT0 | | TOT output for the 16-bit Reload Timer 0 |
| 54 to 57 | P70 to P73 | F | General purpose IO |
| | PWM1P0<br>PWM1M0<br>PWM2P0<br>PWM2M0 | | Output for Stepper Motor Controller channel 0 |
| 59 to 62 | P74 to P77 | F | General purpose IO |
| | PWM1P1<br>PWM1M1<br>PWM2P1<br>PWM2M1 | | Output for Stepper Motor Controller channel 1 |
| 64 to 67 | P80 to P83 | F | General purpose IO |
| | PWM1P2<br>PWM1M2<br>PWM2P2<br>PWM2M2 | | Output for Stepper Motor Controller channel 2 |
| 69 to 72 | P84 to P87 | F | General purpose IO |
| | PWM1P3<br>PWM1M3<br>PWM2P3<br>PWM2M3 | | Output for Stepper Motor Controller channel 3 |
| 74 | P90 | D | General purpose IO |
| | TX | | TX output for CAN Interface |
| 75 | P91 | D | General purpose IO |
| | RX | | RX input for CAN Interface |

| Circuit Type | Circuit | Remarks |
|---|---|---|
| D |  | ■ CMOS output<br>■ CMOS Hysteresis input |
| E |  | ■ CMOS output<br>■ CMOS Hysteresis input<br>■ Analog input |

*(Continued)*

## 5. Handling Devices

**(1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).**

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding $V_{CC}$ or an voltage below $V_{SS}$ is applied to input or output pins or a voltage exceeding the rating is applied across $V_{CC}$ and $V_{SS}$.

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage ($AV_{CC}$, AVRH, $DV_{CC}$) and analog input voltages not exceed the digital voltage ($V_{CC}$).

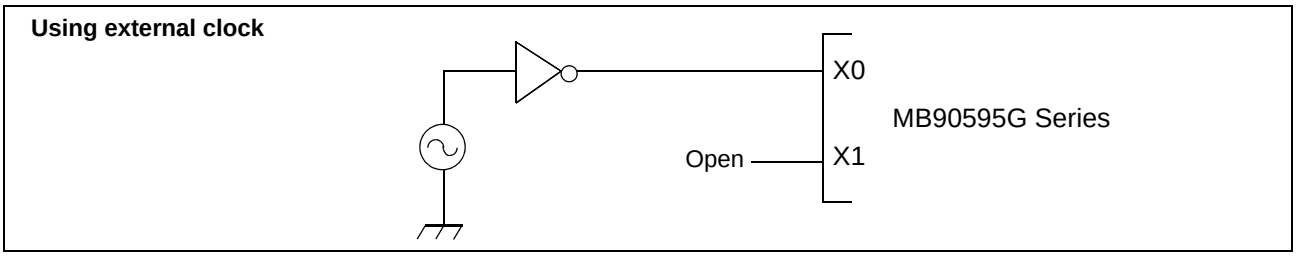
**(2) Treatment of Unused Pins**

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

**(3) Using external clock**

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

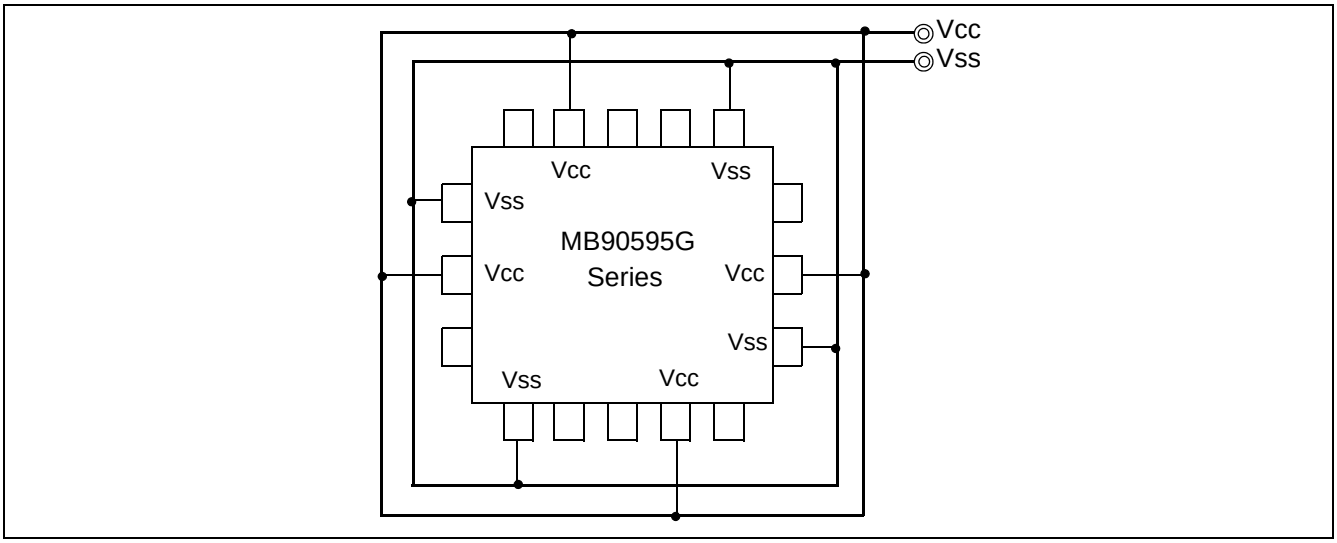



**(4) Power supply pins (Vcc/Vss)**

In products with multiple $V_{cc}$ or $V_{ss}$ pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)

Make sure to connect $V_{cc}$ and $V_{ss}$ pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between $V_{cc}$ and $V_{ss}$ pins near the device.



**(5) Pull-up/down resistors**
The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

**(6) Crystal Oscillator Circuit**
Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.
A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

**(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs**
Make sure to turn on the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply ($V_{CC}$).
Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable).

**(8) Connection of Unused Pins of A/D Converter**
Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = DV_{CC} = V_{SS}$.

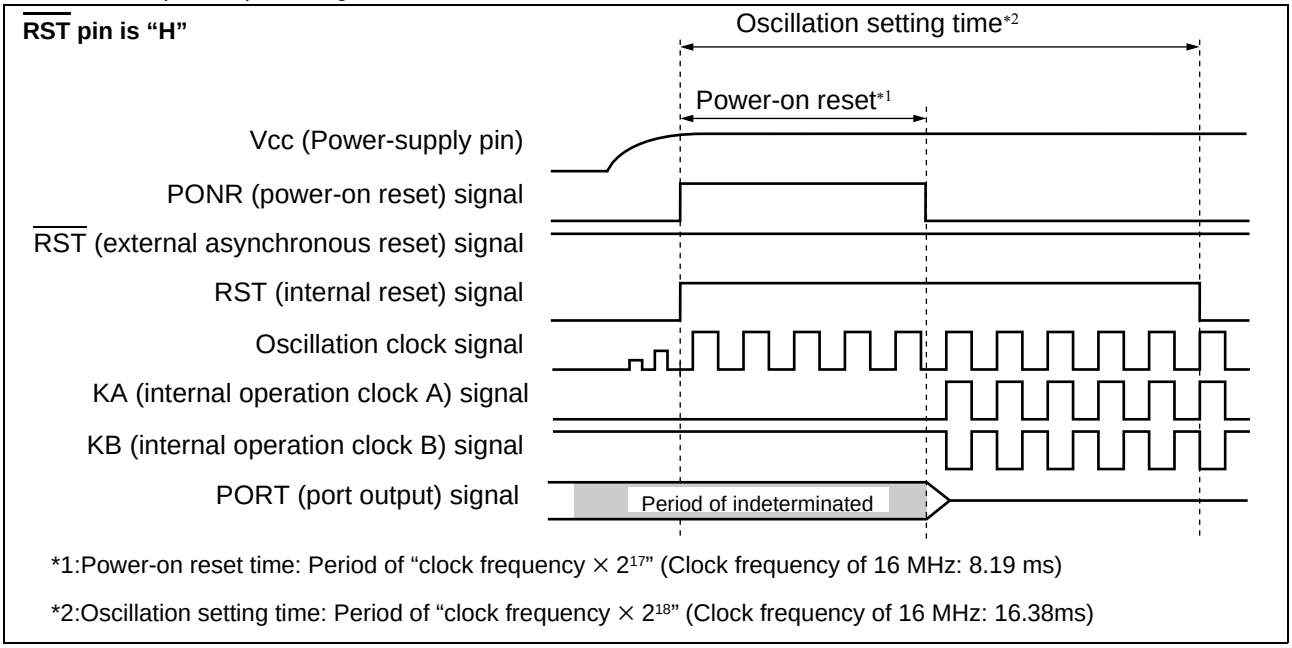
**(9) N.C. Pin**
The N.C. (internally connected) pin must be opened for use.

**(10) Notes on Energization**
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

**(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)**
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

■ If $\overline{RST}$ pin is “H”, the outputs become indeterminate.

■ If $\overline{RST}$ pin is “L”, the outputs become high-impedance.
Pay attention to the port output timing shown as follows.




*1:Power-on reset time: Period of “clock frequency × $2^{17}$” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × $2^{18}$” (Clock frequency of 16 MHz: 16.38ms)

## 8. I/O Map

| Address | Register | Abbreviation | Access | Peripheral | Initial value |
|---|---|---|---|---|---|
| $00_H$ | Port 0 Data Register | PDR0 | R/W | Port 0 | $XXXXXXXX_B$ |
| $01_H$ | Port 1 Data Register | PDR1 | R/W | Port 1 | $XXXXXXXX_B$ |
| $02_H$ | Port 2 Data Register | PDR2 | R/W | Port 2 | $XXXXXXXX_B$ |
| $03_H$ | Port 3 Data Register | PDR3 | R/W | Port 3 | $XXXXXXXX_B$ |
| $04_H$ | Port 4 Data Register | PDR4 | R/W | Port 4 | $XXXXXXXX_B$ |
| $05_H$ | Port 5 Data Register | PDR5 | R/W | Port 5 | $XXXXXXXX_B$ |
| $06_H$ | Port 6 Data Register | PDR6 | R/W | Port 6 | $XXXXXXXX_B$ |
| $07_H$ | Port 7 Data Register | PDR7 | R/W | Port 7 | $XXXXXXXX_B$ |
| $08_H$ | Port 8 Data Register | PDR8 | R/W | Port 8 | $XXXXXXXX_B$ |
| $09_H$ | Port 9 Data Register | PDR9 | R/W | Port 9 | $\_\_XXXXXX_B$ |
| $0A_H$ to $0F_H$ | Reserved | | | | |
| $10_H$ | Port 0 Direction Register | DDR0 | R/W | Port 0 | $00000000_B$ |
| $11_H$ | Port 1 Direction Register | DDR1 | R/W | Port 1 | $00000000_B$ |
| $12_H$ | Port 2 Direction Register | DDR2 | R/W | Port 2 | $00000000_B$ |
| $13_H$ | Port 3 Direction Register | DDR3 | R/W | Port 3 | $00000000_B$ |
| $14_H$ | Port 4 Direction Register | DDR4 | R/W | Port 4 | $00000000_B$ |
| $15_H$ | Port 5 Direction Register | DDR5 | R/W | Port 5 | $00000000_B$ |
| $16_H$ | Port 6 Direction Register | DDR6 | R/W | Port 6 | $00000000_B$ |
| $17_H$ | Port 7 Direction Register | DDR7 | R/W | Port 7 | $00000000_B$ |
| $18_H$ | Port 8 Direction Register | DDR8 | R/W | Port 8 | $00000000_B$ |
| $19_H$ | Port 9 Direction Register | DDR9 | R/W | Port 9 | $\_\_000000_B$ |
| $1A_H$ | Reserved | | | | |
| $1B_H$ | Analog Input Enable Register | ADER | R/W | Port 6, A/D | $11111111_B$ |
| $1C_H$ to $1F_H$ | Reserved | | | | |
| $20_H$ | Serial Mode Control Register 0 | UMC0 | R/W | UART0 | $00000100_B$ |
| $21_H$ | Serial status Register 0 | USR0 | R/W | | $00010000_B$ |
| $22_H$ | Serial Input/Output Data Register 0 | UIDR0/UODR0 | R/W | | $XXXXXXXX_B$ |
| $23_H$ | Rate and Data Register 0 | URD0 | R/W | | $0000000X_B$ |
| $24_H$ | Serial Mode Register 1 | SMR1 | R/W | UART1 | $00000000_B$ |
| $25_H$ | Serial Control Register 1 | SCR1 | R/W | | $00000100_B$ |
| $26_H$ | Serial Input/Output Data Register 1 | SIDR1/SODR1 | R/W | | $XXXXXXXX_B$ |
| $27_H$ | Serial Status Register 1 | SSR1 | R/W | | $0001\_00_B$ |
| $28_H$ | UART1 Prescaler Control Register | U1CDCR | R/W | | $0\_\_\_1111_B$ |

*(Continued)*

| Address | Register | Abbreviation | Access | Peripheral | Initial value |
|---|---|---|---|---|---|
| 4C$_H$ | PPGA Operation Mode Control Register | PPGCA | R/W | 16-bit Programmable Pulse Generator A/B | 0 _ 0 0 0 _ _ 1$_B$ |
| 4D$_H$ | PPGB Operation Mode Control Register | PPGCB | R/W | | 0 _ 0 0 0 0 0 1$_B$ |
| 4E$_H$ | PPGA, B Output Pin Control Register | PPGAB | R/W | | 0 0 0 0 0 0 _ _$_B$ |
| 4F$_H$ | Reserved | | | | |
| 50$_H$ | Timer Control Status Register 0 | TMCSR0 | R/W | 16-bit Reload Timer 0 | 0 0 0 0 0 0 0 0$_B$ |
| 51$_H$ | Timer Control Status Register 0 | TMCSR0 | R/W | | _ _ _ _ 0 0 0 0$_B$ |
| 52$_H$ | Timer 0/Reload Register 0 | TMR0/TMRLR0 | R/W | | XXXXXXXX$_B$ |
| 53$_H$ | Timer 0/Reload Register 0 | TMR0/TMRLR0 | R/W | | XXXXXXXX$_B$ |
| 54$_H$ | Timer Control Status Register 1 | TMCSR1 | R/W | 16-bit Reload Timer 1 | 0 0 0 0 0 0 0 0$_B$ |
| 55$_H$ | Timer Control Status Register 1 | TMCSR1 | R/W | | _ _ _ _ 0 0 0 0$_B$ |
| 56$_H$ | Timer Register 1/Reload Register 1 | TMR1/TMRLR1 | R/W | | XXXXXXXX$_B$ |
| 57$_H$ | Timer Register 1/Reload Register 1 | TMR1/TMRLR1 | R/W | | XXXXXXXX$_B$ |
| 58$_H$ | Output Compare Control Status Register 0 | OCS0 | R/W | Output Compare 0/1 | 0 0 0 0 _ _ 0 0$_B$ |
| 59$_H$ | Output Compare Control Status Register 1 | OCS1 | R/W | | _ _ _ 0 0 0 0 0$_B$ |
| 5A$_H$ | Output Compare Control Status Register 2 | OCS2 | R/W | Output Compare 2/3 | 0 0 0 0 _ _ 0 0$_B$ |
| 5B$_H$ | Output Compare Control Status Register 3 | OCS3 | R/W | | _ _ _ 0 0 0 0 0$_B$ |
| 5C$_H$ | Input Capture Control Status Register 0/1 | ICS01 | R/W | Input Capture 0/1 | 0 0 0 0 0 0 0 0$_B$ |
| 5D$_H$ | Input Capture Control Status Register 2/3 | ICS23 | R/W | Input Capture 2/3 | 0 0 0 0 0 0 0 0$_B$ |
| 5E$_H$ | PWM Control Register 0 | PWC0 | R/W | Stepping Motor Controller 0 | 0 0 0 0 0 _ _ 0$_B$ |
| 5F$_H$ | Reserved | | | | |
| 60$_H$ | PWM Control Register 1 | PWC1 | R/W | Stepping Motor Controller 1 | 0 0 0 0 0 _ _ 0$_B$ |
| 61$_H$ | Reserved | | | | |
| 62$_H$ | PWM Control Register 2 | PWC2 | R/W | Stepping Motor Controller 2 | 0 0 0 0 0 _ _ 0$_B$ |
| 63$_H$ | Reserved | | | | |
| 64$_H$ | PWM Control Register 3 | PWC3 | R/W | Stepping Motor Controller 3 | 0 0 0 0 0 _ _ 0$_B$ |
| 65$_H$ | Reserved | | | | |
| 66$_H$ | Timer Data Register (low-order) | TCDT | R/W | 16-bit Free-run Timer | 0 0 0 0 0 0 0 0$_B$ |
| 67$_H$ | Timer Data Register (high-order) | TCDT | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 68$_H$ | Timer Control Status Register | TCCS | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 69$_H$ to 6E$_H$ | Reserved | | | | |

*(Continued)*

| Address | Register | Abbreviation | Access | Peripheral | Initial value |
|---|---|---|---|---|---|
| 6F$_H$ | ROM Mirror Function Selection Register | ROMM | R/W | ROM Mirror | _ _ _ _ _ _ _ 1$_B$ |
| 70$_H$ | PWM1 Compare Register 0 | PWC10 | R/W | Stepping Motor Controller 0 | XXXXXXXX$_B$ |
| 71$_H$ | PWM2 Compare Register 0 | PWC20 | R/W | | XXXXXXXX$_B$ |
| 72$_H$ | PWM1 Select Register 0 | PWS10 | R/W | | _ _ 0 0 0 0 0 0$_B$ |
| 73$_H$ | PWM2 Select Register 0 | PWS20 | R/W | | _ 0 0 0 0 0 0 0$_B$ |
| 74$_H$ | PWM1 Compare Register 1 | PWC11 | R/W | Stepping Motor Controller 1 | XXXXXXXX$_B$ |
| 75$_H$ | PWM2 Compare Register 1 | PWC21 | R/W | | XXXXXXXX$_B$ |
| 76$_H$ | PWM1 Select Register 1 | PWS11 | R/W | | _ _ 0 0 0 0 0 0$_B$ |
| 77$_H$ | PWM2 Select Register 1 | PWS21 | R/W | | _ 0 0 0 0 0 0 0$_B$ |
| 78$_H$ | PWM1 Compare Register 2 | PWC12 | R/W | Stepping Motor Controller 2 | XXXXXXXX$_B$ |
| 79$_H$ | PWM2 Compare Register 2 | PWC22 | R/W | | XXXXXXXX$_B$ |
| 7A$_H$ | PWM1 Select Register 2 | PWS12 | R/W | | _ _ 0 0 0 0 0 0$_B$ |
| 7B$_H$ | PWM2 Select Register 2 | PWS22 | R/W | | _ 0 0 0 0 0 0 0$_B$ |
| 7C$_H$ | PWM1 Compare Register 3 | PWC13 | R/W | Stepping Motor Controller 3 | XXXXXXXX$_B$ |
| 7D$_H$ | PWM2 Compare Register 3 | PWC23 | R/W | | XXXXXXXX$_B$ |
| 7E$_H$ | PWM1 Select Register 3 | PWS13 | R/W | | _ _ 0 0 0 0 0 0$_B$ |
| 7F$_H$ | PWM2 Select Register 3 | PWS23 | R/W | | _ 0 0 0 0 0 0 0$_B$ |
| 80$_H$ to 8F$_H$ | CAN Controller. Refer to section about CAN Controller | | | | |
| 90$_H$ to 9D$_H$ | Reserved | | | | |
| 9E$_H$ | Program Address Detection Control Status Register | PACSR | R/W | Address Match Detection Function | 0 0 0 0 0 0 0 0$_B$ |
| 9F$_H$ | Delayed Interrupt/Request Register | DIRR | R/W | Delayed Interrupt | _ _ _ _ _ _ _ 0$_B$ |
| A0$_H$ | Low-Power Mode Control Register | LPMCR | R/W | Low Power Controller | 0 0 0 1 1 0 0 0$_B$ |
| A1$_H$ | Clock Selection Register | CKSCR | R/W | Low Power Controller | 1 1 1 1 1 1 0 0$_B$ |
| A2$_H$ to A7$_H$ | Reserved | | | | |
| A8$_H$ | Watchdog Timer Control Register | WDTC | R/W | Watchdog Timer | XXXXX 1 1 1$_B$ |
| A9$_H$ | Time Base Timer Control Register | TBTC | R/W | Time Base Timer | 1 _ _ 0 0 1 0 0$_B$ |
| AA$_H$ to AD$_H$ | Reserved | | | | |
| AE$_H$ | Flash Memory Control Status Register (MB90F598G only. Otherwise reserved) | FMCS | R/W | Flash Memory | 0 0 0 X 0 0 0 0$_B$ |
| AF$_H$ | Reserved | | | | |

*(Continued)*

### 9.3 List of Message Buffers (DLC Registers and Data Registers)

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 001A60H | DLC register 0 | DLCR0 | R/W | ----XXXXB |
| 001A61H | | | | |
| 001A62H | DLC register 1 | DLCR1 | R/W | ----XXXXB |
| 001A63H | | | | |
| 001A64H | DLC register 2 | DLCR2 | R/W | ----XXXXB |
| 001A65H | | | | |
| 001A66H | DLC register 3 | DLCR3 | R/W | ----XXXXB |
| 001A67H | | | | |
| 001A68H | DLC register 4 | DLCR4 | R/W | ----XXXXB |
| 001A69H | | | | |
| 001A6AH | DLC register 5 | DLCR5 | R/W | ----XXXXB |
| 001A6BH | | | | |
| 001A6CH | DLC register 6 | DLCR6 | R/W | ----XXXXB |
| 001A6DH | | | | |
| 001A6EH | DLC register 7 | DLCR7 | R/W | ----XXXXB |
| 001A6FH | | | | |
| 001A70H | DLC register 8 | DLCR8 | R/W | ----XXXX |
| 001A71H | | | | |
| 001A72H | DLC register 9 | DLCR9 | R/W | ----XXXXB |
| 001A73H | | | | |
| 001A74H | DLC register 10 | DLCR10 | R/W | ----XXXXB |
| 001A75H | | | | |
| 001A76H | DLC register 11 | DLCR11 | R/W | ----XXXXB |
| 001A77H | | | | |
| 001A78H | DLC register 12 | DLCR12 | R/W | ----XXXXB |
| 001A79H | | | | |
| 001A7AH | DLC register 13 | DLCR13 | R/W | ----XXXXB |
| 001A7BH | | | | |
| 001A7CH | DLC register 14 | DLCR14 | R/W | ----XXXXB |
| 001A7DH | | | | |
| 001A7EH | DLC register 15 | DLCR15 | R/W | ----XXXXB |
| 001A7FH | | | | |
| 001A80H to 001A87H | Data register 0 (8 bytes) | DTR0 | R/W | XXXXXXXXB to XXXXXXXXB |

*(Continued)*

*(Continued)*

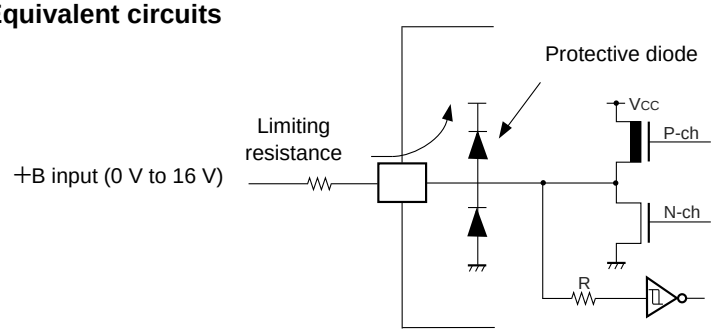
| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 001A88H to 001A8FH | Data register 1 (8 bytes) | DTR1 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001A90H to 001A97H | Data register 2 (8 bytes) | DTR2 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001A98H to 001A9FH | Data register 3 (8 bytes) | DTR3 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AA0H to 001AA7H | Data register 4 (8 bytes) | DTR4 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AA8H to 001AAFH | Data register 5 (8 bytes) | DTR5 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AB0H to 001AB7H | Data register 6 (8 bytes) | DTR6 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AB8H to 001ABFH | Data register 7 (8 bytes) | DTR7 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AC0H to 001AC7H | Data register 8 (8 bytes) | DTR8 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AC8H to 001ACFH | Data register 9 (8 bytes) | DTR9 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AD0H to 001AD7H | Data register 10 (8 bytes) | DTR10 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AD8H to 001ADFH | Data register 11 (8 bytes) | DTR11 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AE0H to 001AE7H | Data register 12 (8 bytes) | DTR12 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AE8H to 001AEFH | Data register 13 (8 bytes) | DTR13 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AF0H to 001AF7H | Data register 14 (8 bytes) | DTR14 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AF8H to 001AFFH | Data register 15 (8 bytes) | DTR15 | R/W | XXXXXXXXB to XXXXXXXXB |

Notes:

- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the $V_{CC}$ pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

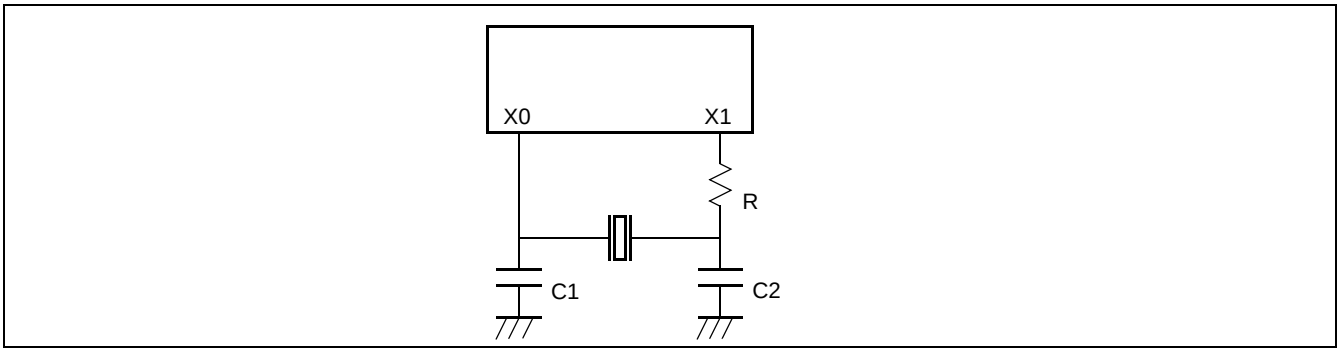
**• Input/Output Equivalent circuits**



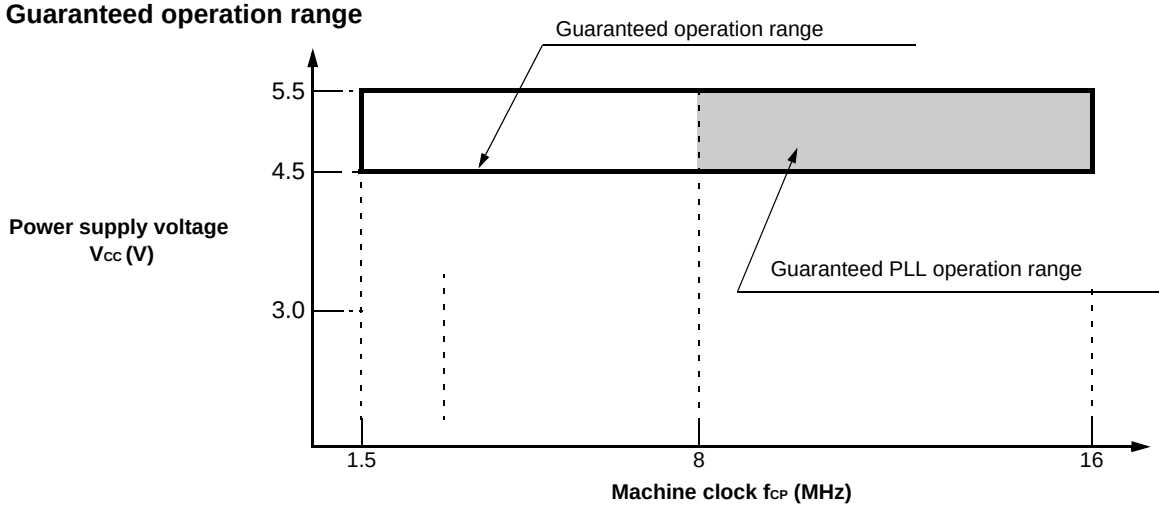

Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

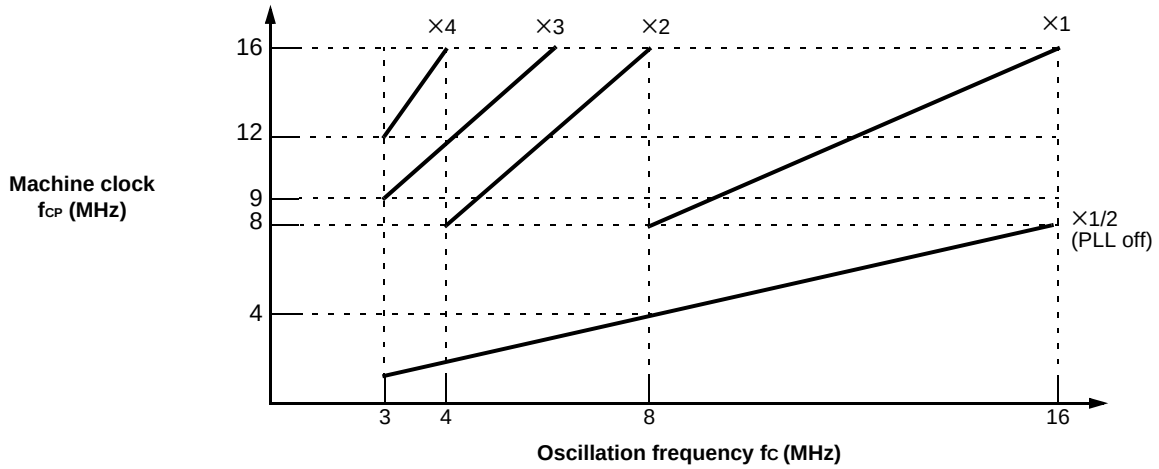
■ Example of Oscillation circuit



- **Guaranteed operation range**



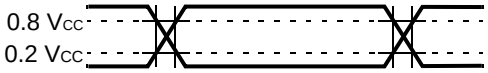

- **Oscillation frequency and machine clock frequency**




AC characteristics are set to the measured reference voltage values below.

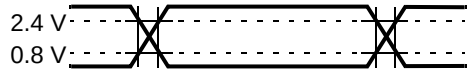
- **Input signal waveform**

**Hysteresis Input Pin**




- **Output signal waveform**

**Output Pin**



*11.4.2 Reset and Hardware Standby Input*

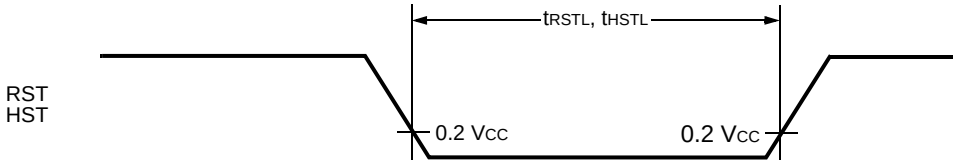
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +85 °C)

| Parameter | Symbol | Pin name | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|
| | | | Min | Max | | |
| Reset input time | $t_{RSTL}$ | $\overline{RST}$ | 16 $t_{CP}$*1 | — | ns | Under normal operation |
| | | | Oscillation time of oscillator*2 + 16 $t_{CP}$*1 | — | ms | In stop mode |
| Hardware standby input time | $t_{HSTL}$ | $\overline{HST}$ | 16 $t_{CP}$*1 | — | ns | Under normal operation |
| | | | Oscillation time of oscillator*2 + 16 $t_{CP}$*1 | — | ms | In stop mode |

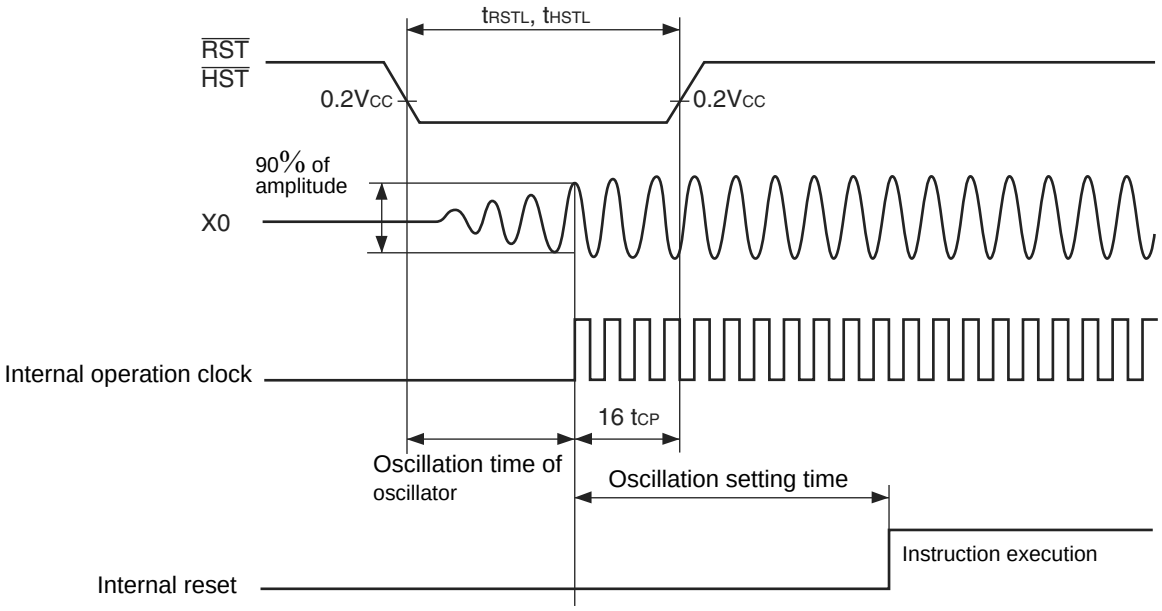
*1: "$t_{cp}$" represents one cycle time of the machine clock.
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

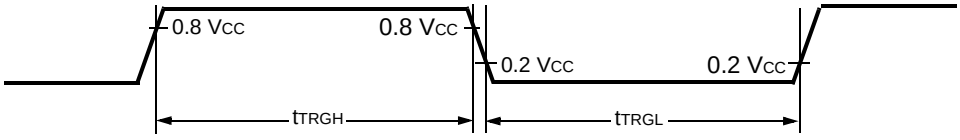
**Under Normal Operation**




**In Stop Mode**



- **Trigger Input Timing**




*11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)*

($V_{CC}$ = 5.0 V±10 %, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Output Rise/Fall time | $t_{R2}$<br>$t_{F2}$ | Port P70 to P77,<br>Port P80 to P87 | — | 15 | 40 | 150 | ns | |

- Slew Rate Output Timing


$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

## 11.5 A/D Converter

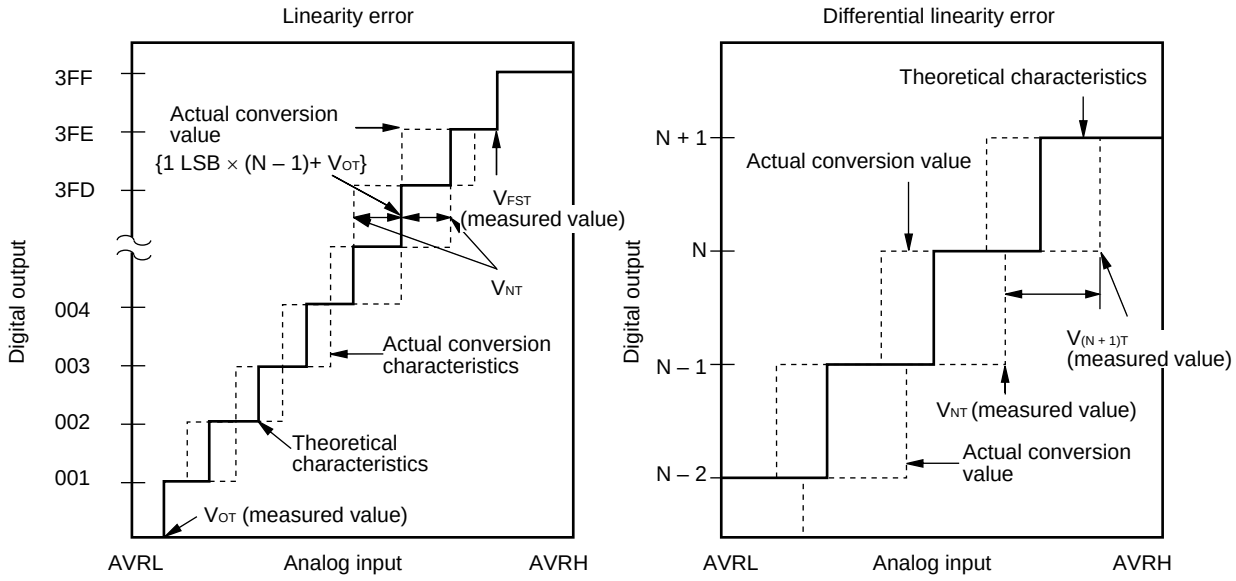
($V_{CC}$ = $AV_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V,3.0 V ≤ AVRH − AVRL, $T_A$ = −40 °C to +85 °C)

| Parameter | Sym-bol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | | 10 | bit | |
| Conversion error | — | — | — | — | ±5.0 | LSB | |
| Nonlinearity error | — | — | — | — | ±2.5 | LSB | |
| Differential linearity error | — | — | — | — | ±1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | AVRL − 3.5 LSB | AVRL + 0.5 LSB | AVRL + 4.5 LSB | V | |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH − 6.5 LSB | AVRH − 1.5 LSB | AVRH + 1.5 LSB | V | |
| Conversion time | — | — | — | 352$t_{CP}$ | — | ns | |
| Sampling time | — | — | — | 64$t_{CP}$ | — | ns | |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | −10 | — | 10 | µA | |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN7 | AVRL | — | AVRH | V | |

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Reference voltage range | — | AVRH | AVRL + 3.0 | — | $AV_{CC}$ | V | |
| | — | AVRL | 0 | — | AVRH − 3.0 | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 5 | — | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage current | $I_R$ | AVRH | — | 400 | 600 | µA | MB90V595G, MB90F598G |
| | | | — | 140 | 600 | µA | MB90598G |
| | $I_{RH}$ | AVRH | — | — | 5 | µA | * |
| Offset between input channels | — | AN0 to AN7 | — | — | 4 | LSB | |

* : When not operating A/D converter, this is the current ($V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) when the CPU is stopped.

*(Continued)*




$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$V_{OT}$: Voltage at transition of digital output from "$000_H$" to "$001_H$"
$V_{FST}$: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

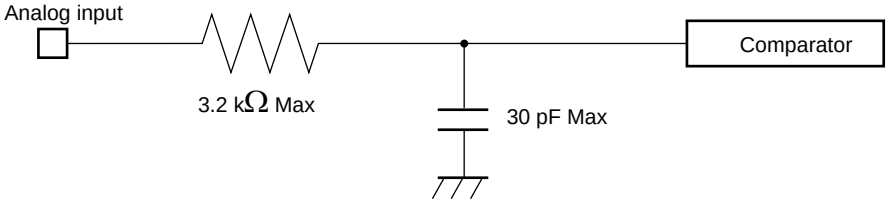
### 11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions,:

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**

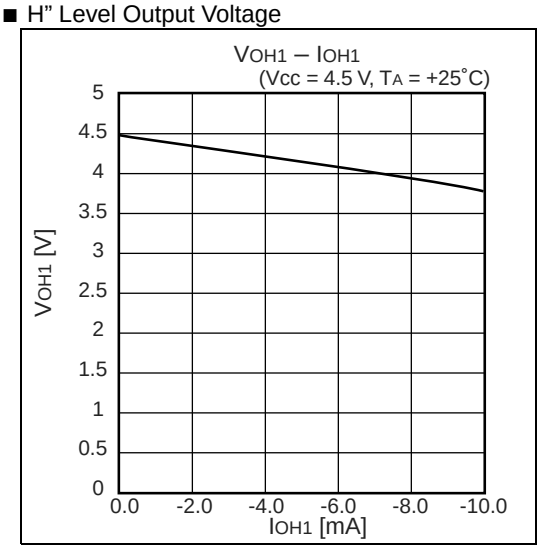


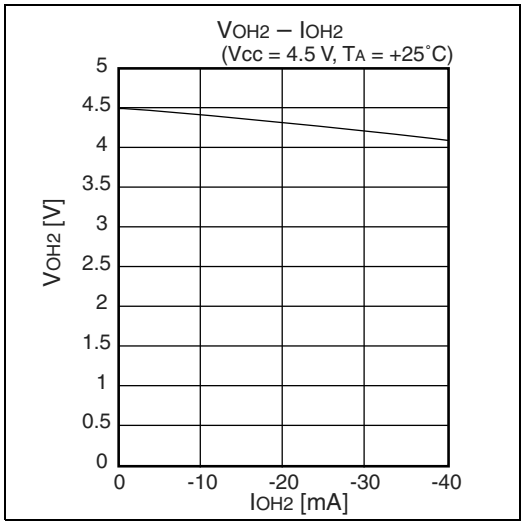

**■ Error**

The smaller the | AVRH − AVRL |, the greater the error would become relatively.

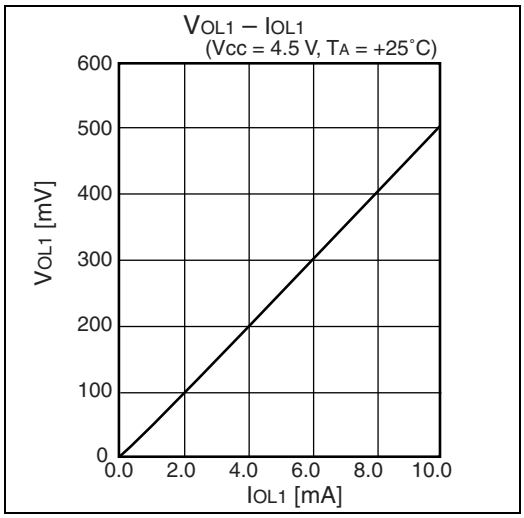
## 12. Example Characteristics

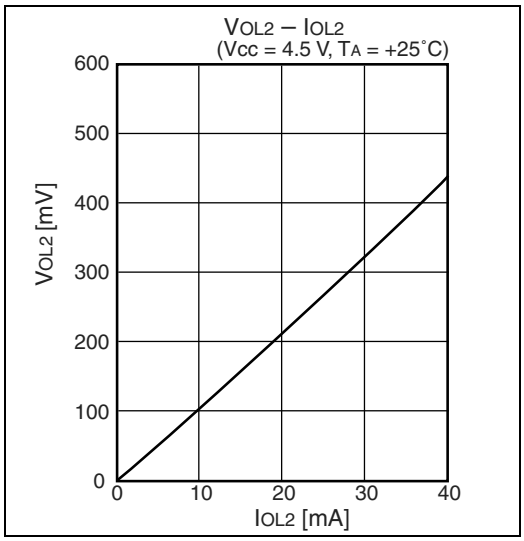
■ H" Level Output Voltage



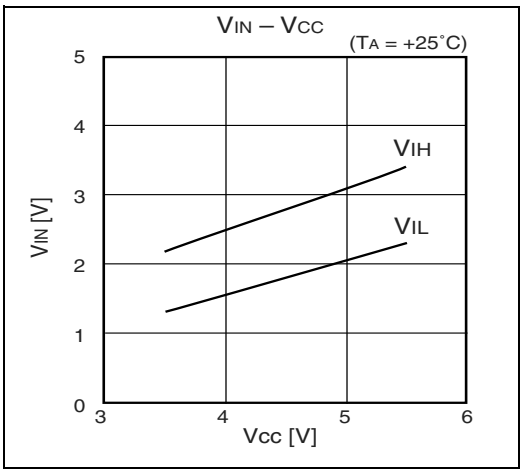




■ L" Level Input Voltage




■ H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



**Supply Current**