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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-146-bnd

1. Product Lineup

Features		MB90598G	MB90F598G	MB90V595G
Classification		Mask ROM product	Flash ROM product	Evaluation product
ROM size		128 Kbytes	128 Kbytes Boot block Hard-wired reset vector	None
RAM size		4 Kbytes	4 Kbytes	6 Kbytes
Emulator-specific power supply *1		—		None
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 μs (at machine clock frequency of 16 MHz, minimum value)		
UART0		Clock synchronized transmission (500 K/1 M/2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
UART1(SCI)		Clock synchronized transmission (62.5 K/125 K/250 K/500 K/1 Mbps) Clock asynchronized transmission (1202/2404/4808/9615/31250 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers (6 channels)		Number of channels: 6 (8/16-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 (fsys = system clock frequency) 128μs (fosc = 4MHz: oscillation clock frequency)		
16-bit Reload timer		Number of channels: 2 Operation clock frequency: fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)		

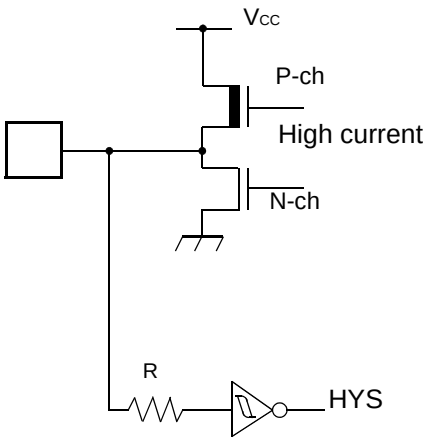
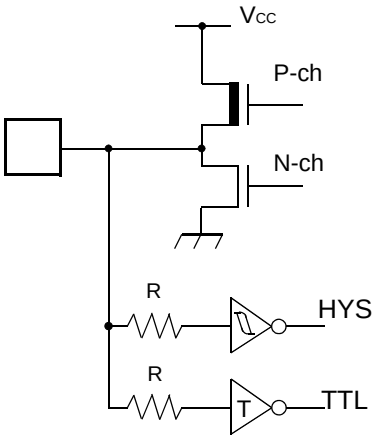
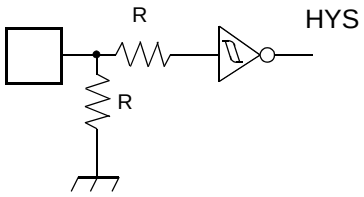
Features	MB90598G	MB90F598G	MB90V595G
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90598G/F598G:TSEG2 ≥ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics, Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*2	+5 V±10 %		
Package	QFP-100		PGA-256

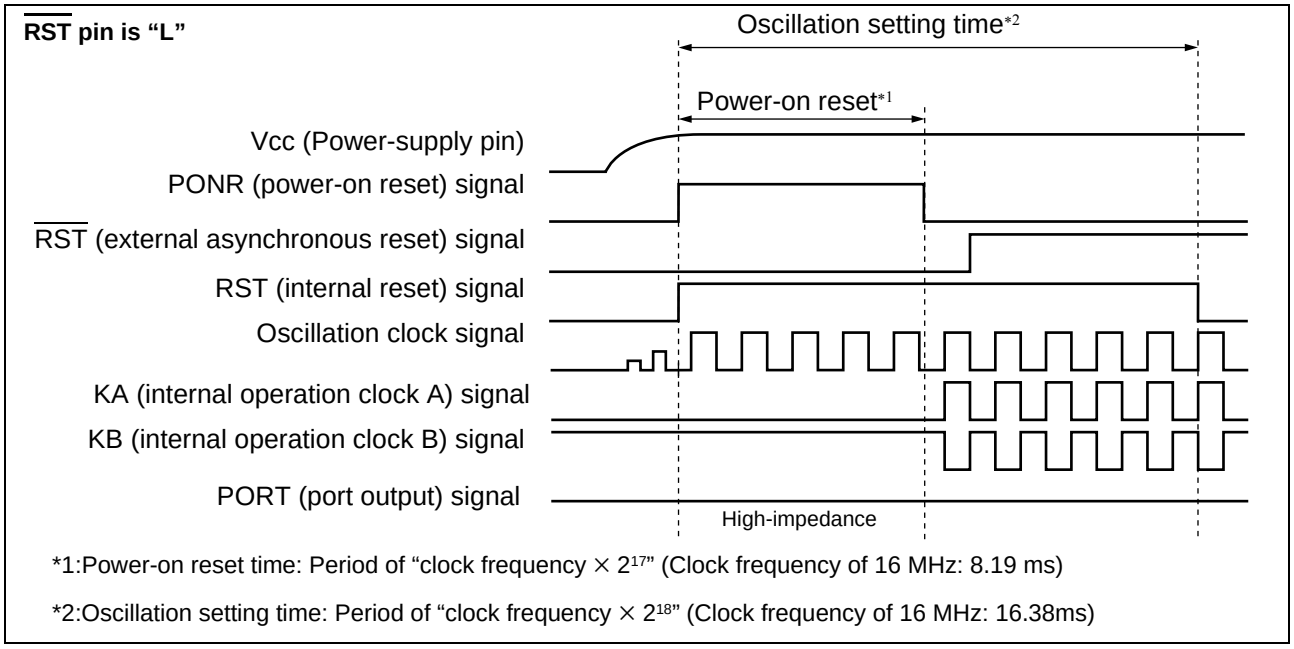
*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2: Varies with conditions such as the operating frequency. (See "Electrical Characteristics.")

3. Pin Description

Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{\text{RST}}$	B	Reset input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

Circuit Type	Circuit	Remarks
F		■ CMOS high current output ■ CMOS Hysteresis input
G		■ CMOS output ■ CMOS Hysteresis input ■ TTL input (MB90F598G, only in Flash mode)
H		■ Hysteresis input Pull-down Resistor: 50 kΩ approx. (except MB90F598G)



*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)

(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

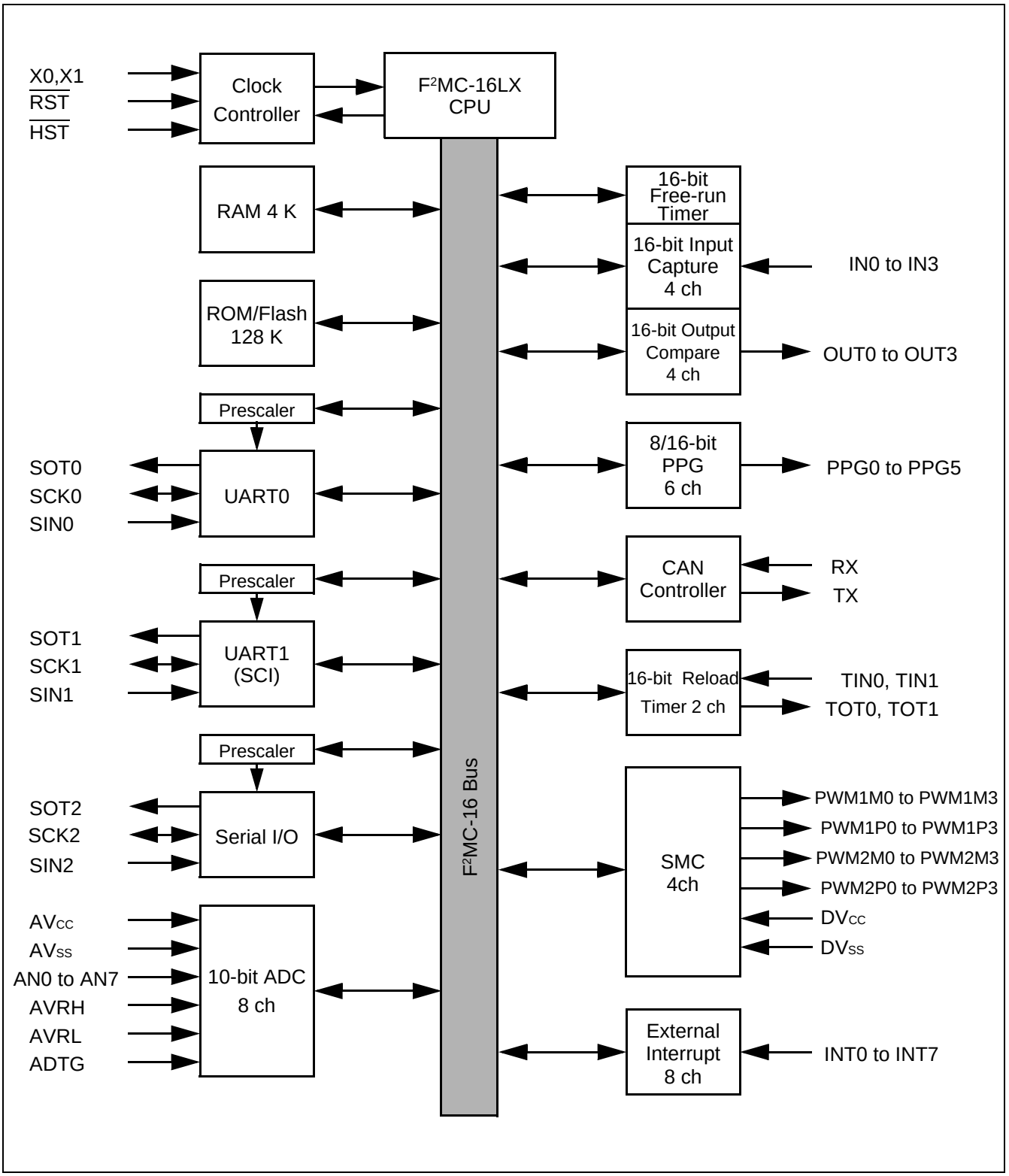
(14) Using REALOS

The use of EI^2OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

6. Block Diagram



Address	Register	Abbreviation	Access	Peripheral	Initial value
29H to 2AH	Reserved				
2BH	Serial IO Prescaler	SCDCR	R/W	Serial IO	0 _ _ _ 1 1 1 1B
2CH	Serial Mode Control Register (low-order)	SMCS	R/W		_ _ _ _ 0 0 0 0B
2DH	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial Data Register	SDR	R/W		XXXXXXXXB
2FH	Edge Selector	SES	R/W		_ _ _ _ _ _ _ 0B
30H	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External Interrupt Request Register	EIRR	R/W		XXXXXXXXB
32H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D Data Register 0	ADCR0	R		XXXXXXXXB
37H	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0, 1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Reserved				
3CH	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1B
3DH	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2, 3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Reserved				
40H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4, 5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Reserved				
44H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6, 7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 _ _B
47H	Reserved				
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1B
4AH	PPG8, 9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 _ _B
4BH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910H	Reload Register L	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
1911H	Reload Register H	PRLH8	R/W		XXXXXXXXB
1912H	Reload Register L	PRLL9	R/W		XXXXXXXXB
1913H	Reload Register H	PRLH9	R/W		XXXXXXXXB
1914H	Reload Register L	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1915H	Reload Register H	PRLHA	R/W		XXXXXXXXB
1916H	Reload Register L	PRLLB	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1917H	Reload Register H	PRLHB	R/W		XXXXXXXXB
1918H to 191FH	Reserved				
1920H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXXB
1921H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXXB
1922H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXXB
1923H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXXB
1924H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXXB
1925H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXXB
1926H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXXB
1927H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXXB
1928H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1929H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
192AH	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
192BH	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB

(Continued)

9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60H	DLC register 0	DLCR0	R/W	----XXXXB
001A61H				
001A62H	DLC register 1	DLCR1	R/W	----XXXXB
001A63H				
001A64H	DLC register 2	DLCR2	R/W	----XXXXB
001A65H				
001A66H	DLC register 3	DLCR3	R/W	----XXXXB
001A67H				
001A68H	DLC register 4	DLCR4	R/W	----XXXXB
001A69H				
001A6AH	DLC register 5	DLCR5	R/W	----XXXXB
001A6BH				
001A6CH	DLC register 6	DLCR6	R/W	----XXXXB
001A6DH				
001A6EH	DLC register 7	DLCR7	R/W	----XXXXB
001A6FH				
001A70H	DLC register 8	DLCR8	R/W	----XXXX
001A71H				
001A72H	DLC register 9	DLCR9	R/W	----XXXXB
001A73H				
001A74H	DLC register 10	DLCR10	R/W	----XXXXB
001A75H				
001A76H	DLC register 11	DLCR11	R/W	----XXXXB
001A77H				
001A78H	DLC register 12	DLCR12	R/W	----XXXXB
001A79H				
001A7AH	DLC register 13	DLCR13	R/W	----XXXXB
001A7BH				
001A7CH	DLC register 14	DLCR14	R/W	----XXXXB
001A7DH				
001A7EH	DLC register 15	DLCR15	R/W	----XXXXB
001A7FH				
001A80H to 001A87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

Interrupt source	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	# 08	FFFFDC$_H$	——	——
INT9 instruction	N/A	# 09	FFFFD8$_H$	——	——
Exception	N/A	# 10	FFFFD4$_H$	——	——
CAN RX	N/A	# 11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN TX/NS	N/A	# 12	FFFFCC$_H$		
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8$_H$	ICR01	0000B1$_H$
Time Base Timer	N/A	# 14	FFFFC4$_H$		
16-bit Reload Timer 0	*1	# 15	FFFFC0$_H$	ICR02	0000B2$_H$
8/10-bit A/D Converter	*1	# 16	FFFFBC$_H$		
16-bit Free-run Timer	N/A	# 17	FFFFB8$_H$	ICR03	0000B3$_H$
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4$_H$		
Serial I/O	*1	# 19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt (INT4/INT5)	*1	# 20	FFFFAC$_H$		
Input Capture 0	*1	# 21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	# 22	FFFFA4$_H$		
Output Compare 0	*1	# 23	FFFFA0$_H$	ICR06	0000B6$_H$
8/16-bit PPG 2/3	N/A	# 24	FFFF9C$_H$		
External Interrupt (INT6/INT7)	*1	# 25	FFFF98$_H$	ICR07	0000B7$_H$
Input Capture 1	*1	# 26	FFFF94$_H$		
8/16-bit PPG 4/5	N/A	# 27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 1	*1	# 28	FFFF8C$_H$		
8/16-bit PPG 6/7	N/A	# 29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2	*1	# 30	FFFF84$_H$		
8/16-bit PPG 8/9	N/A	# 31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 2	*1	# 32	FFFF7C$_H$		
Input Capture 3	*1	# 33	FFFF78$_H$	ICR11	0000BB$_H$
8/16-bit PPG A/B	N/A	# 34	FFFF74$_H$		
Output Compare 3	*1	# 35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	# 36	FFFF6C$_H$		
UART 0 RX	*2	# 37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	# 38	FFFF64$_H$		
UART 1 RX	*2	# 39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	# 40	FFFF5C$_H$		
Flash Memory	N/A	# 41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	# 42	FFFF54$_H$		

*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A:The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} − 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/L, AVRH ≥ AVRL *1
	DV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} ≥ DV_{CC}
Input voltage	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Maximum Clamp Current	I_{CLAMP}	−2.0	2.0	mA	*6
Maximum Total Clamp Current	$\sum \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level Max. output current	I_{OL1}	—	15	mA	Normal output *3
“L” level Avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
“L” level Max. output current	I_{OL2}	—	40	mA	High current output *3
“L” level Avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
“L” level Max. overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
“L” level Max. overall output current	$\sum I_{OL2}$	—	330	mA	Total high current output
“L” level Avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
“L” level Avg. overall output current	$\sum I_{OLAV2}$	—	250	mA	Total high current output, average value *5
“H” level Max. output current	I_{OH1}	—	−15	mA	Normal output *3
“H” level Avg. output current	I_{OHAV1}	—	−4	mA	Normal output, average value *4
“H” level Max. output current	I_{OH2}	—	−40	mA	High current output *3
“H” level Avg. output current	I_{OHAV2}	—	−30	mA	High current output, average value *4
“H” level Max. overall output current	$\sum I_{OH1}$	—	−100	mA	Total normal output
“H” level Max. overall output current	$\sum I_{OH2}$	—	−330	mA	Total high current output
“H” level Avg. overall output current	$\sum I_{OHAV1}$	—	−50	mA	Total normal output, average value *5
“H” level Avg. overall output current	$\sum I_{OHAV2}$	—	−250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F598G
		—	400	mW	MB90598G
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1: AV_{CC}, AVRH, AVRL and DV_{CC} shall not exceed V_{CC}. AVRH and AVRL shall not exceed AV_{CC}. Also, AVRL shall never exceed AVRH.

*2: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

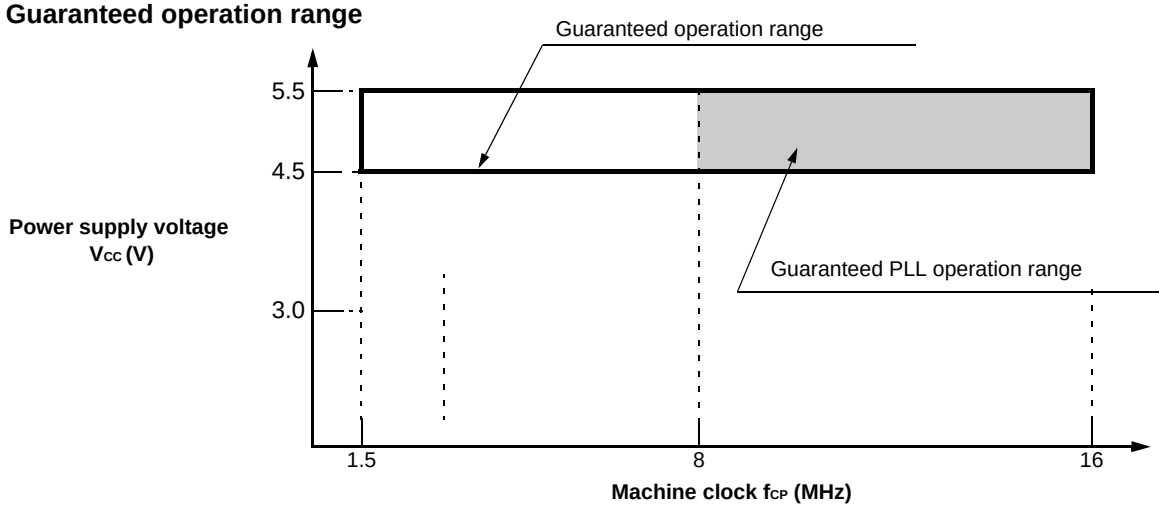
*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

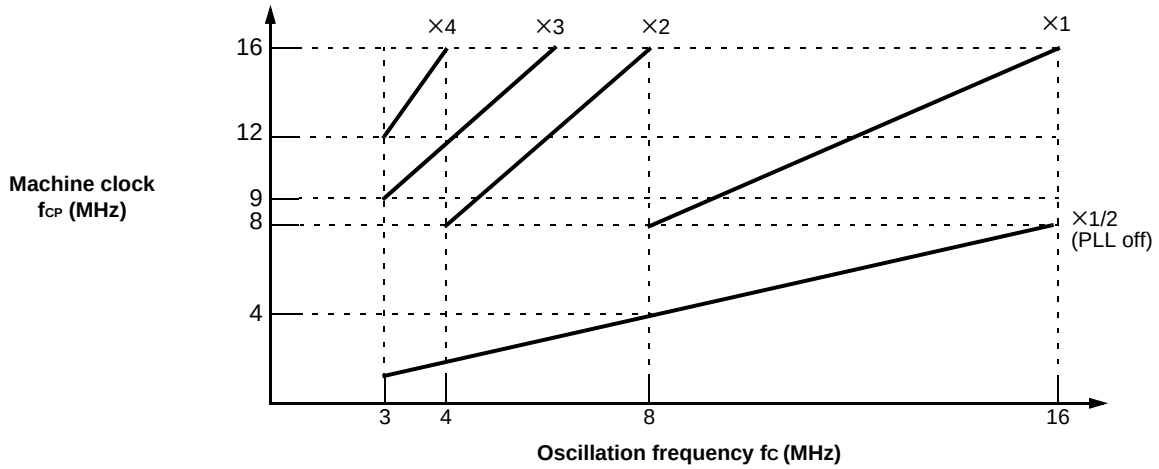
*6:

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

- **Guaranteed operation range**



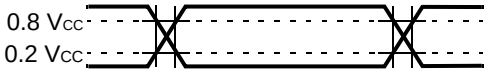
- **Oscillation frequency and machine clock frequency**



AC characteristics are set to the measured reference voltage values below.

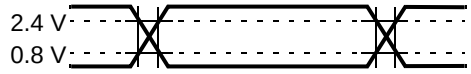
- **Input signal waveform**

Hysteresis Input Pin



- **Output signal waveform**

Output Pin



11.4.2 Reset and Hardware Standby Input

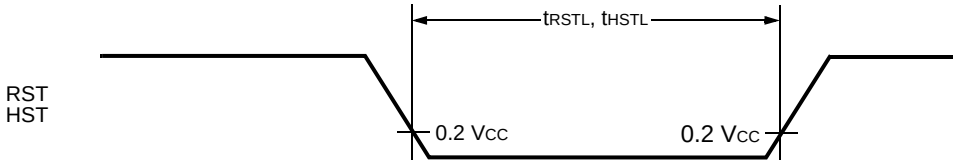
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode

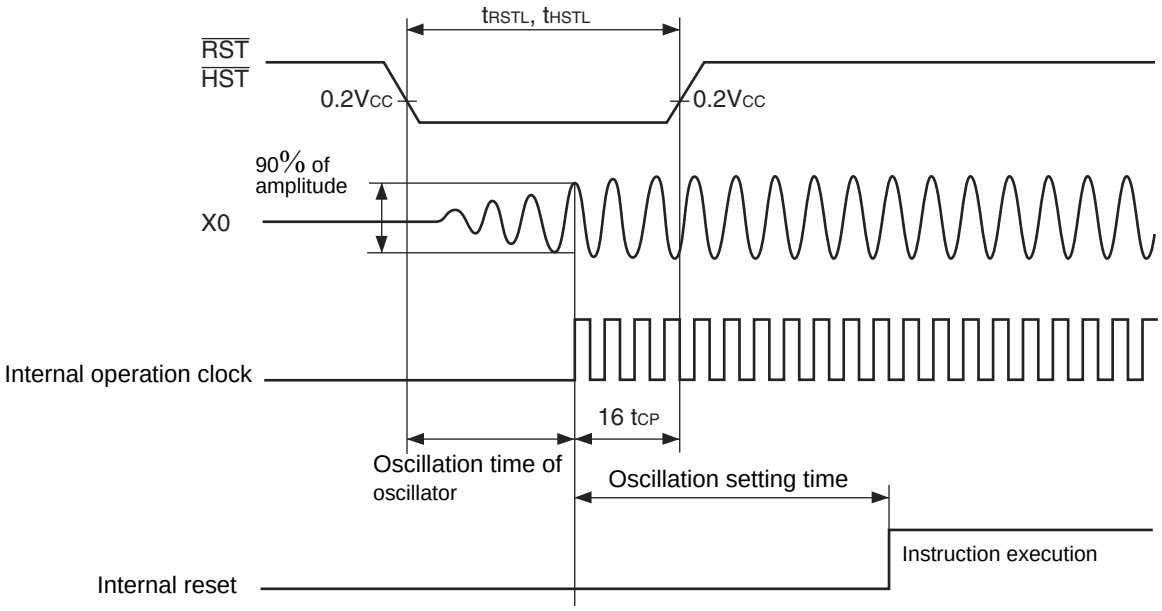
*1: "t_{cp}" represents one cycle time of the machine clock.
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

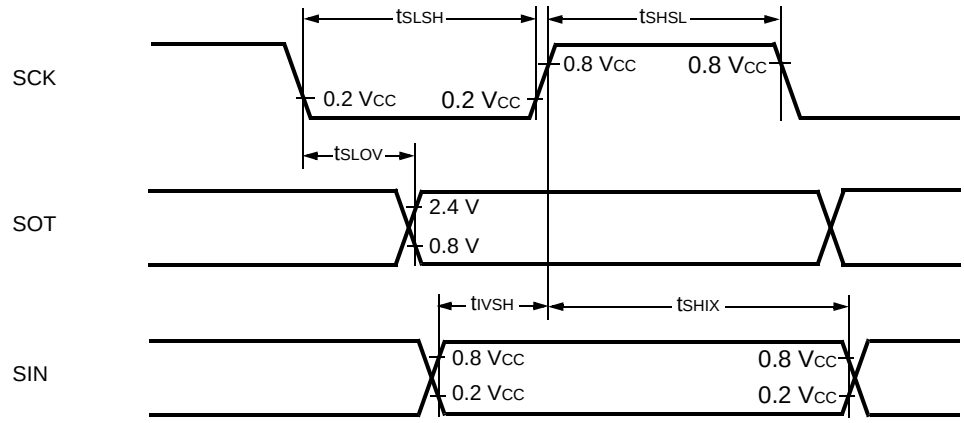
Under Normal Operation



In Stop Mode



• **External Shift Clock Mode**

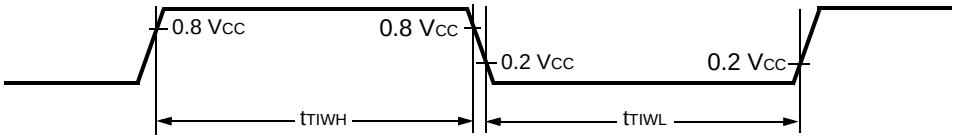


(5) Timer Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN3					

• **Timer Input Timing**



11.4.5 Trigger Input Timing

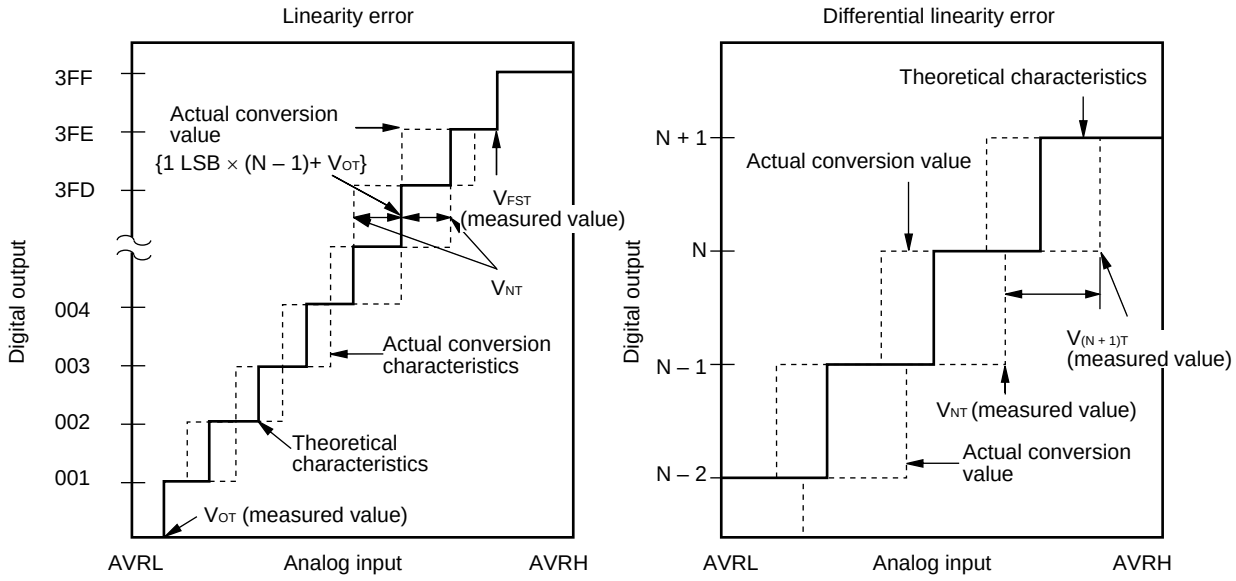
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under normal operation
				1	—	µs	In stop mode

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	—	AVRH	AVRL + 3.0	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 3.0	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	400	600	µA	MB90V595G, MB90F598G
			—	140	600	µA	MB90598G
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at transition of digital output from "000_H" to "001_H"
V_{FST}: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

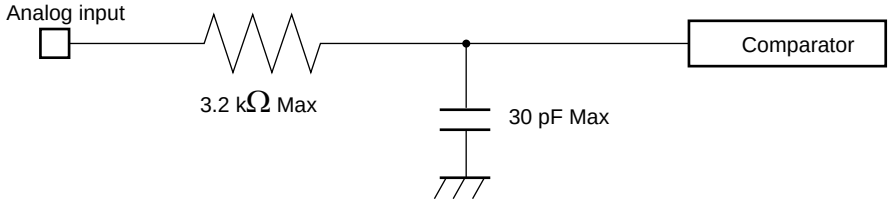
11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions,:

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**

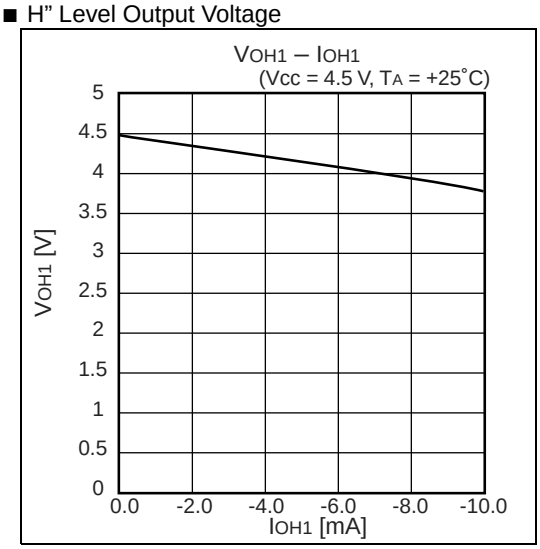


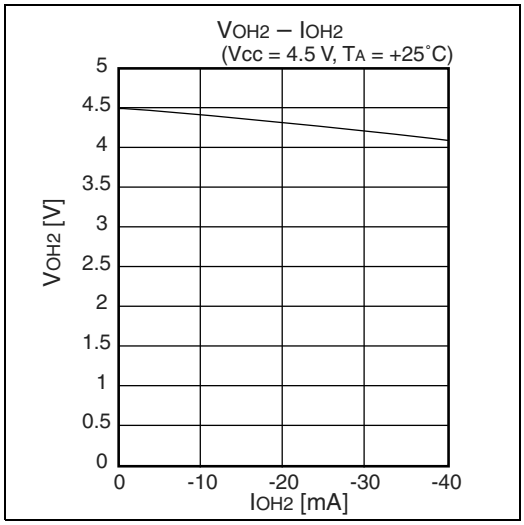
■ Error

The smaller the | AVRH − AVRL |, the greater the error would become relatively.

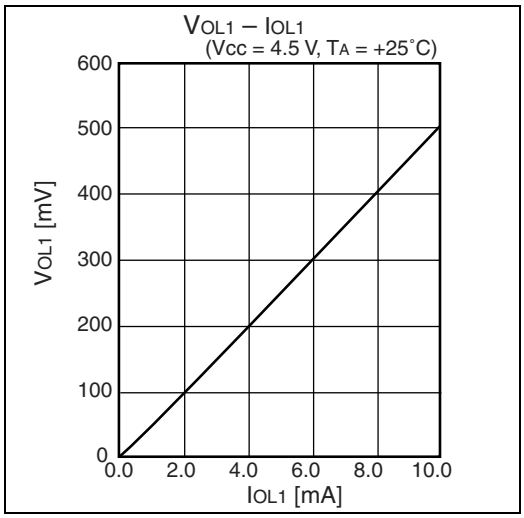
12. Example Characteristics

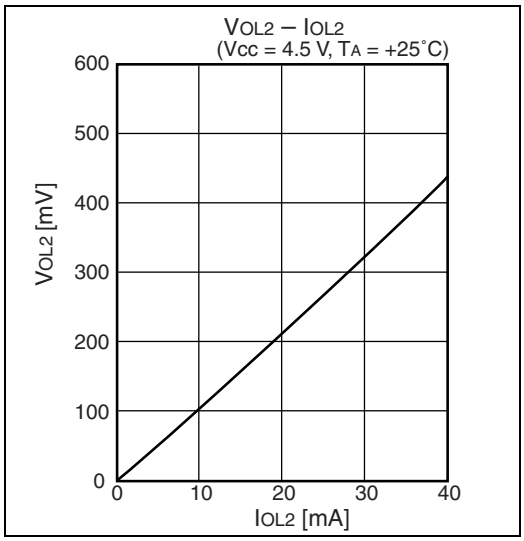
■ H" Level Output Voltage



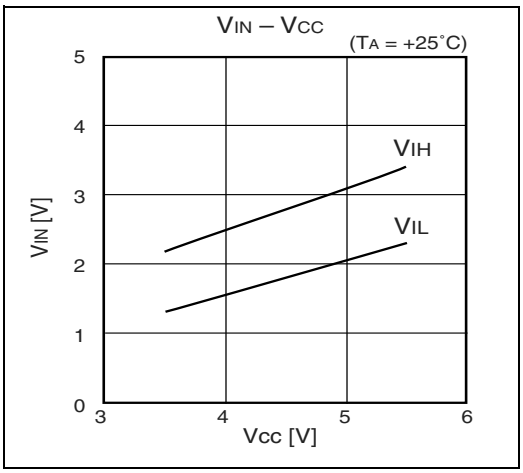


■ L" Level Input Voltage





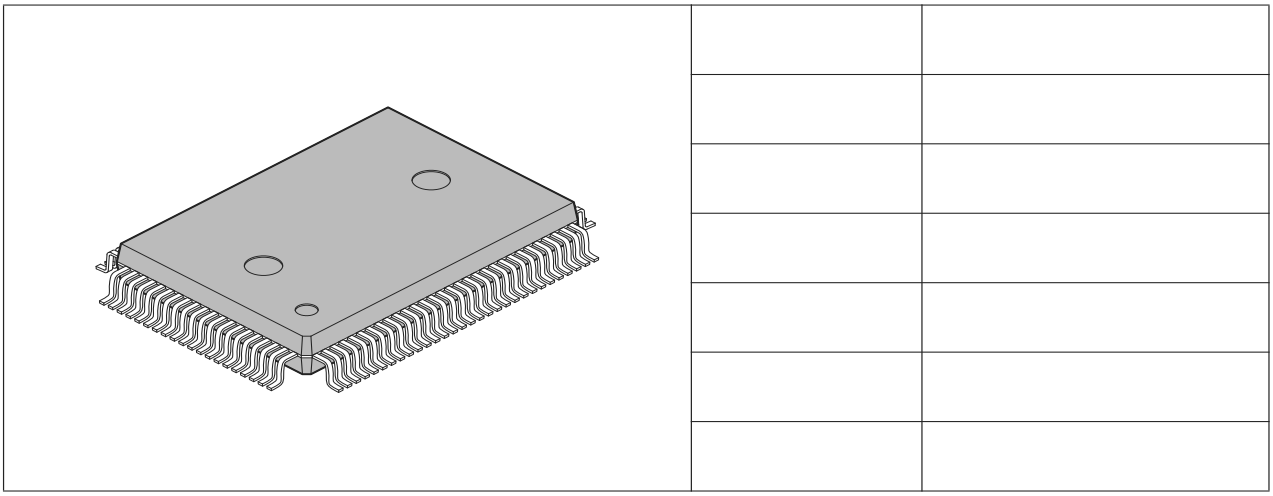
■ H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

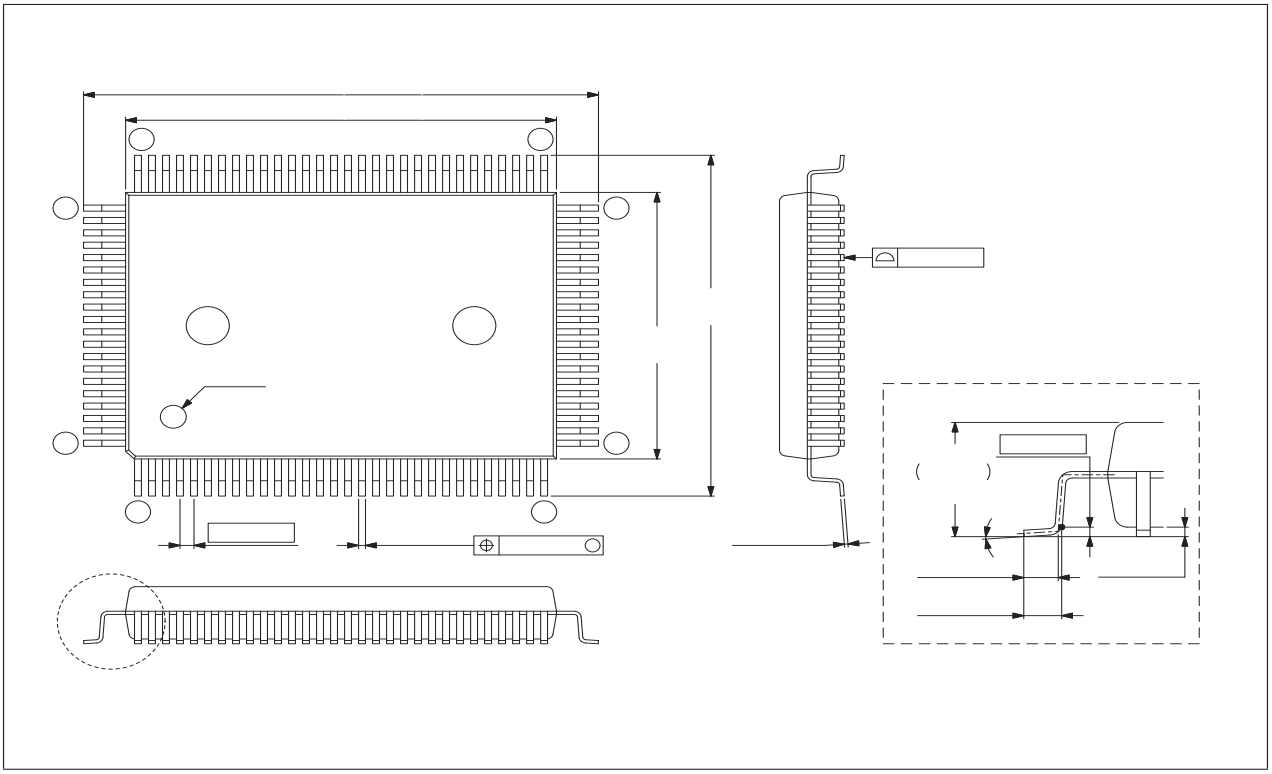


13. Ordering Information

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

14. Package Dimensions





15. Major Changes

Spansion Publication Number: DS07-13705-7E

Section	Change Results
—	Deleted the old products, MB90598, MB90F598, and MB90V595.
—	Changed the series name; MB90595/595G series ? MB90595G series
—	Changed the following erroneous name. I/O timer → 16-bit Free-run Timer
PRODUCT LINEUP	One of Standby mode name is changed. Clock mode → Watch mode
I/O CIRCUIT TYPE	Changed Pull-down resistor value of circuit type H.
ELECTRICAL CHARACTERISTICS AC Characteristics	Add the “External clock input” and “Flash Read cycle time” in (1) Clock Timing
	Figure in (2) Reset and Hardware Standby Input RST/HST input level of “In Stop Mode” is changed. 0.6 V_{CC} 0.2 V_{CC}
ELECTRICAL CHARACTERISTICS 5. A/D Converter	Changed the items of “Zero transition voltage” and “Full scale transition voltage”.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90598G/F598G/V595G F²MC-16LX MB90595G Series CMOS 16-bit Proprietary Microcontroller Document Number: 002-07700				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	09/26/2008	Migrated to Cypress and assigned document number 002-07700. No change to document contents or format.
*A	5537128	AKIH	11/30/2016	Updated to Cypress template

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