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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

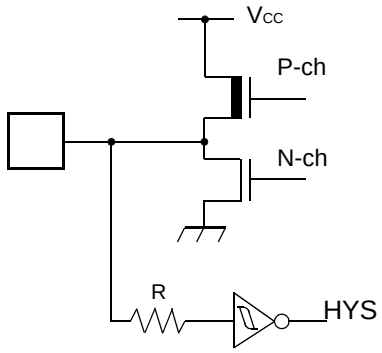
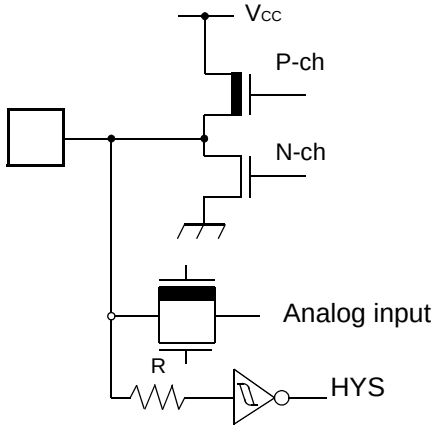
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-151-jne1

Contents

3. Pin Description

Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{\text{RST}}$	B	Reset input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

Circuit Type	Circuit	Remarks
D		■ CMOS output ■ CMOS Hysteresis input
E		■ CMOS output ■ CMOS Hysteresis input ■ Analog input

(Continued)

(5) Pull-up/down resistors
The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit
Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.
A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).
Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter
Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = DV_{CC} = V_{SS}$.

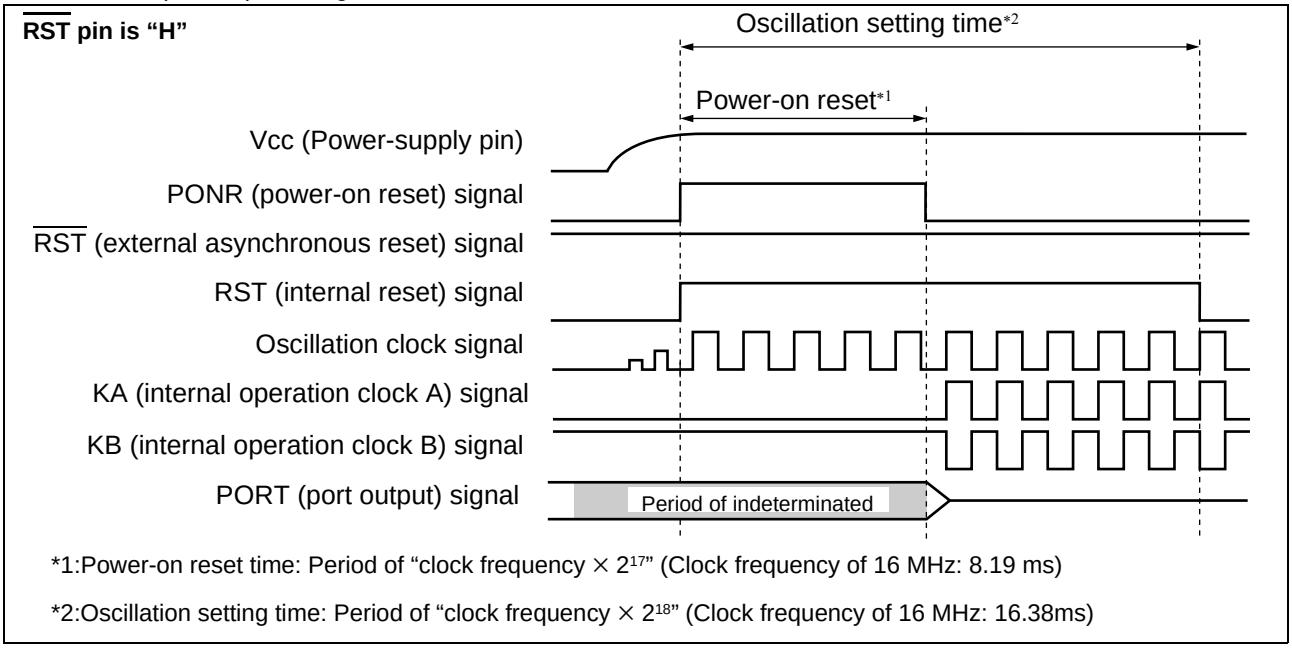
(9) N.C. Pin
The N.C. (internally connected) pin must be opened for use.

(10) Notes on Energization
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

■ If $\overline{RST}$ pin is “H”, the outputs become indeterminate.

■ If $\overline{RST}$ pin is “L”, the outputs become high-impedance.
Pay attention to the port output timing shown as follows.



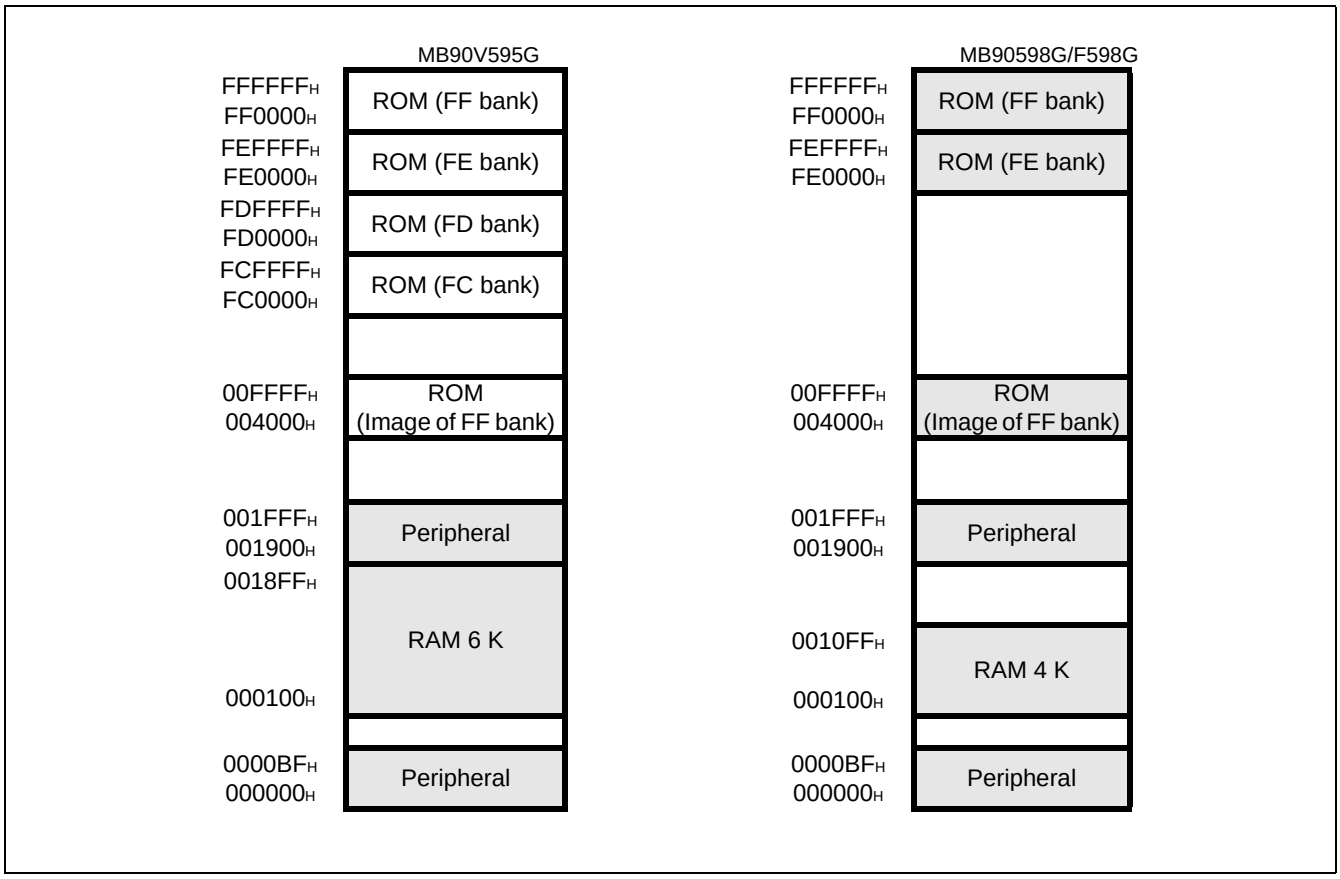
*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)

7. Memory Space

The memory space of the MB90595G Series is shown below

Figure 1. Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access 00C000H , the contents of the ROM at FFC000H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H	Port 7 Data Register	PDR7	R/W	Port 7	$XXXXXXXX_B$
08_H	Port 8 Data Register	PDR8	R/W	Port 8	$XXXXXXXX_B$
09_H	Port 9 Data Register	PDR9	R/W	Port 9	$\_\_XXXXXX_B$
$0A_H$ to $0F_H$	Reserved				
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000_B
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000_B
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000_B
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
17_H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000_B
18_H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000_B
19_H	Port 9 Direction Register	DDR9	R/W	Port 9	$\_\_000000_B$
$1A_H$	Reserved				
$1B_H$	Analog Input Enable Register	ADER	R/W	Port 6, A/D	11111111_B
$1C_H$ to $1F_H$	Reserved				
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	00000100_B
21_H	Serial status Register 0	USR0	R/W		00010000_B
22_H	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W		$XXXXXXXX_B$
23_H	Rate and Data Register 0	URD0	R/W		$0000000X_B$
24_H	Serial Mode Register 1	SMR1	R/W	UART1	00000000_B
25_H	Serial Control Register 1	SCR1	R/W		00000100_B
26_H	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W		$XXXXXXXX_B$
27_H	Serial Status Register 1	SSR1	R/W		0001_00_B
28_H	UART1 Prescaler Control Register	U1CDCR	R/W		$0\_\_\_1111_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910H	Reload Register L	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
1911H	Reload Register H	PRLH8	R/W		XXXXXXXXB
1912H	Reload Register L	PRLL9	R/W		XXXXXXXXB
1913H	Reload Register H	PRLH9	R/W		XXXXXXXXB
1914H	Reload Register L	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1915H	Reload Register H	PRLHA	R/W		XXXXXXXXB
1916H	Reload Register L	PRLLB	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1917H	Reload Register H	PRLHB	R/W		XXXXXXXXB
1918H to 191FH	Reserved				
1920H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXXB
1921H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXXB
1922H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXXB
1923H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXXB
1924H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXXB
1925H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXXB
1926H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXXB
1927H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXXB
1928H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1929H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
192AH	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
192BH	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
192C$_H$	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
192D$_H$	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX$_B$
192E$_H$	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX$_B$
192F$_H$	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX$_B$
1930$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Controller. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Controller. Refer to section about CAN Controller				
1C00$_H$ to 1EFF$_H$	Reserved				
1FF0$_H$	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX$_B$
1FF1$_H$	Program Address Detection Register 0 (middle-order)				XXXXXXXX$_B$
1FF2$_H$	Program Address Detection Register 0 (high-order)				XXXXXXXX$_B$
1FF3$_H$	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX$_B$
1FF4$_H$	Program Address Detection Register 1 (middle-order)				XXXXXXXX$_B$
1FF5$_H$	Program Address Detection Register 1 (high-order)				XXXXXXXX$_B$
1FF6$_H$ to 1FFF$_H$	Reserved				

■ Description for Read/Write
R/W : Readable/writable
R : Read only
W : Write only

■ Description of initial value
0 : the initial value of this bit is "0".
1 : the initial value of this bit is "1".
X : the initial value of this bit is undefined.
_ : this bit is unused. the initial value is undefined.

Note: : Addresses in the range of 0000$_H$ to 00FF$_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

Address	Register	Abbreviation	Access	Initial Value
001A2C$_H$	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX$_B$
001A2D$_H$				
001A2E$_H$				XXXXX--- XXXXXXXX$_B$
001A2F$_H$				
001A30$_H$	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX$_B$
001A31$_H$				
001A32$_H$				XXXXX--- XXXXXXXX$_B$
001A33$_H$				
001A34$_H$	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX$_B$
001A35$_H$				
001A36$_H$				XXXXX--- XXXXXXXX$_B$
001A37$_H$				
001A38$_H$	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX$_B$
001A39$_H$				
001A3A$_H$				XXXXX--- XXXXXXXX$_B$
001A3B$_H$				
001A3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
001A3D$_H$				
001A3E$_H$				XXXXX--- XXXXXXXX$_B$
001A3F$_H$				

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Initial Value
001A40H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXXB
001A41H				
001A42H				XXXXX--- XXXXXXXXB
001A43H				
001A44H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXXB
001A45H				
001A46H				XXXXX--- XXXXXXXXB
001A47H				
001A48H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXXB
001A49H				
001A4AH				XXXXX--- XXXXXXXXB
001A4BH				
001A4CH	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXXB
001A4DH				
001A4EH				XXXXX--- XXXXXXXXB
001A4FH				
001A50H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXXB
001A51H				
001A52H				XXXXX--- XXXXXXXXB
001A53H				
001A54H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXXB
001A55H				
001A56H				XXXXX--- XXXXXXXXB
001A57H				
001A58H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXXB
001A59H				
001A5AH				XXXXX--- XXXXXXXXB
001A5BH				
001A5CH	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXXB
001A5DH				
001A5EH				XXXXX--- XXXXXXXXB
001A5FH				

9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60H	DLC register 0	DLCR0	R/W	----XXXXB
001A61H				
001A62H	DLC register 1	DLCR1	R/W	----XXXXB
001A63H				
001A64H	DLC register 2	DLCR2	R/W	----XXXXB
001A65H				
001A66H	DLC register 3	DLCR3	R/W	----XXXXB
001A67H				
001A68H	DLC register 4	DLCR4	R/W	----XXXXB
001A69H				
001A6AH	DLC register 5	DLCR5	R/W	----XXXXB
001A6BH				
001A6CH	DLC register 6	DLCR6	R/W	----XXXXB
001A6DH				
001A6EH	DLC register 7	DLCR7	R/W	----XXXXB
001A6FH				
001A70H	DLC register 8	DLCR8	R/W	----XXXX
001A71H				
001A72H	DLC register 9	DLCR9	R/W	----XXXXB
001A73H				
001A74H	DLC register 10	DLCR10	R/W	----XXXXB
001A75H				
001A76H	DLC register 11	DLCR11	R/W	----XXXXB
001A77H				
001A78H	DLC register 12	DLCR12	R/W	----XXXXB
001A79H				
001A7AH	DLC register 13	DLCR13	R/W	----XXXXB
001A7BH				
001A7CH	DLC register 14	DLCR14	R/W	----XXXXB
001A7DH				
001A7EH	DLC register 15	DLCR15	R/W	----XXXXB
001A7FH				
001A80H to 001A87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

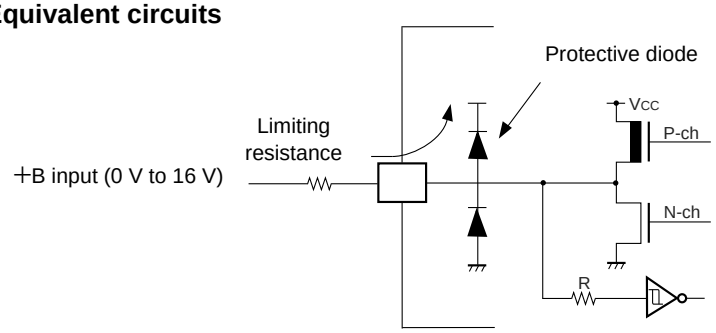
(Continued)

Notes:

- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

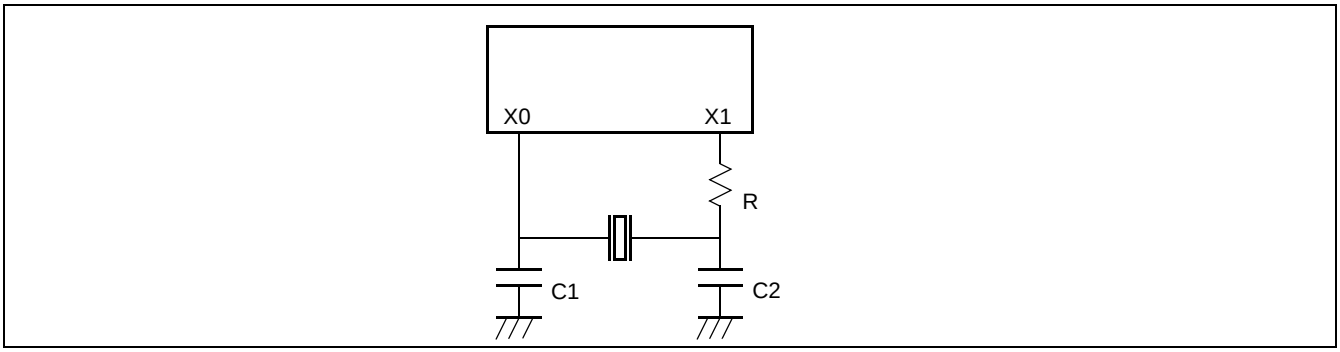
• Input/Output Equivalent circuits



Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ Example of Oscillation circuit

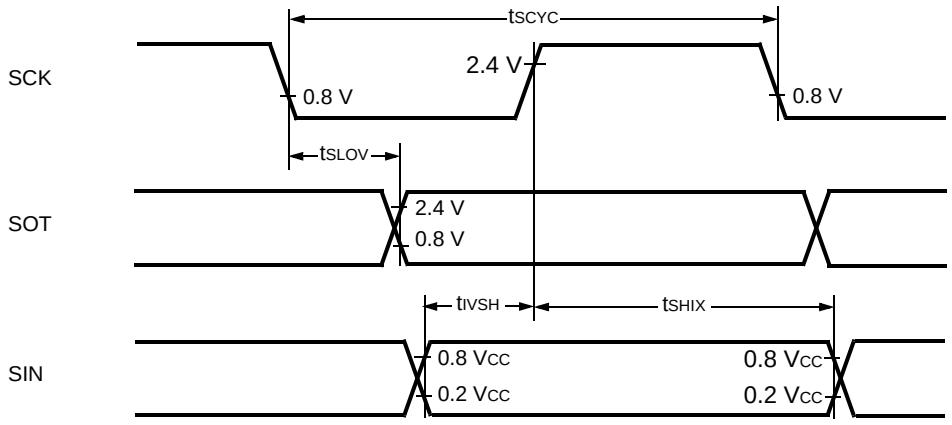


Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{cp} (external operation clock cycle time) : see Clock timing.

- **Internal Shift Clock Mode**



Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	—	AVRH	AVRL + 3.0	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 3.0	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	400	600	µA	MB90V595G, MB90F598G
			—	140	600	µA	MB90598G
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

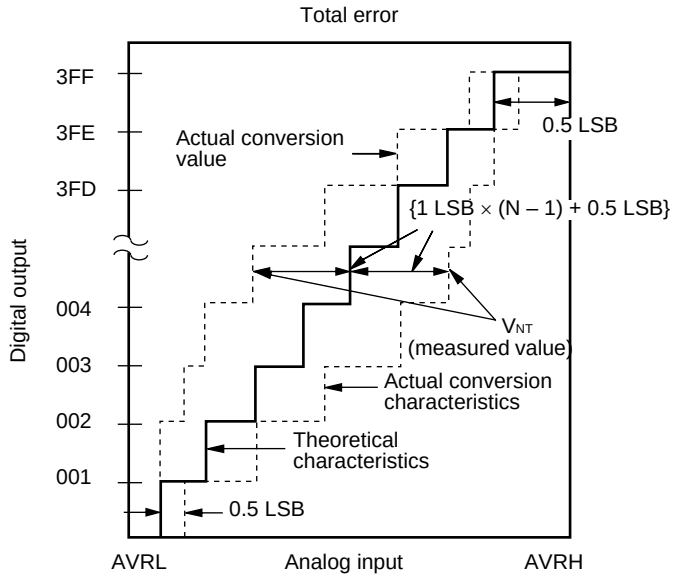
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

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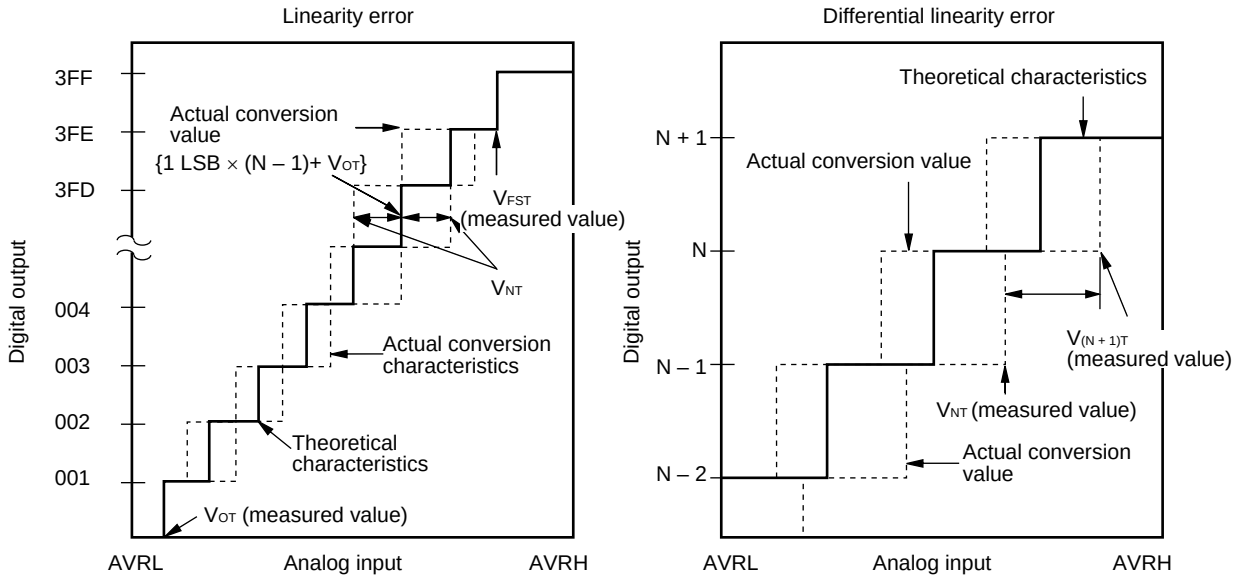


$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at transition of digital output from "000_H" to "001_H"
V_{FST}: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

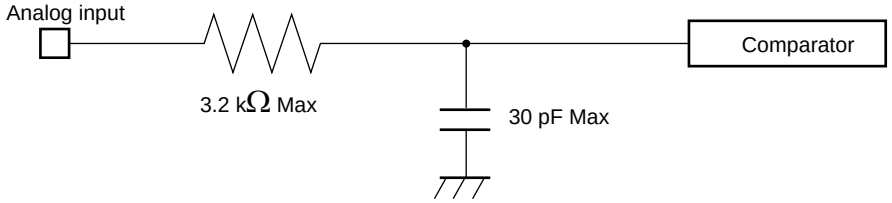
11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions,:

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**



■ Error

The smaller the | AVRH − AVRL |, the greater the error would become relatively.

11.8 Flash memory

■ Erase and programming performance

Parameter	Condition	Value			Unit	Remarks	
		Min	Typ	Max			
Sector erase time	$T_A = +25\ ^{\circ}C$, $V_{CC} = 5.0$ V	—	1	15	s	MB90F598G	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	MB90F598G	Excludes 00H programming prior
Word (16-bit) programming time		—	16	3600	µs	MB90F598G	Excludes system-level overhead
Erase/Program cycle	—	10000	—	—	cycle		

15. Major Changes

Spansion Publication Number: DS07-13705-7E

Section	Change Results
—	Deleted the old products, MB90598, MB90F598, and MB90V595.
—	Changed the series name; MB90595/595G series ? MB90595G series
—	Changed the following erroneous name. I/O timer → 16-bit Free-run Timer
PRODUCT LINEUP	One of Standby mode name is changed. Clock mode → Watch mode
I/O CIRCUIT TYPE	Changed Pull-down resistor value of circuit type H.
ELECTRICAL CHARACTERISTICS AC Characteristics	Add the “External clock input” and “Flash Read cycle time” in (1) Clock Timing
	Figure in (2) Reset and Hardware Standby Input RST/HST input level of “In Stop Mode” is changed. 0.6 V_{CC} 0.2 V_{CC}
ELECTRICAL CHARACTERISTICS 5. A/D Converter	Changed the items of “Zero transition voltage” and “Full scale transition voltage”.

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB90598G/F598G/V595G F²MC-16LX MB90595G Series CMOS 16-bit Proprietary Microcontroller Document Number: 002-07700				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	AKIH	09/26/2008	Migrated to Cypress and assigned document number 002-07700. No change to document contents or format.
*A	5537128	AKIH	11/30/2016	Updated to Cypress template