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What is "Embedded - Microcontrollers"?

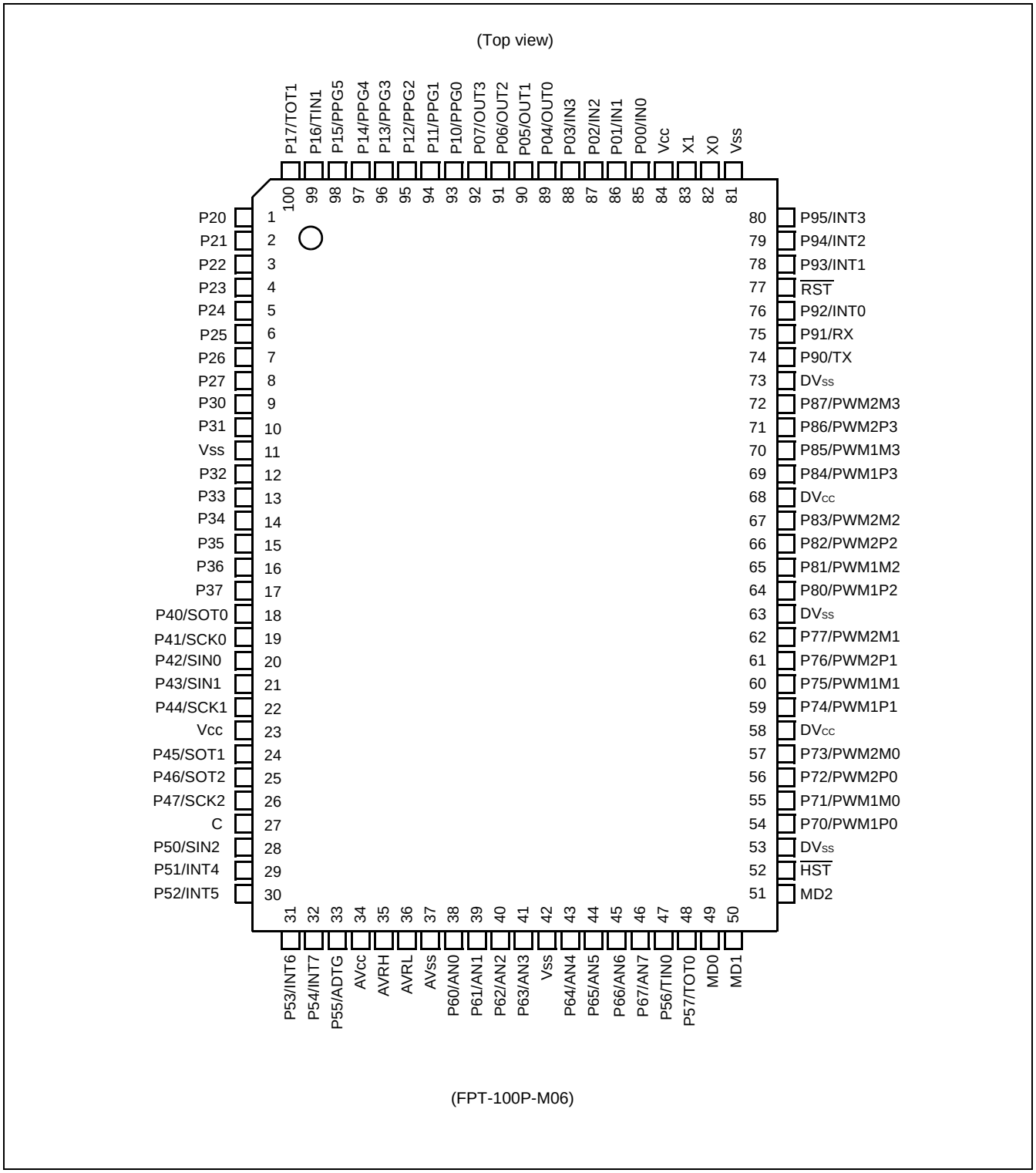
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

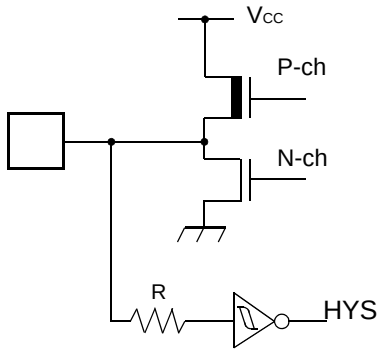
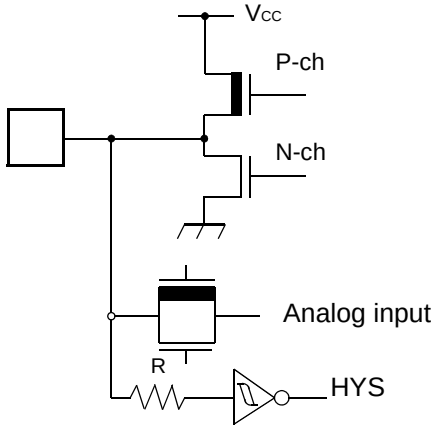
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-151

Contents

2. Pin Assignment



Circuit Type	Circuit	Remarks
D		■ CMOS output ■ CMOS Hysteresis input
E		■ CMOS output ■ CMOS Hysteresis input ■ Analog input

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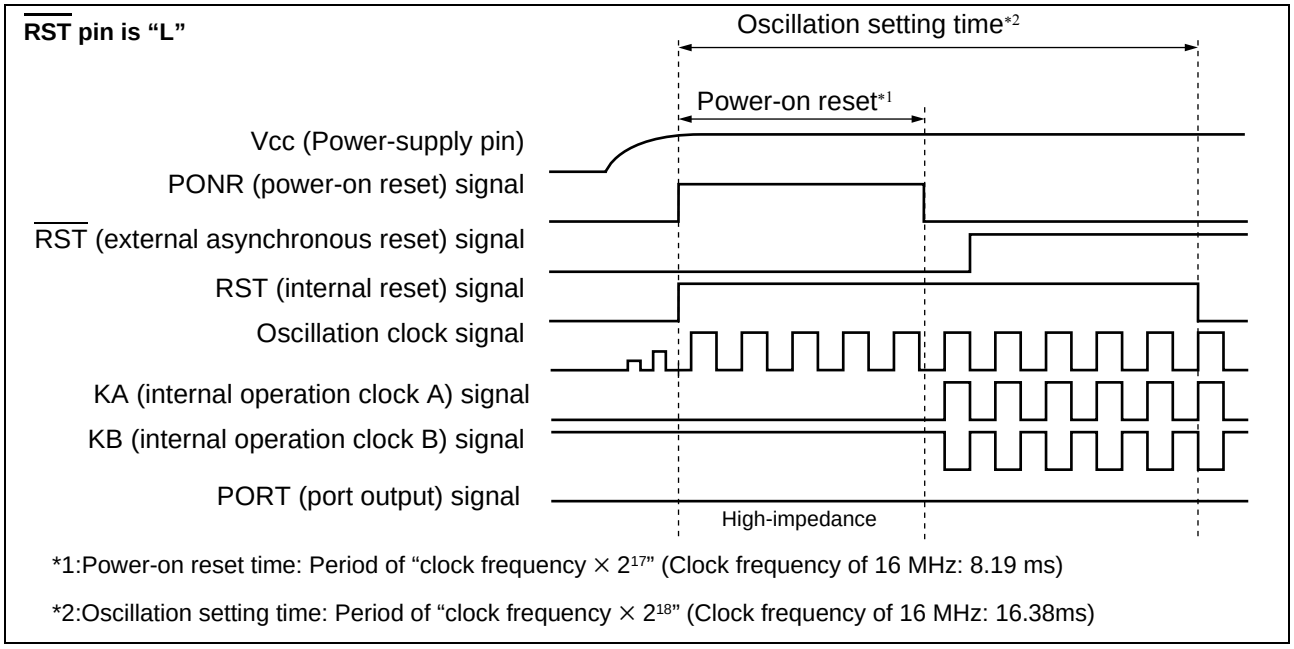


*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)

(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

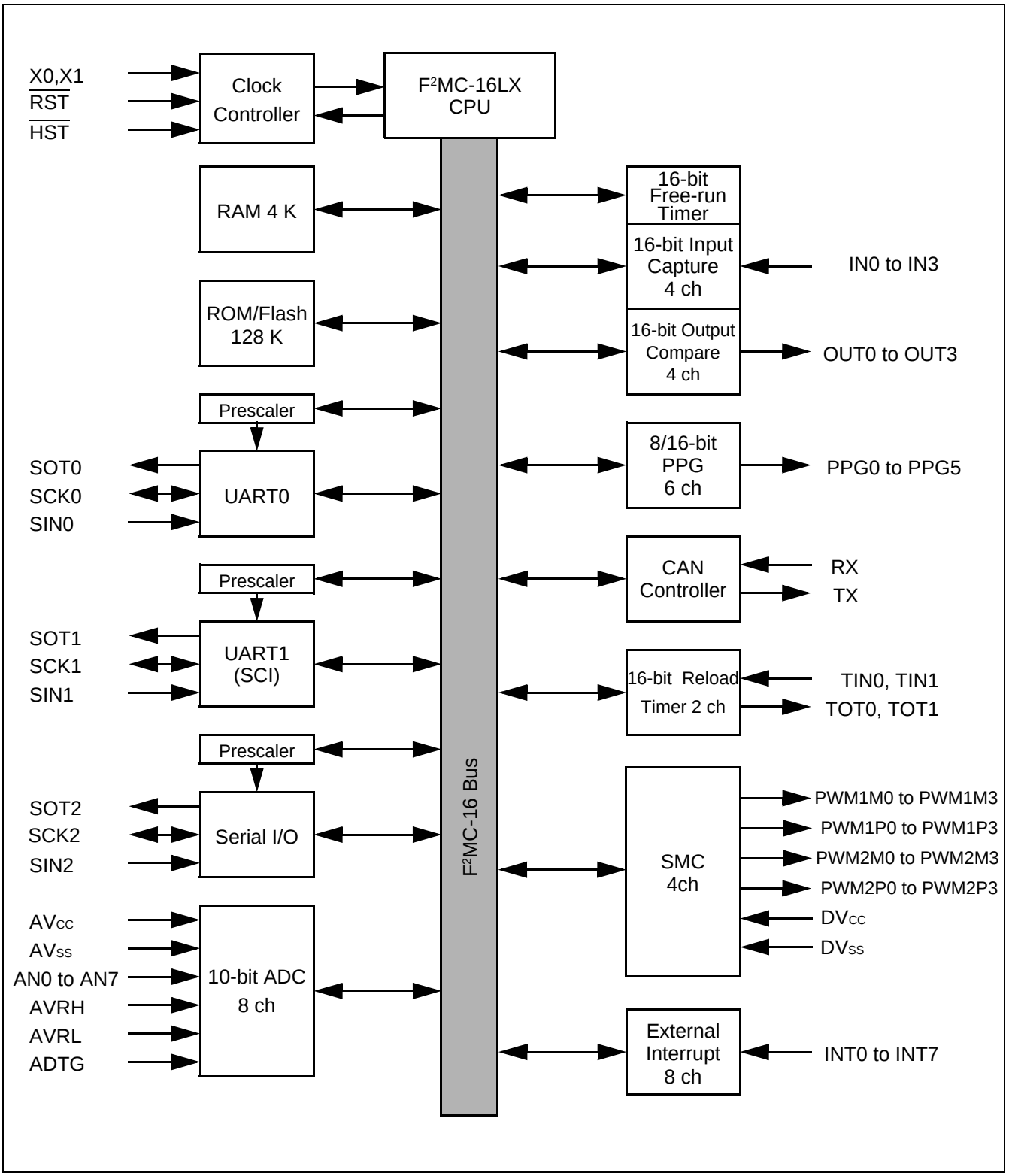
(14) Using REALOS

The use of EI^2OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

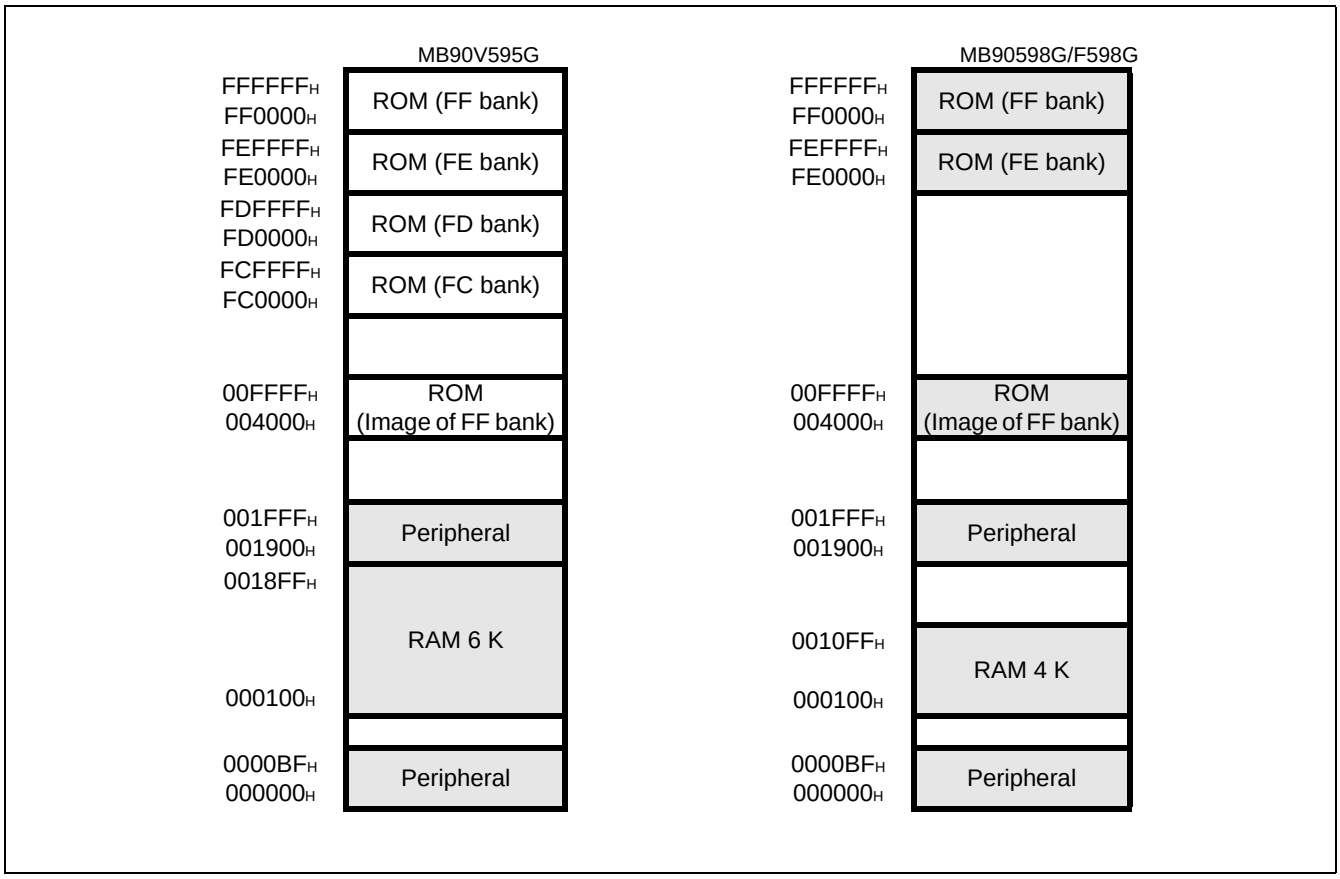
6. Block Diagram



7. Memory Space

The memory space of the MB90595G Series is shown below

Figure 1. Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access 00C000H , the contents of the ROM at FFC000H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

Address	Register	Abbreviation	Access	Peripheral	Initial value
4C$_H$	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0 _ 0 0 0 _ _ 1$_B$
4D$_H$	PPGB Operation Mode Control Register	PPGCB	R/W		0 _ 0 0 0 0 0 1$_B$
4E$_H$	PPGA, B Output Pin Control Register	PPGAB	R/W		0 0 0 0 0 0 _ _$_B$
4F$_H$	Reserved				
50$_H$	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0$_B$
51$_H$	Timer Control Status Register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0$_B$
52$_H$	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W		XXXXXXXX$_B$
53$_H$	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W		XXXXXXXX$_B$
54$_H$	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0$_B$
55$_H$	Timer Control Status Register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0$_B$
56$_H$	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W		XXXXXXXX$_B$
57$_H$	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W		XXXXXXXX$_B$
58$_H$	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0$_B$
59$_H$	Output Compare Control Status Register 1	OCS1	R/W		_ _ _ 0 0 0 0 0$_B$
5A$_H$	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0$_B$
5B$_H$	Output Compare Control Status Register 3	OCS3	R/W		_ _ _ 0 0 0 0 0$_B$
5C$_H$	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0$_B$
5D$_H$	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0$_B$
5E$_H$	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	0 0 0 0 0 _ _ 0$_B$
5F$_H$	Reserved				
60$_H$	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	0 0 0 0 0 _ _ 0$_B$
61$_H$	Reserved				
62$_H$	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	0 0 0 0 0 _ _ 0$_B$
63$_H$	Reserved				
64$_H$	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	0 0 0 0 0 _ _ 0$_B$
65$_H$	Reserved				
66$_H$	Timer Data Register (low-order)	TCDT	R/W	16-bit Free-run Timer	0 0 0 0 0 0 0 0$_B$
67$_H$	Timer Data Register (high-order)	TCDT	R/W		0 0 0 0 0 0 0 0$_B$
68$_H$	Timer Control Status Register	TCCS	R/W		0 0 0 0 0 0 0 0$_B$
69$_H$ to 6E$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
6F$_H$	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1$_B$
70$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
71$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
72$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0$_B$
73$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0$_B$
74$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
75$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
76$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0$_B$
77$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0$_B$
78$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
79$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
7A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0$_B$
7B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0$_B$
7C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
7D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
7E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0$_B$
7F$_H$	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 0$_B$
80$_H$ to 8F$_H$	CAN Controller. Refer to section about CAN Controller				
90$_H$ to 9D$_H$	Reserved				
9E$_H$	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0$_B$
9F$_H$	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0$_B$
A0$_H$	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0$_B$
A1$_H$	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0$_B$
A2$_H$ to A7$_H$	Reserved				
A8$_H$	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1$_B$
A9$_H$	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 _ _ 0 0 1 0 0$_B$
AA$_H$ to AD$_H$	Reserved				
AE$_H$	Flash Memory Control Status Register (MB90F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0$_B$
AF$_H$	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
192C$_H$	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
192D$_H$	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX$_B$
192E$_H$	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX$_B$
192F$_H$	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX$_B$
1930$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Controller. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Controller. Refer to section about CAN Controller				
1C00$_H$ to 1EFF$_H$	Reserved				
1FF0$_H$	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX$_B$
1FF1$_H$	Program Address Detection Register 0 (middle-order)				XXXXXXXX$_B$
1FF2$_H$	Program Address Detection Register 0 (high-order)				XXXXXXXX$_B$
1FF3$_H$	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX$_B$
1FF4$_H$	Program Address Detection Register 1 (middle-order)				XXXXXXXX$_B$
1FF5$_H$	Program Address Detection Register 1 (high-order)				XXXXXXXX$_B$
1FF6$_H$ to 1FFF$_H$	Reserved				

■ Description for Read/Write
R/W : Readable/writable
R : Read only
W : Write only

■ Description of initial value
0 : the initial value of this bit is "0".
1 : the initial value of this bit is "1".
X : the initial value of this bit is undefined.
_ : this bit is unused. the initial value is undefined.

Note: : Addresses in the range of 0000$_H$ to 00FF$_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

9. Can Controller

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame format
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

9.1 List of Control Registers

Address	Register	Abbreviation	Access	Initial Value
000080H	Message buffer valid register	BVALR	R/W	00000000 00000000B
000081H				
000082H	Transmit request register	TREQR	R/W	00000000 00000000B
000083H				
000084H	Transmit cancel register	TCANR	W	00000000 00000000B
000085H				
000086H	Transmit complete register	TCR	R/W	00000000 00000000B
000087H				
000088H	Receive complete register	RCR	R/W	00000000 00000000B
000089H				
00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000B
00008BH				
00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000B
00008DH				
00008EH	Receive interrupt enable register	RIER	R/W	00000000 00000000B
00008FH				
001B00H	Control status register	CSR	R/W, R	00---000 0----0-1B
001B01H				
001B02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
001B03H				
001B04H	Receive/transmit error counter	RTEC	R	00000000 00000000B
001B05H				
001B06H	Bit timing register	BTR	R/W	-1111111 11111111B
001B07H				

(Continued)

Address	Register	Abbreviation	Access	Initial Value
001A2C$_H$	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX$_B$
001A2D$_H$				
001A2E$_H$				XXXXX--- XXXXXXXX$_B$
001A2F$_H$				
001A30$_H$	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX$_B$
001A31$_H$				
001A32$_H$				XXXXX--- XXXXXXXX$_B$
001A33$_H$				
001A34$_H$	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX$_B$
001A35$_H$				
001A36$_H$				XXXXX--- XXXXXXXX$_B$
001A37$_H$				
001A38$_H$	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX$_B$
001A39$_H$				
001A3A$_H$				XXXXX--- XXXXXXXX$_B$
001A3B$_H$				
001A3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
001A3D$_H$				
001A3E$_H$				XXXXX--- XXXXXXXX$_B$
001A3F$_H$				

(Continued)

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

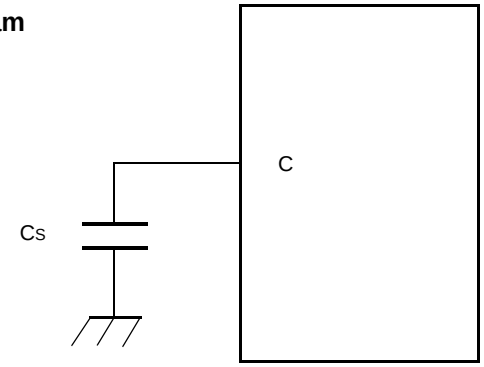
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC} AV_{CC}	4.5	5.0	5.5	V	Under normal operation
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	–40	—	+85	°C	

*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

- **C Pin Connection Diagram**



11.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} +0.3	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} +0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} +0.3	V	
Output H voltage	V_{OH1}	Output pins except P70 to P87	V_{CC} = 4.5 V, I_{OH1} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P70 to P87	V_{CC} = 4.5 V, I_{OH2} = –30.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL1}	Output pins except P70 to P87	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P70 to P87	V_{CC} = 4.5 V, I_{OL2} = 30.0 mA	—	—	0.5	V	

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics

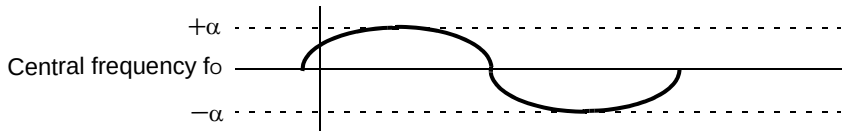
11.4.1 Clock Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

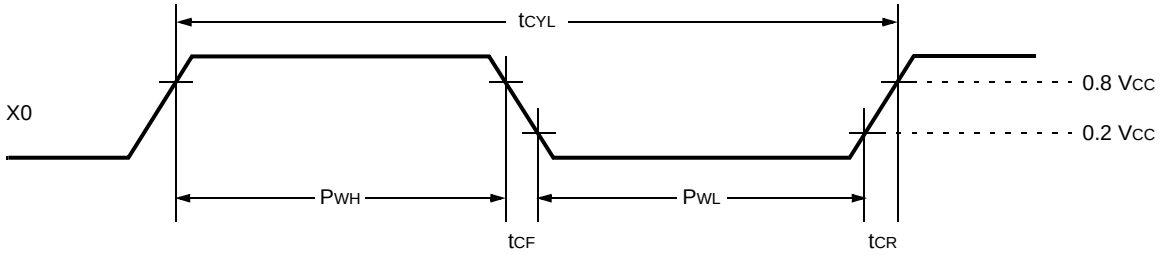
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	5	MHz	When using oscillation circuit
Oscillation cycle time	t_{CYL}	X0, X1	200	—	333	ns	When using oscillation circuit
External clock frequency	f_C	X0, X1	3	—	16	MHz	When using external clock
External clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using external clock
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash Read cycle time	t_{CYL}	—	—	2*t_{CP}	—	ns	When Flash is accessed via CPU

*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

$$\Delta f = \frac{|\alpha|}{fo} \times 100\%$$



- **Clock Timing**



11.4.2 Reset and Hardware Standby Input

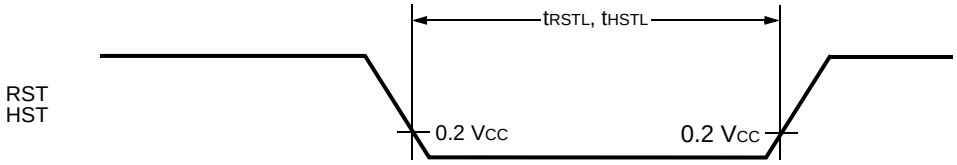
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode

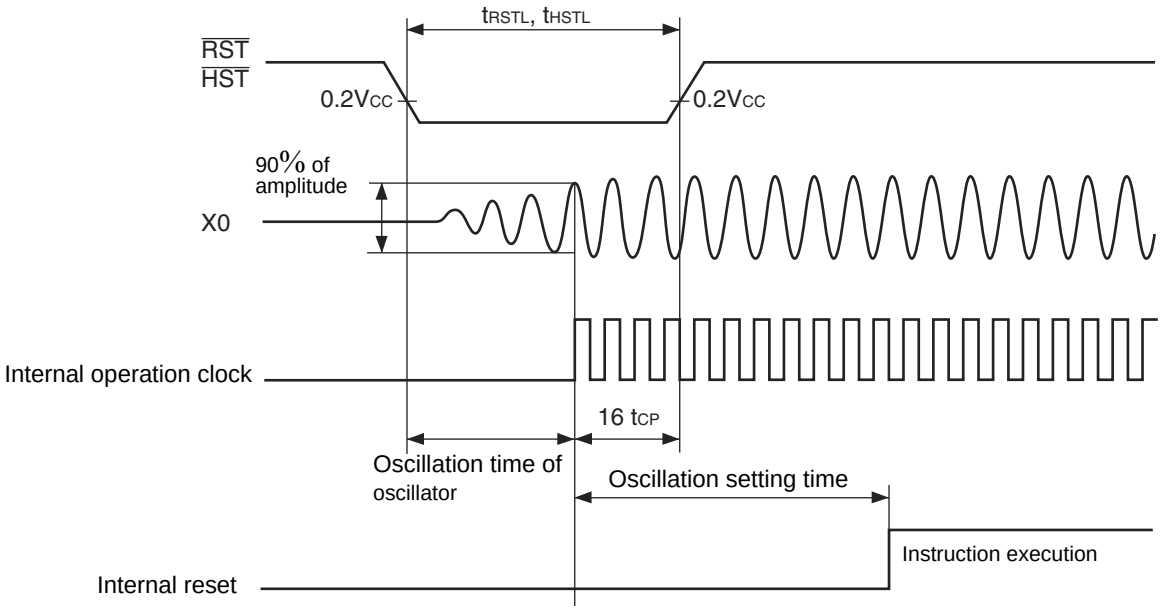
*1: "t_{cp}" represents one cycle time of the machine clock.
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

Under Normal Operation



In Stop Mode

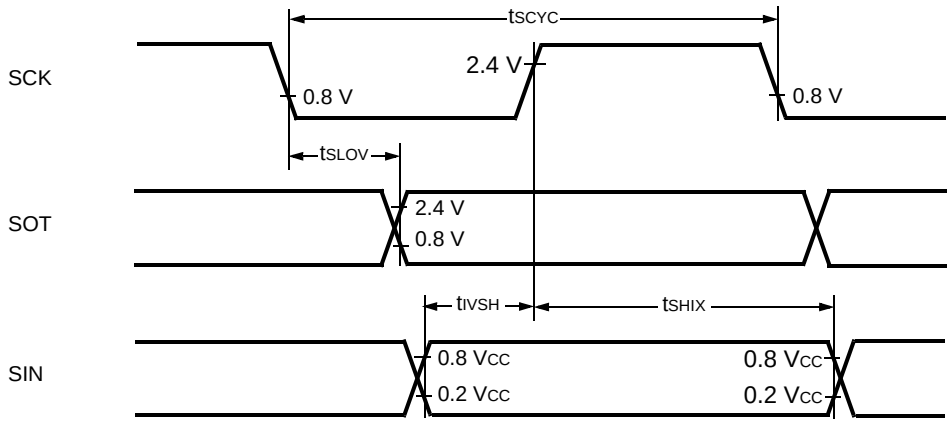


Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

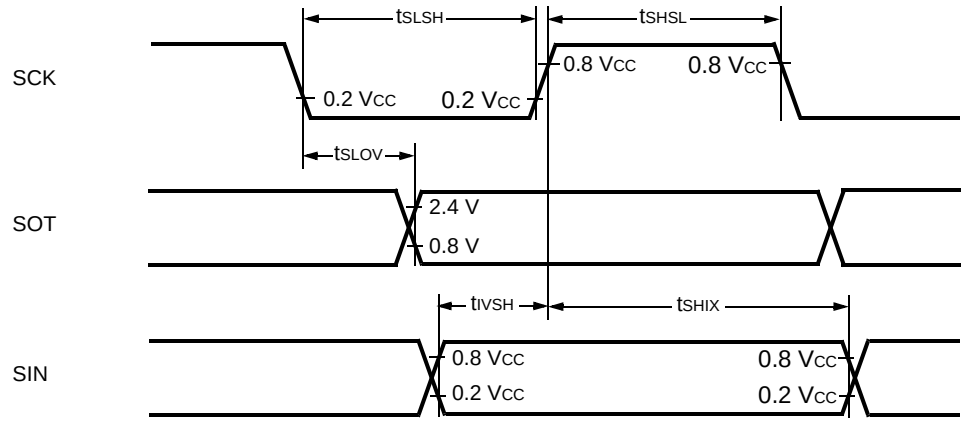
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{cp} (external operation clock cycle time) : see Clock timing.

- **Internal Shift Clock Mode**



• **External Shift Clock Mode**

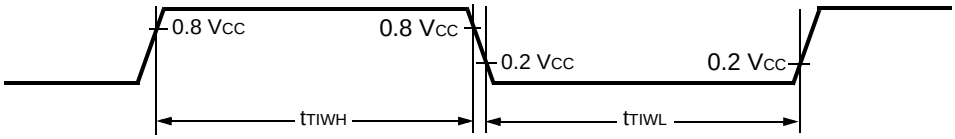


(5) Timer Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP}	—	ns	
	t_{TIWL}	IN0 to IN3					

• **Timer Input Timing**



11.4.5 Trigger Input Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT0 to INT7, ADTG	—	5 t_{CP}	—	ns	Under normal operation
				1	—	µs	In stop mode

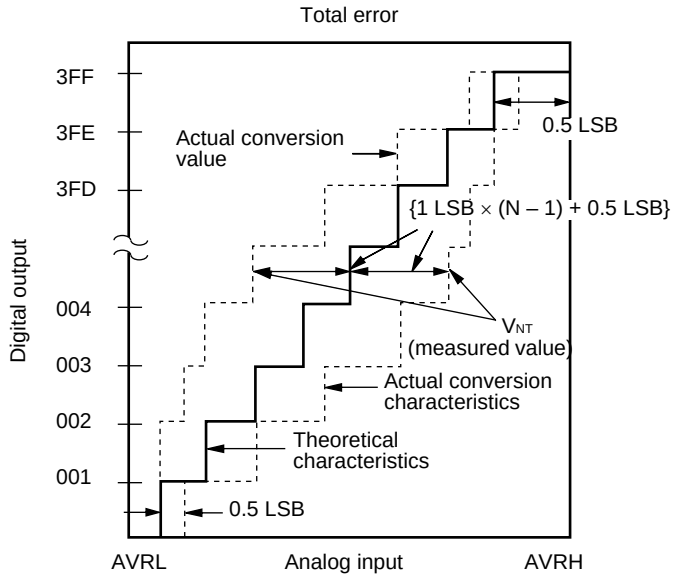
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)

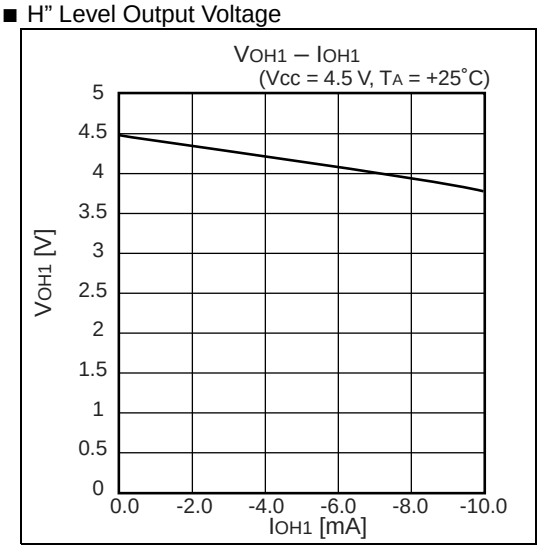
11.8 Flash memory

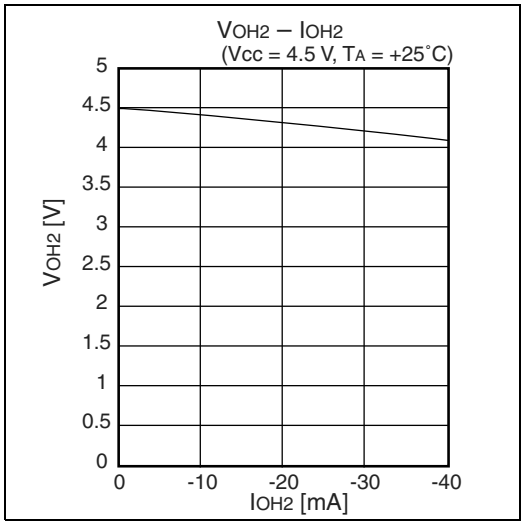
■ Erase and programming performance

Parameter	Condition	Value			Unit	Remarks	
		Min	Typ	Max			
Sector erase time	$T_A = +25\ ^{\circ}C$, $V_{CC} = 5.0$ V	—	1	15	s	MB90F598G	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	MB90F598G	Excludes 00H programming prior
Word (16-bit) programming time		—	16	3600	µs	MB90F598G	Excludes system-level overhead
Erase/Program cycle	—	10000	—	—	cycle		

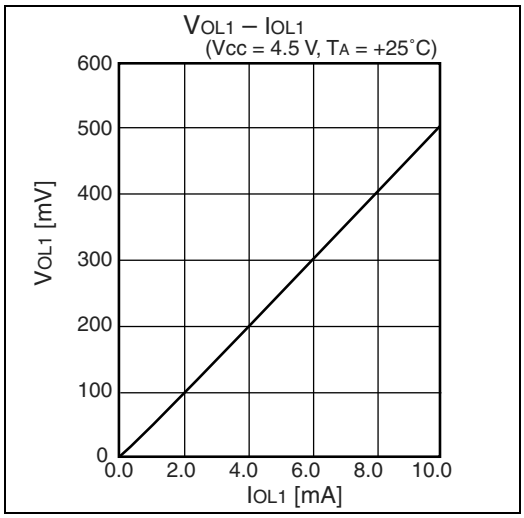
12. Example Characteristics

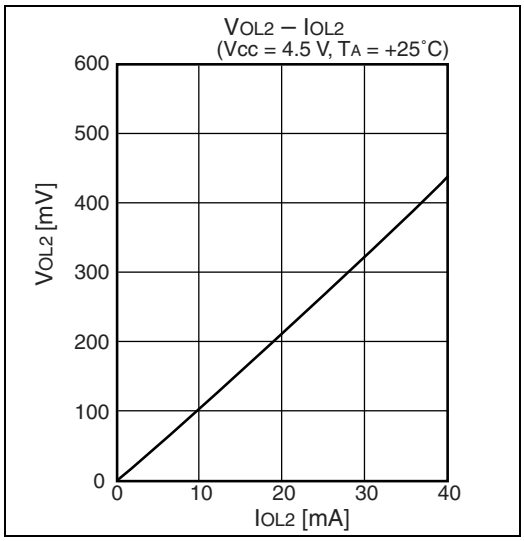
■ H" Level Output Voltage



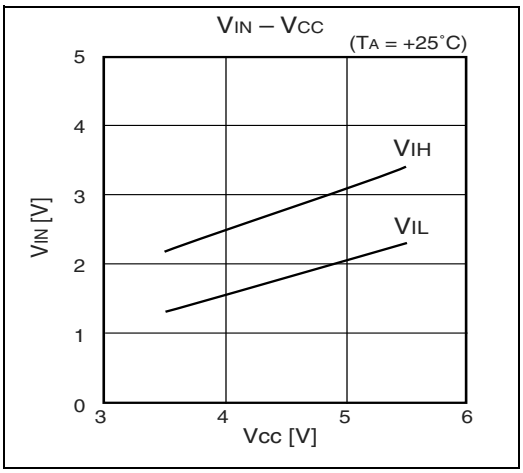


■ L" Level Input Voltage





■ H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)



13. Ordering Information

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

14. Package Dimensions