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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-152-jne1

Contents

1. Product Lineup

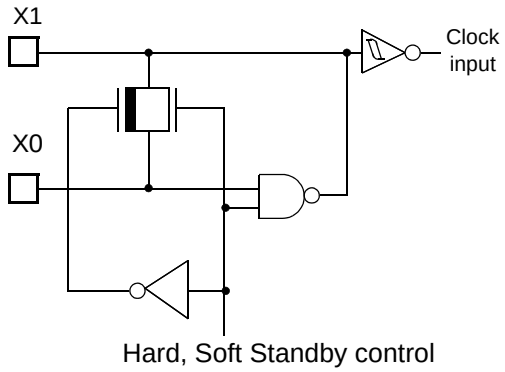
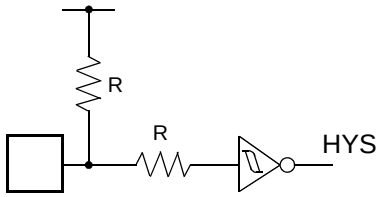
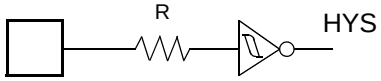
Features		MB90598G	MB90F598G	MB90V595G
Classification		Mask ROM product	Flash ROM product	Evaluation product
ROM size		128 Kbytes	128 Kbytes Boot block Hard-wired reset vector	None
RAM size		4 Kbytes	4 Kbytes	6 Kbytes
Emulator-specific power supply *1		—		None
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 μs (at machine clock frequency of 16 MHz, minimum value)		
UART0		Clock synchronized transmission (500 K/1 M/2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
UART1(SCI)		Clock synchronized transmission (62.5 K/125 K/250 K/500 K/1 Mbps) Clock asynchronized transmission (1202/2404/4808/9615/31250 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers (6 channels)		Number of channels: 6 (8/16-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: fsys, fsys/2^1, fsys/2^2, fsys/2^3, fsys/2^4 (fsys = system clock frequency) 128μs (fosc = 4MHz: oscillation clock frequency)		
16-bit Reload timer		Number of channels: 2 Operation clock frequency: fsys/2^1, fsys/2^3, fsys/2^5 (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)		

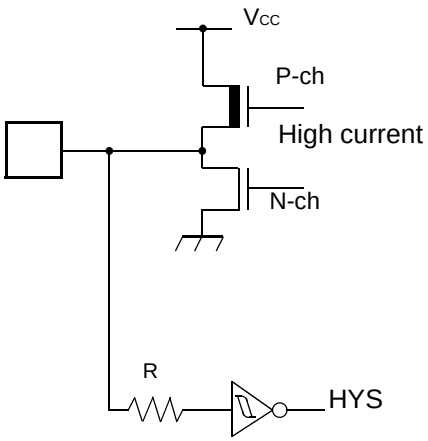
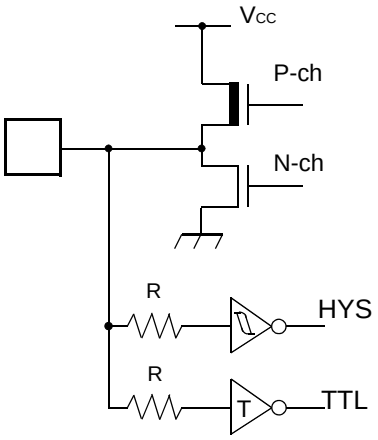
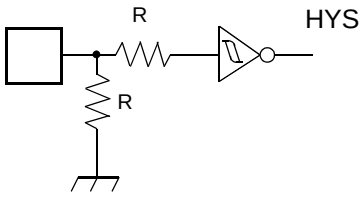
3. Pin Description

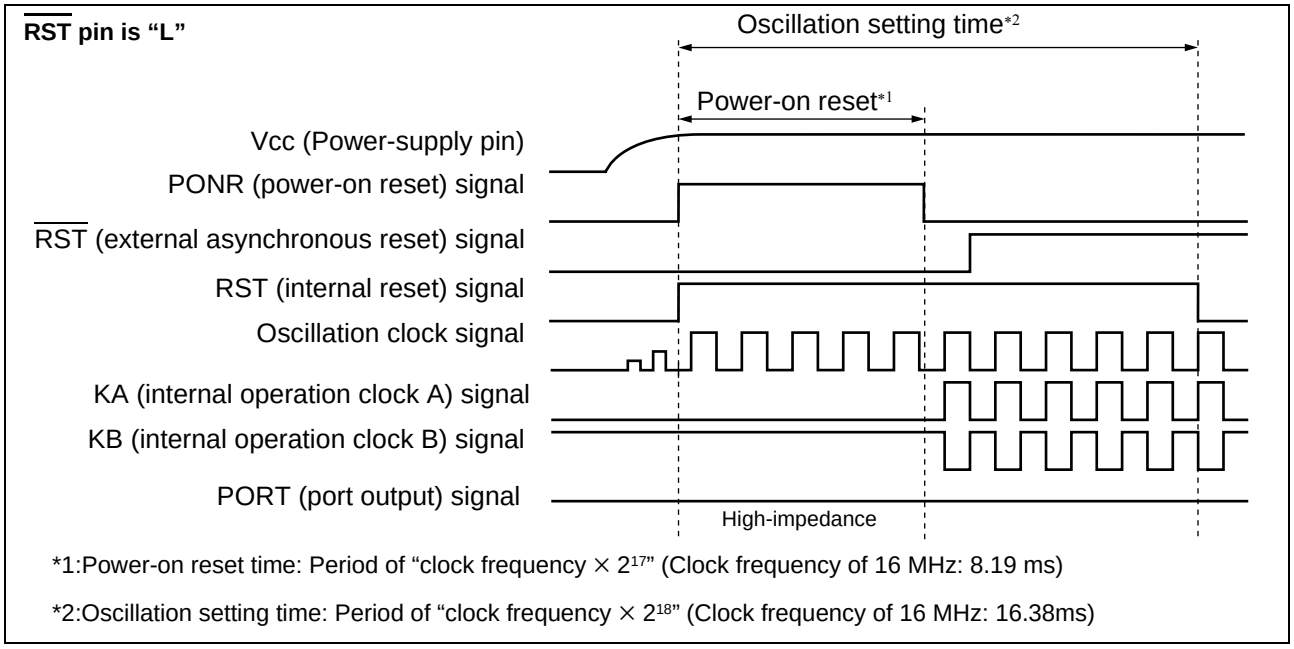
Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{\text{RST}}$	B	Reset input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

Pin no.	Pin name	Circuit type	Function
76	P92	D	General purpose IO
	INT0		External interrupt input for INT0
78 to 80	P93 to P95	D	General purpose IO
	INT1 to INT3		External interrupt input for INT1 to INT3
58, 68	DV_{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV_{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV_{CC}	Power supply	Dedicated power supply pin for the A/D Converter
37	AV_{SS}	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter
49, 50	MD0 MD1	C	Operating mode selection input pins. These pins should be connected to V_{CC} or V_{SS}.
51	MD2	H	Operating mode selection input pin. This pin should be connected to V_{CC} or V_{SS}.
27	C	—	External capacitor pin. A capacitor of 0.1μF should be connected to this pin and V_{SS}.
23, 84	V_{CC}	Power supply	Power supply pins (5.0 V).
11, 42, 81	V_{SS}	Power supply	Ground pins (0.0 V).

4. I/O Circuit Type

Circuit Type	Circuit	Remarks
A		■ Oscillation feedback resistor: 1 MΩ approx.
B		■ Hysteresis input with pull-up Resistor: 50 kΩ approx.
C		■ Hysteresis input

Circuit Type	Circuit	Remarks
F		■ CMOS high current output ■ CMOS Hysteresis input
G		■ CMOS output ■ CMOS Hysteresis input ■ TTL input (MB90F598G, only in Flash mode)
H		■ Hysteresis input Pull-down Resistor: 50 kΩ approx. (except MB90F598G)



*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)

(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(14) Using REALOS

The use of EI^2OS is not possible with the REALOS real time operating system.

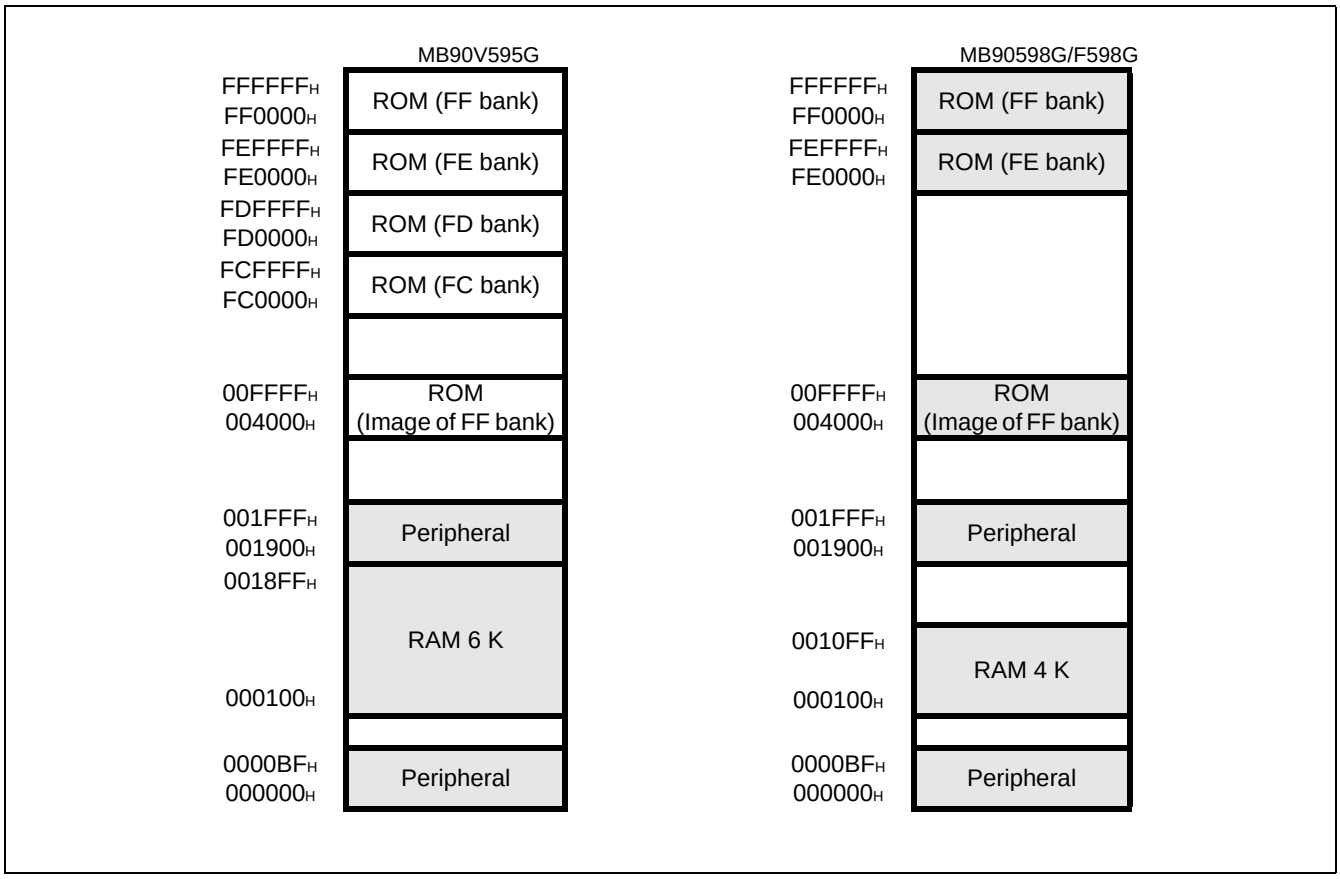
(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

7. Memory Space

The memory space of the MB90595G Series is shown below

Figure 1. Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access 00C000H , the contents of the ROM at FFC000H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

Address	Register	Abbreviation	Access	Peripheral	Initial value
6F$_H$	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1$_B$
70$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
71$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
72$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0$_B$
73$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0$_B$
74$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
75$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
76$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0$_B$
77$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0$_B$
78$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
79$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
7A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0$_B$
7B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0$_B$
7C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
7D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
7E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0$_B$
7F$_H$	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 0$_B$
80$_H$ to 8F$_H$	CAN Controller. Refer to section about CAN Controller				
90$_H$ to 9D$_H$	Reserved				
9E$_H$	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0$_B$
9F$_H$	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0$_B$
A0$_H$	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0$_B$
A1$_H$	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0$_B$
A2$_H$ to A7$_H$	Reserved				
A8$_H$	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1$_B$
A9$_H$	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 _ _ 0 0 1 0 0$_B$
AA$_H$ to AD$_H$	Reserved				
AE$_H$	Flash Memory Control Status Register (MB90F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0$_B$
AF$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
$B0_H$	Interrupt Control Register 00	ICR00	R/W	Interrupt controller	00000111$_B$
$B1_H$	Interrupt Control Register 01	ICR01	R/W		00000111$_B$
$B2_H$	Interrupt Control Register 02	ICR02	R/W		00000111$_B$
$B3_H$	Interrupt Control Register 03	ICR03	R/W		00000111$_B$
$B4_H$	Interrupt Control Register 04	ICR04	R/W	Interrupt controller	00000111$_B$
$B5_H$	Interrupt Control Register 05	ICR05	R/W		00000111$_B$
$B6_H$	Interrupt Control Register 06	ICR06	R/W		00000111$_B$
$B7_H$	Interrupt Control Register 07	ICR07	R/W		00000111$_B$
$B8_H$	Interrupt Control Register 08	ICR08	R/W		00000111$_B$
$B9_H$	Interrupt Control Register 09	ICR09	R/W		00000111$_B$
BA_H	Interrupt Control Register 10	ICR10	R/W		00000111$_B$
BB_H	Interrupt Control Register 11	ICR11	R/W		00000111$_B$
BC_H	Interrupt Control Register 12	ICR12	R/W		00000111$_B$
BD_H	Interrupt Control Register 13	ICR13	R/W		00000111$_B$
BE_H	Interrupt Control Register 14	ICR14	R/W		00000111$_B$
BF_H	Interrupt Control Register 15	ICR15	R/W		00000111$_B$
$C0_H$ to FF_H	Reserved				
1900_H	Reload Register L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX$_B$
1901_H	Reload Register H	PRLH0	R/W		XXXXXXXX$_B$
1902_H	Reload Register L	PRLL1	R/W		XXXXXXXX$_B$
1903_H	Reload Register H	PRLH1	R/W		XXXXXXXX$_B$
1904_H	Reload Register L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX$_B$
1905_H	Reload Register H	PRLH2	R/W		XXXXXXXX$_B$
1906_H	Reload Register L	PRLL3	R/W		XXXXXXXX$_B$
1907_H	Reload Register H	PRLH3	R/W		XXXXXXXX$_B$
1908_H	Reload Register L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX$_B$
1909_H	Reload Register H	PRLH4	R/W		XXXXXXXX$_B$
$190A_H$	Reload Register L	PRLL5	R/W		XXXXXXXX$_B$
$190B_H$	Reload Register H	PRLH5	R/W		XXXXXXXX$_B$
$190C_H$	Reload Register L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX$_B$
$190D_H$	Reload Register H	PRLH6	R/W		XXXXXXXX$_B$
$190E_H$	Reload Register L	PRLL7	R/W		XXXXXXXX$_B$
$190F_H$	Reload Register H	PRLH7	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910H	Reload Register L	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
1911H	Reload Register H	PRLH8	R/W		XXXXXXXXB
1912H	Reload Register L	PRLL9	R/W		XXXXXXXXB
1913H	Reload Register H	PRLH9	R/W		XXXXXXXXB
1914H	Reload Register L	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1915H	Reload Register H	PRLHA	R/W		XXXXXXXXB
1916H	Reload Register L	PRLLB	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1917H	Reload Register H	PRLHB	R/W		XXXXXXXXB
1918H to 191FH	Reserved				
1920H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXXB
1921H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXXB
1922H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXXB
1923H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXXB
1924H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXXB
1925H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXXB
1926H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXXB
1927H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXXB
1928H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1929H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
192AH	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
192BH	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
192C$_H$	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
192D$_H$	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX$_B$
192E$_H$	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX$_B$
192F$_H$	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX$_B$
1930$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Controller. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Controller. Refer to section about CAN Controller				
1C00$_H$ to 1EFF$_H$	Reserved				
1FF0$_H$	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX$_B$
1FF1$_H$	Program Address Detection Register 0 (middle-order)				XXXXXXXX$_B$
1FF2$_H$	Program Address Detection Register 0 (high-order)				XXXXXXXX$_B$
1FF3$_H$	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX$_B$
1FF4$_H$	Program Address Detection Register 1 (middle-order)				XXXXXXXX$_B$
1FF5$_H$	Program Address Detection Register 1 (high-order)				XXXXXXXX$_B$
1FF6$_H$ to 1FFF$_H$	Reserved				

■ Description for Read/Write
R/W : Readable/writable
R : Read only
W : Write only

■ Description of initial value
0 : the initial value of this bit is "0".
1 : the initial value of this bit is "1".
X : the initial value of this bit is undefined.
_ : this bit is unused. the initial value is undefined.

Note: : Addresses in the range of 0000$_H$ to 00FF$_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

Address	Register	Abbreviation	Access	Initial Value
001A2C$_H$	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX$_B$
001A2D$_H$				
001A2E$_H$				XXXXX--- XXXXXXXX$_B$
001A2F$_H$				
001A30$_H$	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX$_B$
001A31$_H$				
001A32$_H$				XXXXX--- XXXXXXXX$_B$
001A33$_H$				
001A34$_H$	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX$_B$
001A35$_H$				
001A36$_H$				XXXXX--- XXXXXXXX$_B$
001A37$_H$				
001A38$_H$	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX$_B$
001A39$_H$				
001A3A$_H$				XXXXX--- XXXXXXXX$_B$
001A3B$_H$				
001A3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
001A3D$_H$				
001A3E$_H$				XXXXX--- XXXXXXXX$_B$
001A3F$_H$				

(Continued)

9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60H	DLC register 0	DLCR0	R/W	----XXXXB
001A61H				
001A62H	DLC register 1	DLCR1	R/W	----XXXXB
001A63H				
001A64H	DLC register 2	DLCR2	R/W	----XXXXB
001A65H				
001A66H	DLC register 3	DLCR3	R/W	----XXXXB
001A67H				
001A68H	DLC register 4	DLCR4	R/W	----XXXXB
001A69H				
001A6AH	DLC register 5	DLCR5	R/W	----XXXXB
001A6BH				
001A6CH	DLC register 6	DLCR6	R/W	----XXXXB
001A6DH				
001A6EH	DLC register 7	DLCR7	R/W	----XXXXB
001A6FH				
001A70H	DLC register 8	DLCR8	R/W	----XXXX
001A71H				
001A72H	DLC register 9	DLCR9	R/W	----XXXXB
001A73H				
001A74H	DLC register 10	DLCR10	R/W	----XXXXB
001A75H				
001A76H	DLC register 11	DLCR11	R/W	----XXXXB
001A77H				
001A78H	DLC register 12	DLCR12	R/W	----XXXXB
001A79H				
001A7AH	DLC register 13	DLCR13	R/W	----XXXXB
001A7BH				
001A7CH	DLC register 14	DLCR14	R/W	----XXXXB
001A7DH				
001A7EH	DLC register 15	DLCR15	R/W	----XXXXB
001A7FH				
001A80H to 001A87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Initial Value
001A88H to 001A8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
001A90H to 001A97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
001A98H to 001A9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
001AA0H to 001AA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
001AA8H to 001AAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
001AB0H to 001AB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
001AB8H to 001ABFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
001AC0H to 001AC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
001AC8H to 001ACFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
001AD0H to 001AD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
001AD8H to 001ADFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
001AE0H to 001AE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
001AE8H to 001AEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
001AF0H to 001AF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
001AF8H to 001AFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

Interrupt source	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	# 08	FFFFDC$_H$	——	——
INT9 instruction	N/A	# 09	FFFFD8$_H$	——	——
Exception	N/A	# 10	FFFFD4$_H$	——	——
CAN RX	N/A	# 11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN TX/NS	N/A	# 12	FFFFCC$_H$		
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8$_H$	ICR01	0000B1$_H$
Time Base Timer	N/A	# 14	FFFFC4$_H$		
16-bit Reload Timer 0	*1	# 15	FFFFC0$_H$	ICR02	0000B2$_H$
8/10-bit A/D Converter	*1	# 16	FFFFBC$_H$		
16-bit Free-run Timer	N/A	# 17	FFFFB8$_H$	ICR03	0000B3$_H$
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4$_H$		
Serial I/O	*1	# 19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt (INT4/INT5)	*1	# 20	FFFFAC$_H$		
Input Capture 0	*1	# 21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	# 22	FFFFA4$_H$		
Output Compare 0	*1	# 23	FFFFA0$_H$	ICR06	0000B6$_H$
8/16-bit PPG 2/3	N/A	# 24	FFFF9C$_H$		
External Interrupt (INT6/INT7)	*1	# 25	FFFF98$_H$	ICR07	0000B7$_H$
Input Capture 1	*1	# 26	FFFF94$_H$		
8/16-bit PPG 4/5	N/A	# 27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 1	*1	# 28	FFFF8C$_H$		
8/16-bit PPG 6/7	N/A	# 29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2	*1	# 30	FFFF84$_H$		
8/16-bit PPG 8/9	N/A	# 31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 2	*1	# 32	FFFF7C$_H$		
Input Capture 3	*1	# 33	FFFF78$_H$	ICR11	0000BB$_H$
8/16-bit PPG A/B	N/A	# 34	FFFF74$_H$		
Output Compare 3	*1	# 35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	# 36	FFFF6C$_H$		
UART 0 RX	*2	# 37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	# 38	FFFF64$_H$		
UART 1 RX	*2	# 39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	# 40	FFFF5C$_H$		
Flash Memory	N/A	# 41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	# 42	FFFF54$_H$		

*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A:The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

11.2 Recommended Conditions

(V_{SS} = AV_{SS} = 0.0 V)

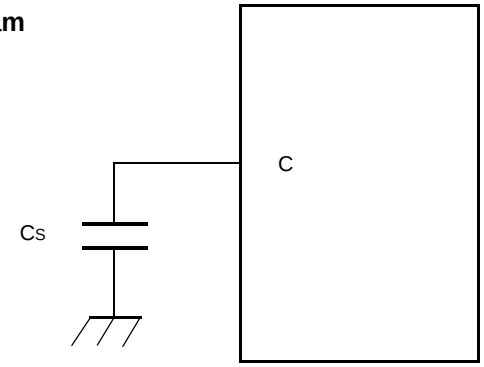
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC} AV_{CC}	4.5	5.0	5.5	V	Under normal operation
		3.0	—	5.5	V	Maintains RAM data in stop mode
Smooth capacitor	C_S	0.022	0.1	1.0	µF	*
Operating temperature	T_A	–40	—	+85	°C	

*: Use a ceramic capacitor or a capacitor with equivalent frequency characteristics. The smoothing capacitor to be connected to the V_{CC} pin must have a capacitance value higher than C_S.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

- **C Pin Connection Diagram**



11.3 DC Characteristics

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input H voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} +0.3	V	
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} +0.3	V	
Input L voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} +0.3	V	
Output H voltage	V_{OH1}	Output pins except P70 to P87	V_{CC} = 4.5 V, I_{OH1} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P70 to P87	V_{CC} = 4.5 V, I_{OH2} = –30.0 mA	V_{CC} – 0.5	—	—	V	
Output L voltage	V_{OL1}	Output pins except P70 to P87	V_{CC} = 4.5 V, I_{OL1} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P70 to P87	V_{CC} = 4.5 V, I_{OL2} = 30.0 mA	—	—	0.5	V	

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics

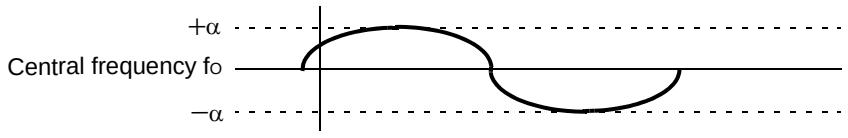
11.4.1 Clock Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

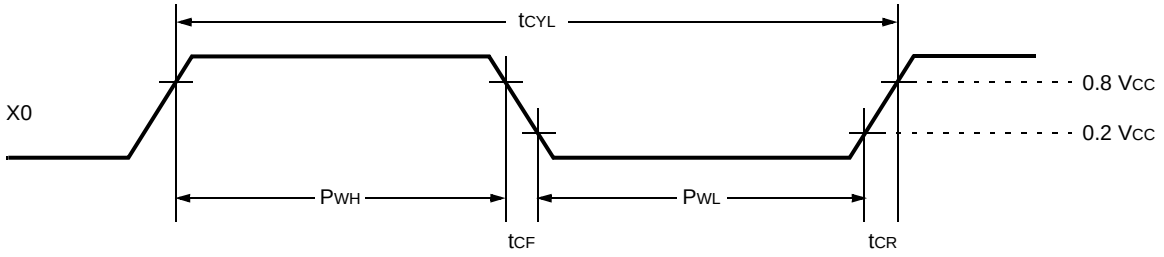
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	5	MHz	When using oscillation circuit
Oscillation cycle time	t_{CYL}	X0, X1	200	—	333	ns	When using oscillation circuit
External clock frequency	f_C	X0, X1	3	—	16	MHz	When using external clock
External clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using external clock
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash Read cycle time	t_{CYL}	—	—	2*t_{CP}	—	ns	When Flash is accessed via CPU

*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

$$\Delta f = \frac{|\alpha|}{fo} \times 100\%$$



- **Clock Timing**

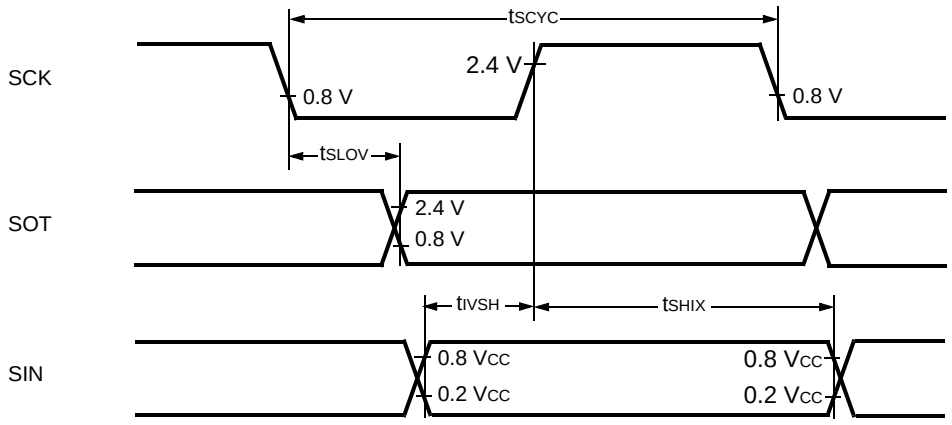


Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

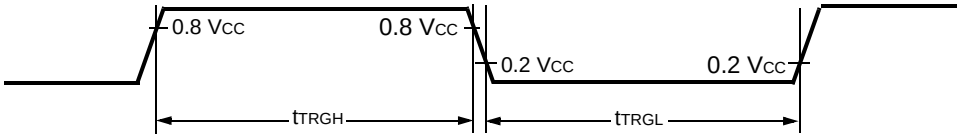
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{cp} (external operation clock cycle time) : see Clock timing.

- **Internal Shift Clock Mode**



- **Trigger Input Timing**



11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	150	ns	

- Slew Rate Output Timing

$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

11.5 A/D Converter

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V,3.0 V ≤ AVRH − AVRL, T_A = −40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	V	
Conversion time	—	—	—	352t_{CP}	—	ns	
Sampling time	—	—	—	64t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	−10	—	10	µA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	

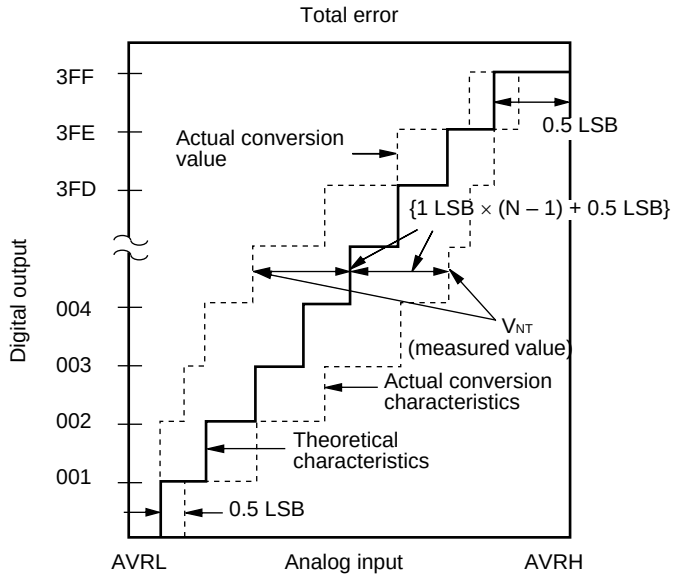
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)