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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

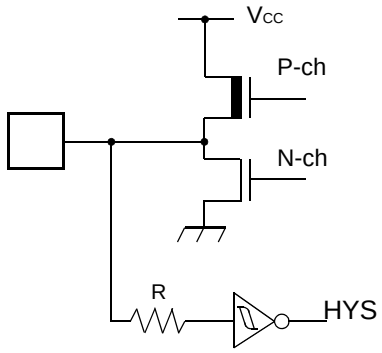
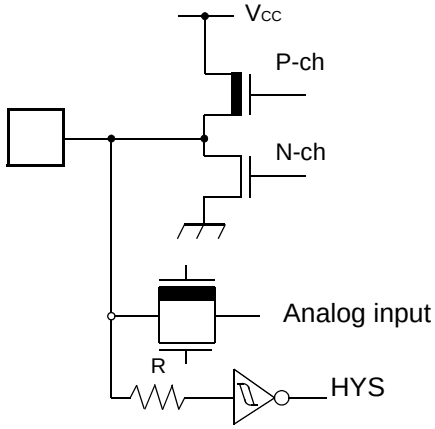
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-152

Features	MB90598G	MB90F598G	MB90V595G
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90598G/F598G:TSEG2 ≥ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics, Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*2	+5 V±10 %		
Package	QFP-100		PGA-256

*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2: Varies with conditions such as the operating frequency. (See "Electrical Characteristics.")

Circuit Type	Circuit	Remarks
D		■ CMOS output ■ CMOS Hysteresis input
E		■ CMOS output ■ CMOS Hysteresis input ■ Analog input

(Continued)

5. Handling Devices

(1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS}.

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC}, AVRH, DV_{CC}) and analog input voltages not exceed the digital voltage (V_{CC}).

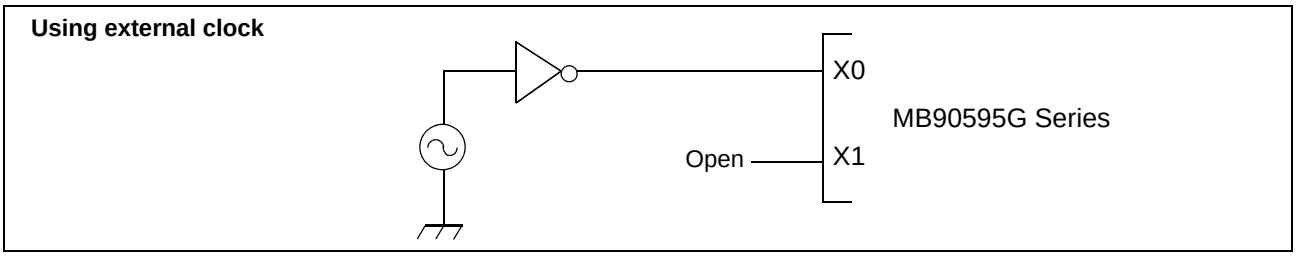
(2) Treatment of Unused Pins

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

(3) Using external clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

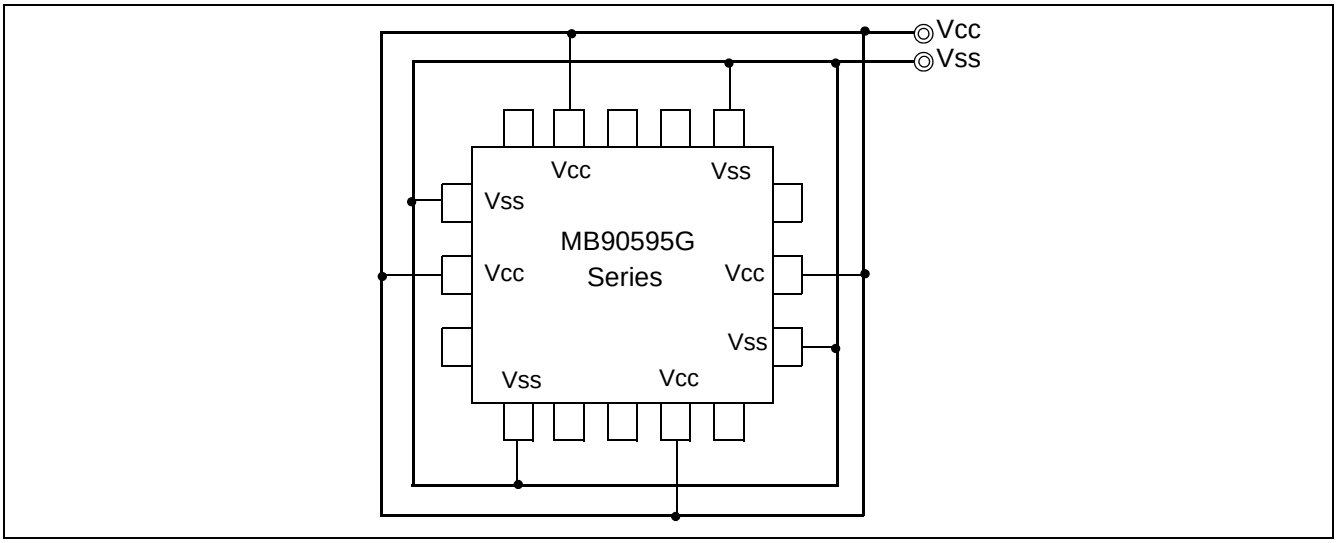


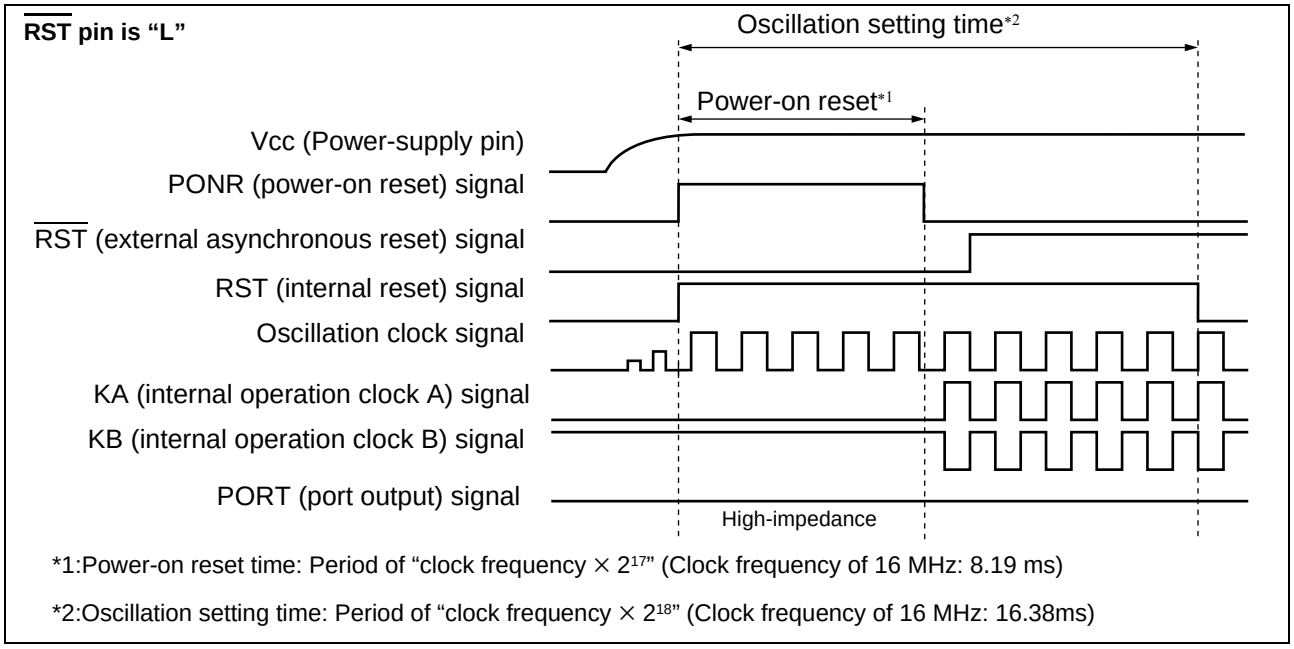
(4) Power supply pins (Vcc/Vss)

In products with multiple V_{cc} or V_{ss} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)

Make sure to connect V_{cc} and V_{ss} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{cc} and V_{ss} pins near the device.





*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)

(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions

In the signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “00_H”.

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than “00_H”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

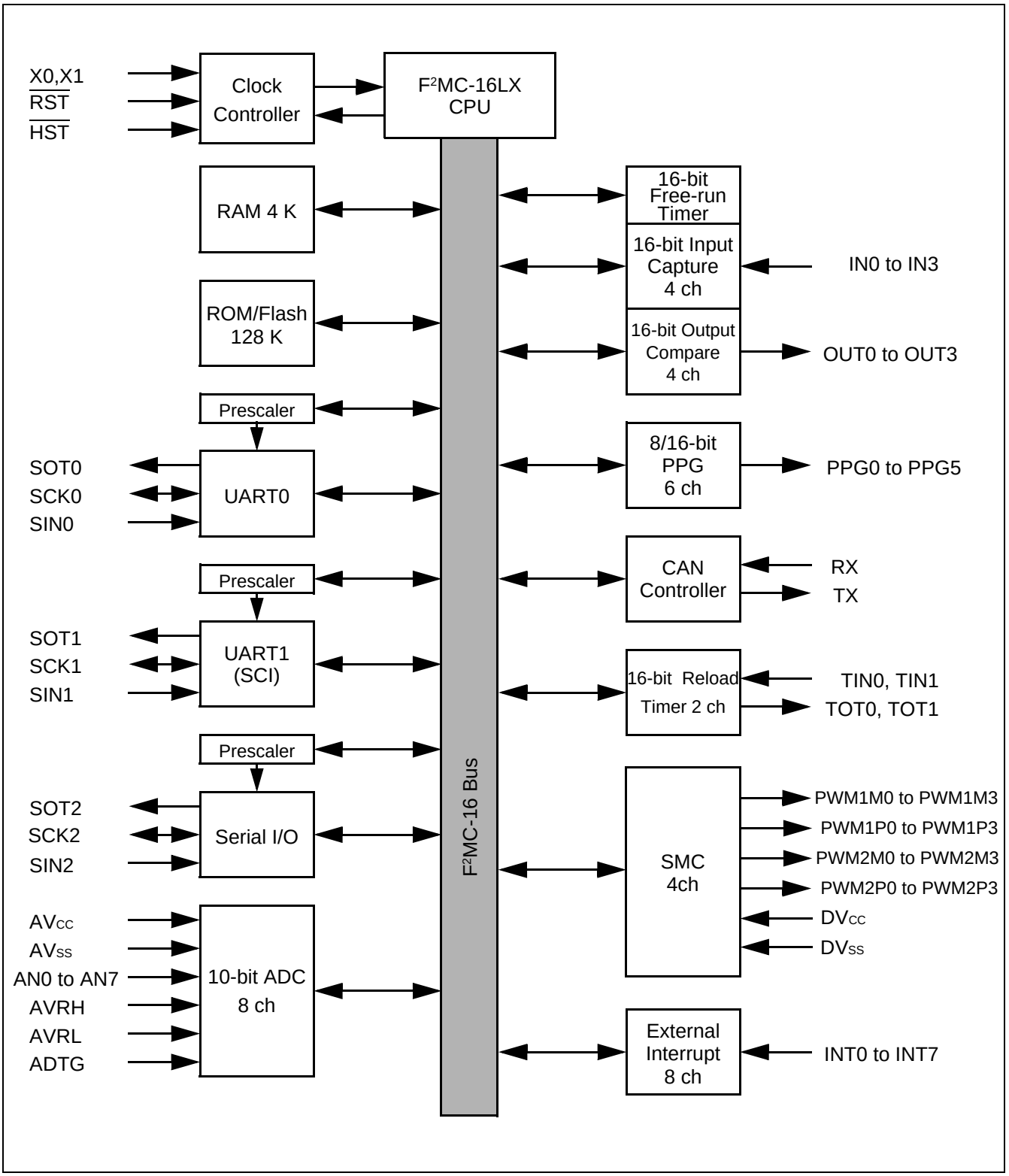
(14) Using REALOS

The use of EI^2OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

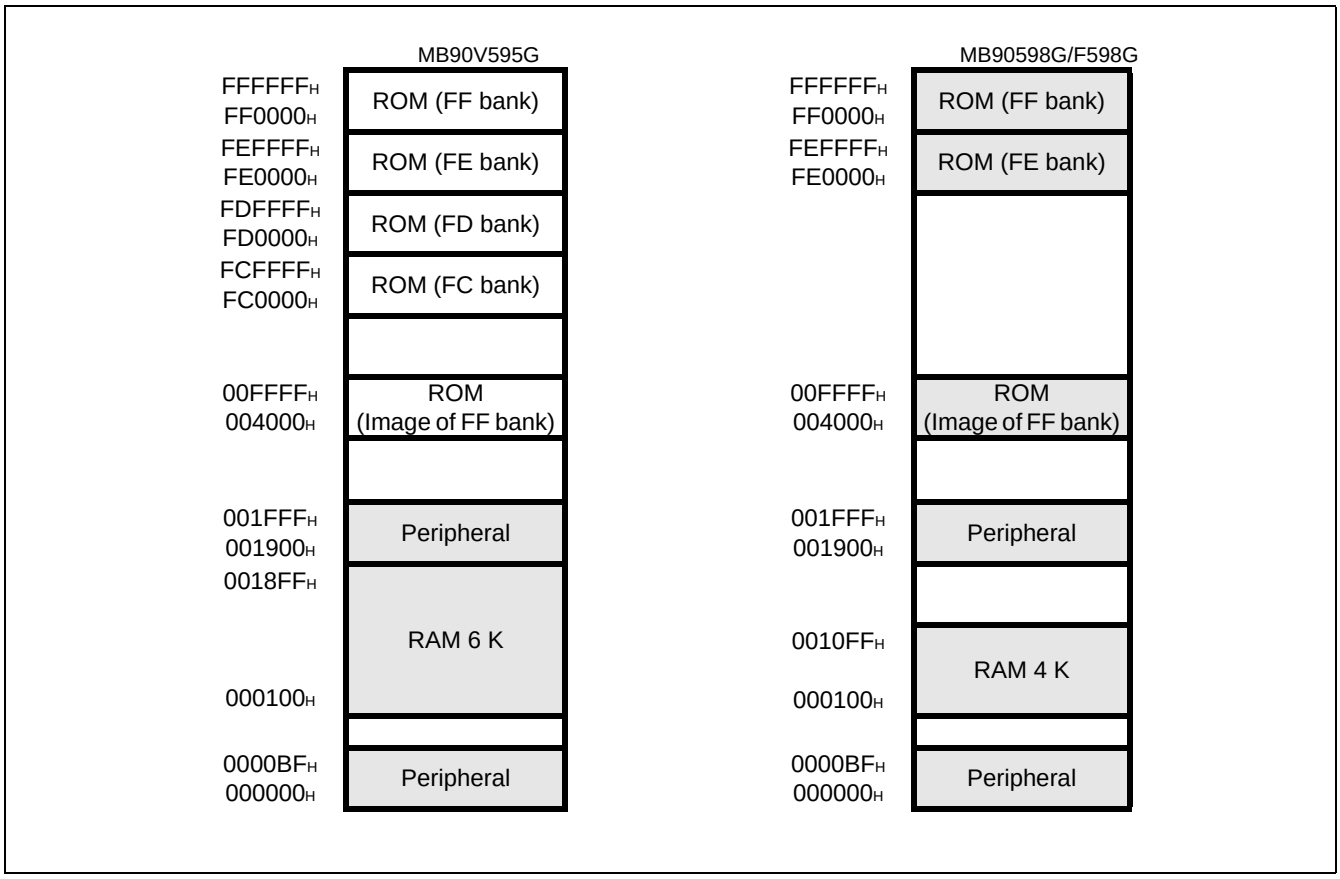
6. Block Diagram



7. Memory Space

The memory space of the MB90595G Series is shown below

Figure 1. Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access 00C000H , the contents of the ROM at FFC000H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H	Port 7 Data Register	PDR7	R/W	Port 7	$XXXXXXXX_B$
08_H	Port 8 Data Register	PDR8	R/W	Port 8	$XXXXXXXX_B$
09_H	Port 9 Data Register	PDR9	R/W	Port 9	$\_\_XXXXXX_B$
$0A_H$ to $0F_H$	Reserved				
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000_B
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000_B
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000_B
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
17_H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000_B
18_H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000_B
19_H	Port 9 Direction Register	DDR9	R/W	Port 9	$\_\_000000_B$
$1A_H$	Reserved				
$1B_H$	Analog Input Enable Register	ADER	R/W	Port 6, A/D	11111111_B
$1C_H$ to $1F_H$	Reserved				
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	00000100_B
21_H	Serial status Register 0	USR0	R/W		00010000_B
22_H	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W		$XXXXXXXX_B$
23_H	Rate and Data Register 0	URD0	R/W		$0000000X_B$
24_H	Serial Mode Register 1	SMR1	R/W	UART1	00000000_B
25_H	Serial Control Register 1	SCR1	R/W		00000100_B
26_H	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W		$XXXXXXXX_B$
27_H	Serial Status Register 1	SSR1	R/W		0001_00_B
28_H	UART1 Prescaler Control Register	U1CDCR	R/W		$0\_\_\_1111_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
4C$_H$	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit Programmable Pulse Generator A/B	0 _ 0 0 0 _ _ 1$_B$
4D$_H$	PPGB Operation Mode Control Register	PPGCB	R/W		0 _ 0 0 0 0 0 1$_B$
4E$_H$	PPGA, B Output Pin Control Register	PPGAB	R/W		0 0 0 0 0 0 _ _$_B$
4F$_H$	Reserved				
50$_H$	Timer Control Status Register 0	TMCSR0	R/W	16-bit Reload Timer 0	0 0 0 0 0 0 0 0$_B$
51$_H$	Timer Control Status Register 0	TMCSR0	R/W		_ _ _ _ 0 0 0 0$_B$
52$_H$	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W		XXXXXXXX$_B$
53$_H$	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W		XXXXXXXX$_B$
54$_H$	Timer Control Status Register 1	TMCSR1	R/W	16-bit Reload Timer 1	0 0 0 0 0 0 0 0$_B$
55$_H$	Timer Control Status Register 1	TMCSR1	R/W		_ _ _ _ 0 0 0 0$_B$
56$_H$	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W		XXXXXXXX$_B$
57$_H$	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W		XXXXXXXX$_B$
58$_H$	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 _ _ 0 0$_B$
59$_H$	Output Compare Control Status Register 1	OCS1	R/W		_ _ _ 0 0 0 0 0$_B$
5A$_H$	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 _ _ 0 0$_B$
5B$_H$	Output Compare Control Status Register 3	OCS3	R/W		_ _ _ 0 0 0 0 0$_B$
5C$_H$	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0$_B$
5D$_H$	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0$_B$
5E$_H$	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	0 0 0 0 0 _ _ 0$_B$
5F$_H$	Reserved				
60$_H$	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	0 0 0 0 0 _ _ 0$_B$
61$_H$	Reserved				
62$_H$	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	0 0 0 0 0 _ _ 0$_B$
63$_H$	Reserved				
64$_H$	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	0 0 0 0 0 _ _ 0$_B$
65$_H$	Reserved				
66$_H$	Timer Data Register (low-order)	TCDT	R/W	16-bit Free-run Timer	0 0 0 0 0 0 0 0$_B$
67$_H$	Timer Data Register (high-order)	TCDT	R/W		0 0 0 0 0 0 0 0$_B$
68$_H$	Timer Control Status Register	TCCS	R/W		0 0 0 0 0 0 0 0$_B$
69$_H$ to 6E$_H$	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
001B08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
001B09H				
001B0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
001B0BH				
001B0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
001B0DH				
001B0EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000B
001B0FH				
001B10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
001B11H				
001B12H				XXXXXXXX XXXXXXXXB
001B13H				
001B14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
001B15H				
001B16H				XXXXX--- XXXXXXXXB
001B17H				
001B18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
001B19H				
001B1AH				XXXXX--- XXXXXXXXB
001B1BH				

9.2 List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
001A00H to 001A1FH	General-purpose RAM	--	R/W	XXXXXXXXB to XXXXXXXXB
001A20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
001A21H				
001A22H				XXXXX--- XXXXXXXXB
001A23H				
001A24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
001A25H				
001A26H				XXXXX--- XXXXXXXXB
001A27H				
001A28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
001A29H				
001A2AH				XXXXX--- XXXXXXXXB
001A2BH				

Address	Register	Abbreviation	Access	Initial Value
001A2C$_H$	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX$_B$
001A2D$_H$				
001A2E$_H$				XXXXX--- XXXXXXXX$_B$
001A2F$_H$				
001A30$_H$	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX$_B$
001A31$_H$				
001A32$_H$				XXXXX--- XXXXXXXX$_B$
001A33$_H$				
001A34$_H$	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX$_B$
001A35$_H$				
001A36$_H$				XXXXX--- XXXXXXXX$_B$
001A37$_H$				
001A38$_H$	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX$_B$
001A39$_H$				
001A3A$_H$				XXXXX--- XXXXXXXX$_B$
001A3B$_H$				
001A3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
001A3D$_H$				
001A3E$_H$				XXXXX--- XXXXXXXX$_B$
001A3F$_H$				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
001A88H to 001A8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
001A90H to 001A97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
001A98H to 001A9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
001AA0H to 001AA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
001AA8H to 001AAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
001AB0H to 001AB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
001AB8H to 001ABFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
001AC0H to 001AC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
001AC8H to 001ACFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
001AD0H to 001AD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
001AD8H to 001ADFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
001AE0H to 001AE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
001AE8H to 001AEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
001AF0H to 001AF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
001AF8H to 001AFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} − 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/L, AVRH ≥ AVRL *1
	DV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} ≥ DV_{CC}
Input voltage	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Maximum Clamp Current	I_{CLAMP}	−2.0	2.0	mA	*6
Maximum Total Clamp Current	$\sum \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level Max. output current	I_{OL1}	—	15	mA	Normal output *3
“L” level Avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
“L” level Max. output current	I_{OL2}	—	40	mA	High current output *3
“L” level Avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
“L” level Max. overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
“L” level Max. overall output current	$\sum I_{OL2}$	—	330	mA	Total high current output
“L” level Avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
“L” level Avg. overall output current	$\sum I_{OLAV2}$	—	250	mA	Total high current output, average value *5
“H” level Max. output current	I_{OH1}	—	−15	mA	Normal output *3
“H” level Avg. output current	I_{OHAV1}	—	−4	mA	Normal output, average value *4
“H” level Max. output current	I_{OH2}	—	−40	mA	High current output *3
“H” level Avg. output current	I_{OHAV2}	—	−30	mA	High current output, average value *4
“H” level Max. overall output current	$\sum I_{OH1}$	—	−100	mA	Total normal output
“H” level Max. overall output current	$\sum I_{OH2}$	—	−330	mA	Total high current output
“H” level Avg. overall output current	$\sum I_{OHAV1}$	—	−50	mA	Total normal output, average value *5
“H” level Avg. overall output current	$\sum I_{OHAV2}$	—	−250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F598G
		—	400	mW	MB90598G
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1: AV_{CC}, AVRH, AVRL and DV_{CC} shall not exceed V_{CC}. AVRH and AVRL shall not exceed AV_{CC}. Also, AVRL shall never exceed AVRH.

*2: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

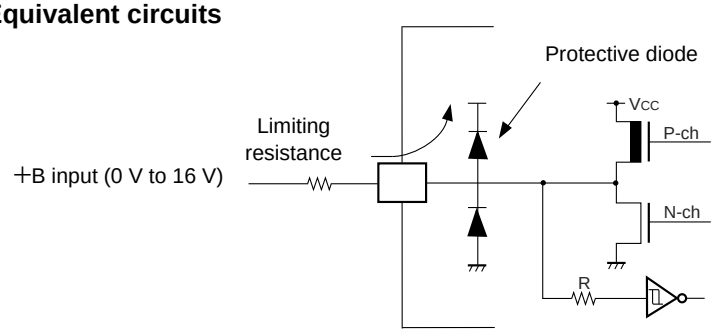
*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6:

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

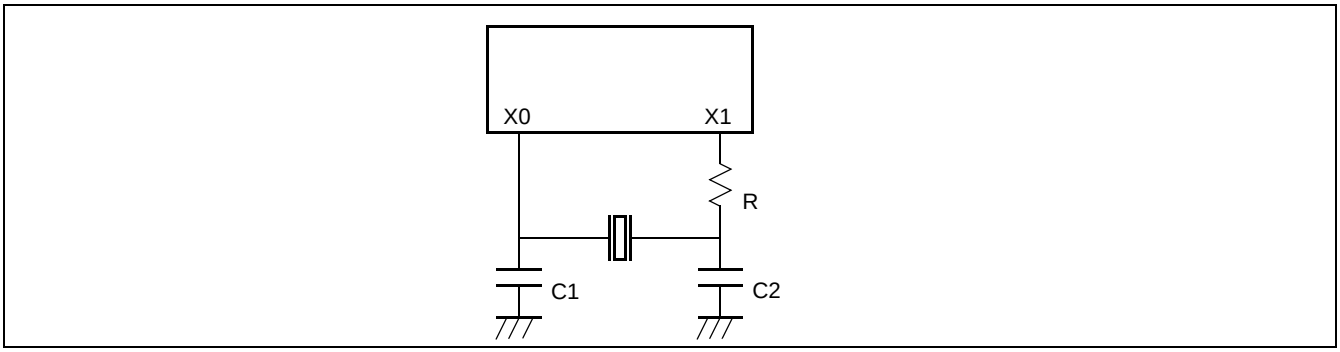
• Input/Output Equivalent circuits



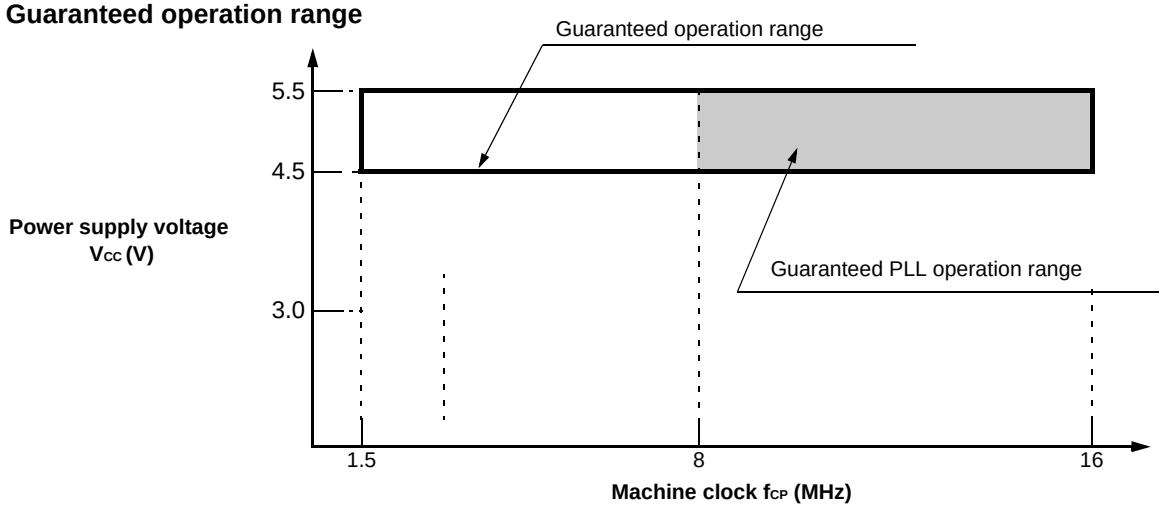
Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

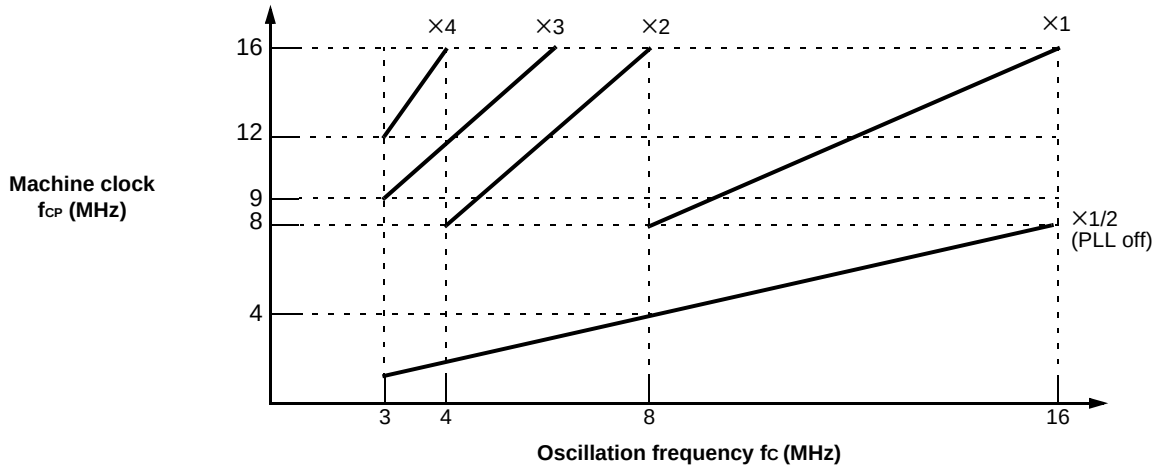
■ Example of Oscillation circuit



- **Guaranteed operation range**



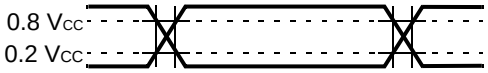
- **Oscillation frequency and machine clock frequency**



AC characteristics are set to the measured reference voltage values below.

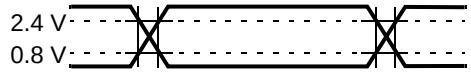
- **Input signal waveform**

Hysteresis Input Pin

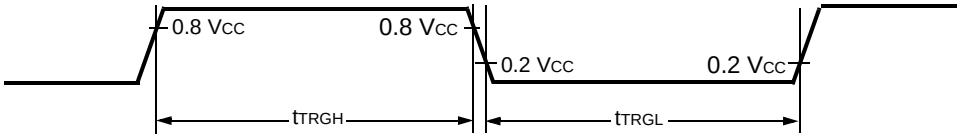


- **Output signal waveform**

Output Pin



- **Trigger Input Timing**



11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	150	ns	

- Slew Rate Output Timing

$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

11.5 A/D Converter

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V,3.0 V ≤ AVRH − AVRL, T_A = −40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	V	
Conversion time	—	—	—	352t_{CP}	—	ns	
Sampling time	—	—	—	64t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	−10	—	10	µA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	—	AVRH	AVRL + 3.0	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 3.0	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	400	600	µA	MB90V595G, MB90F598G
			—	140	600	µA	MB90598G
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

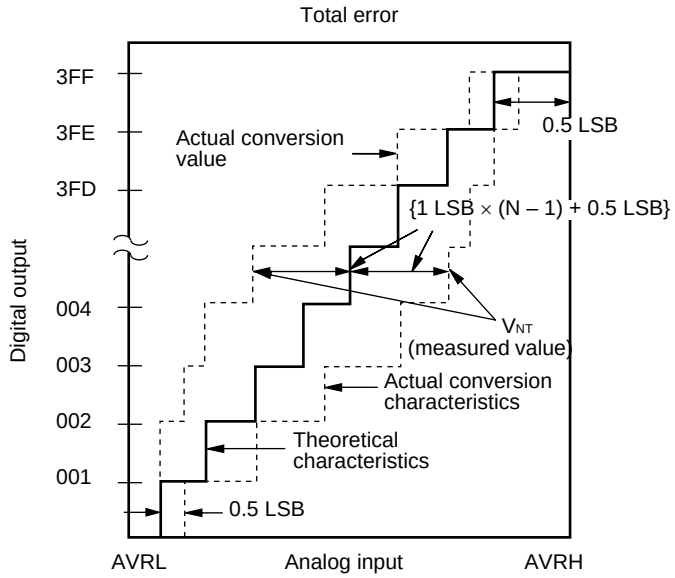
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)

11.8 Flash memory

■ Erase and programming performance

Parameter	Condition	Value			Unit	Remarks	
		Min	Typ	Max			
Sector erase time	$T_A = +25\ ^{\circ}C$, $V_{CC} = 5.0$ V	—	1	15	s	MB90F598G	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	MB90F598G	Excludes 00H programming prior
Word (16-bit) programming time		—	16	3600	µs	MB90F598G	Excludes system-level overhead
Erase/Program cycle	—	10000	—	—	cycle		

Supply Current