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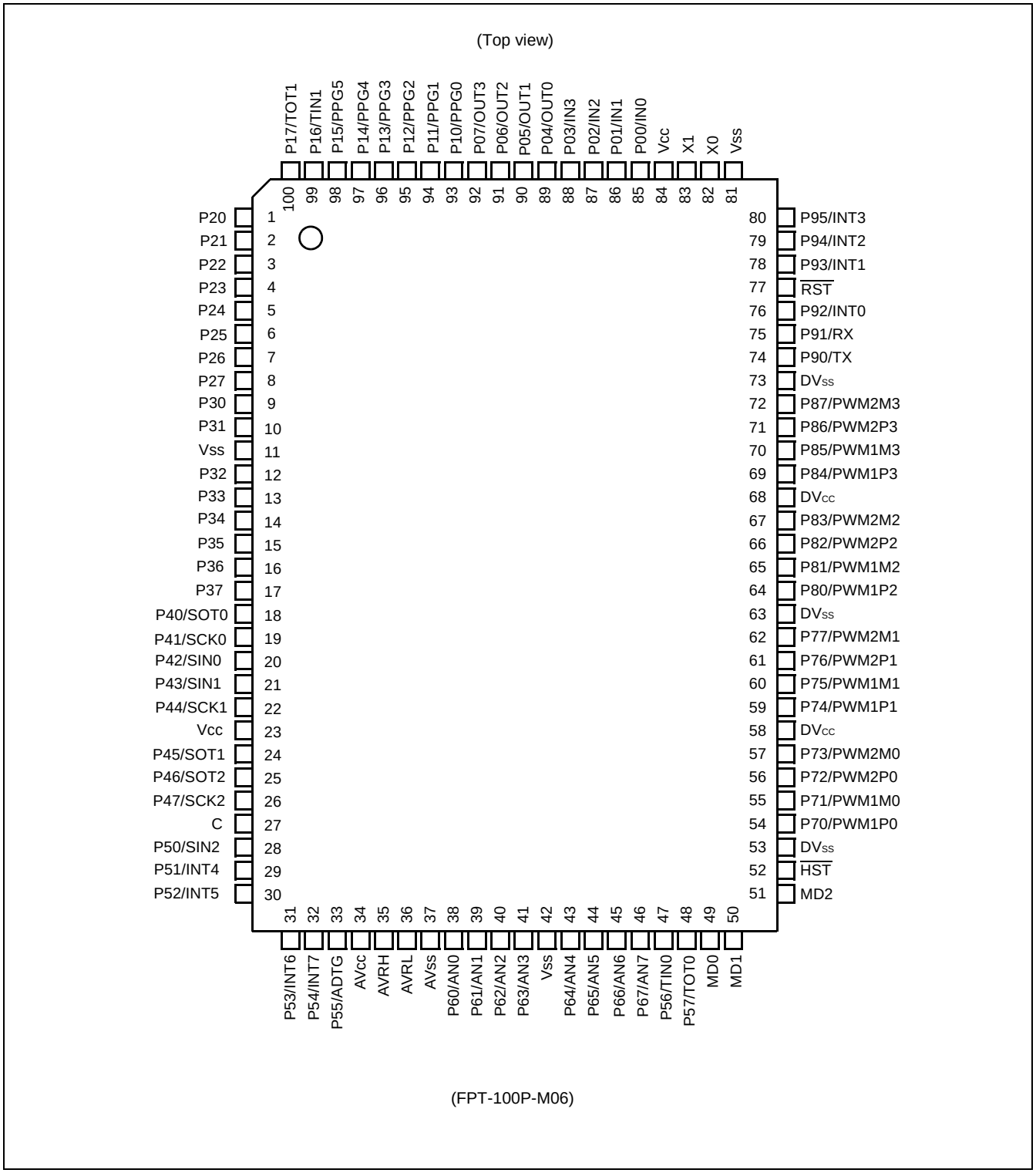
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-153

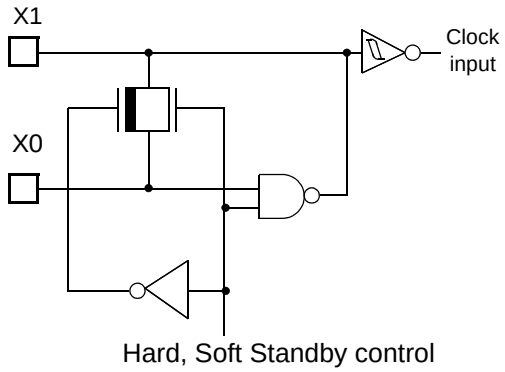
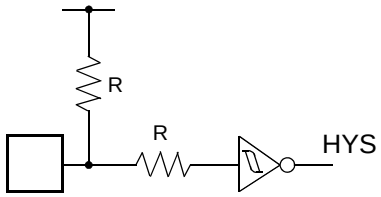
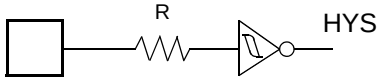
2. Pin Assignment

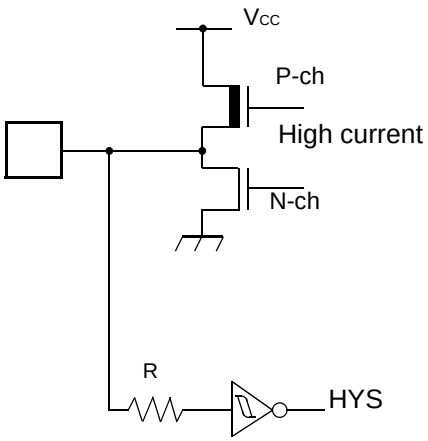
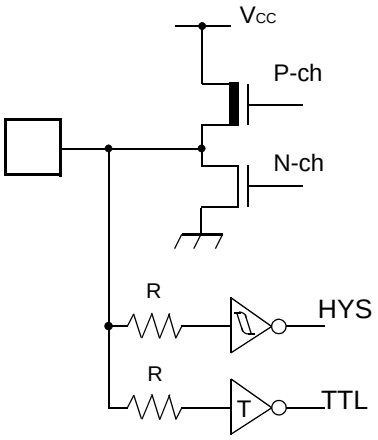
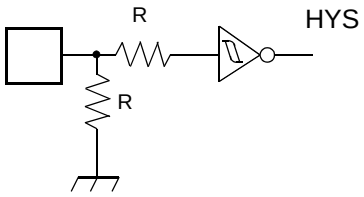


Pin no.	Pin name	Circuit type	Function
28	P50	D	General purpose IO
	SIN2		SIN Input for the Serial IO
29 to 32	P51 to P54	D	General purpose IO
	INT4 to INT7		External interrupt input for INT4 to INT7
33	P55	D	General purpose IO
	ADTG		Input for the external trigger of the A/D Converter
38 to 41	P60 to P63	E	General purpose IO
	AN0 to AN3		Inputs for the A/D Converter
43 to 46	P64 to P67	E	General purpose IO
	AN4 to AN7		Inputs for the A/D Converter
47	P56	D	General purpose IO
	TIN0		TIN input for the 16-bit Reload Timer 0
48	P57	D	General purpose IO
	TOT0		TOT output for the 16-bit Reload Timer 0
54 to 57	P70 to P73	F	General purpose IO
	PWM1P0 PWM1M0 PWM2P0 PWM2M0		Output for Stepper Motor Controller channel 0
59 to 62	P74 to P77	F	General purpose IO
	PWM1P1 PWM1M1 PWM2P1 PWM2M1		Output for Stepper Motor Controller channel 1
64 to 67	P80 to P83	F	General purpose IO
	PWM1P2 PWM1M2 PWM2P2 PWM2M2		Output for Stepper Motor Controller channel 2
69 to 72	P84 to P87	F	General purpose IO
	PWM1P3 PWM1M3 PWM2P3 PWM2M3		Output for Stepper Motor Controller channel 3
74	P90	D	General purpose IO
	TX		TX output for CAN Interface
75	P91	D	General purpose IO
	RX		RX input for CAN Interface

Pin no.	Pin name	Circuit type	Function
76	P92	D	General purpose IO
	INT0		External interrupt input for INT0
78 to 80	P93 to P95	D	General purpose IO
	INT1 to INT3		External interrupt input for INT1 to INT3
58, 68	DV_{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV_{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV_{CC}	Power supply	Dedicated power supply pin for the A/D Converter
37	AV_{SS}	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter
49, 50	MD0 MD1	C	Operating mode selection input pins. These pins should be connected to V_{CC} or V_{SS}.
51	MD2	H	Operating mode selection input pin. This pin should be connected to V_{CC} or V_{SS}.
27	C	—	External capacitor pin. A capacitor of 0.1μF should be connected to this pin and V_{SS}.
23, 84	V_{CC}	Power supply	Power supply pins (5.0 V).
11, 42, 81	V_{SS}	Power supply	Ground pins (0.0 V).

4. I/O Circuit Type

Circuit Type	Circuit	Remarks
A		■ Oscillation feedback resistor: 1 MΩ approx.
B		■ Hysteresis input with pull-up Resistor: 50 kΩ approx.
C		■ Hysteresis input

Circuit Type	Circuit	Remarks
F		■ CMOS high current output ■ CMOS Hysteresis input
G		■ CMOS output ■ CMOS Hysteresis input ■ TTL input (MB90F598G, only in Flash mode)
H		■ Hysteresis input Pull-down Resistor: 50 kΩ approx. (except MB90F598G)

5. Handling Devices

(1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).

In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS}.

When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.

In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC}, AVRH, DV_{CC}) and analog input voltages not exceed the digital voltage (V_{CC}).

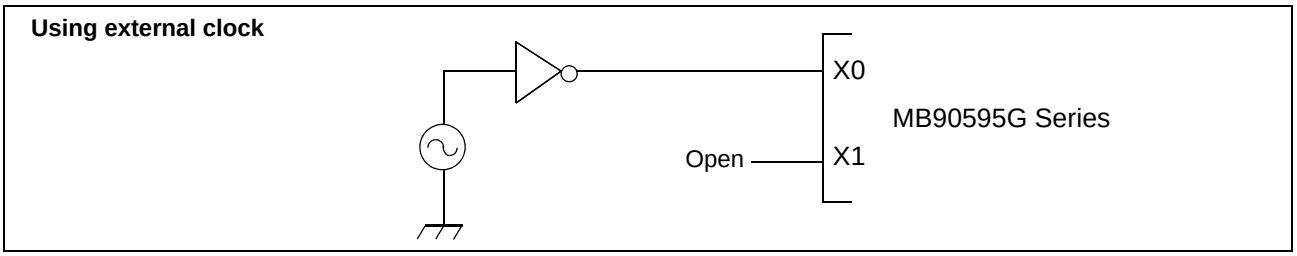
(2) Treatment of Unused Pins

Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.

Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

(3) Using external clock

In using the external clock, drive X0 pin only and leave X1 pin unconnected.

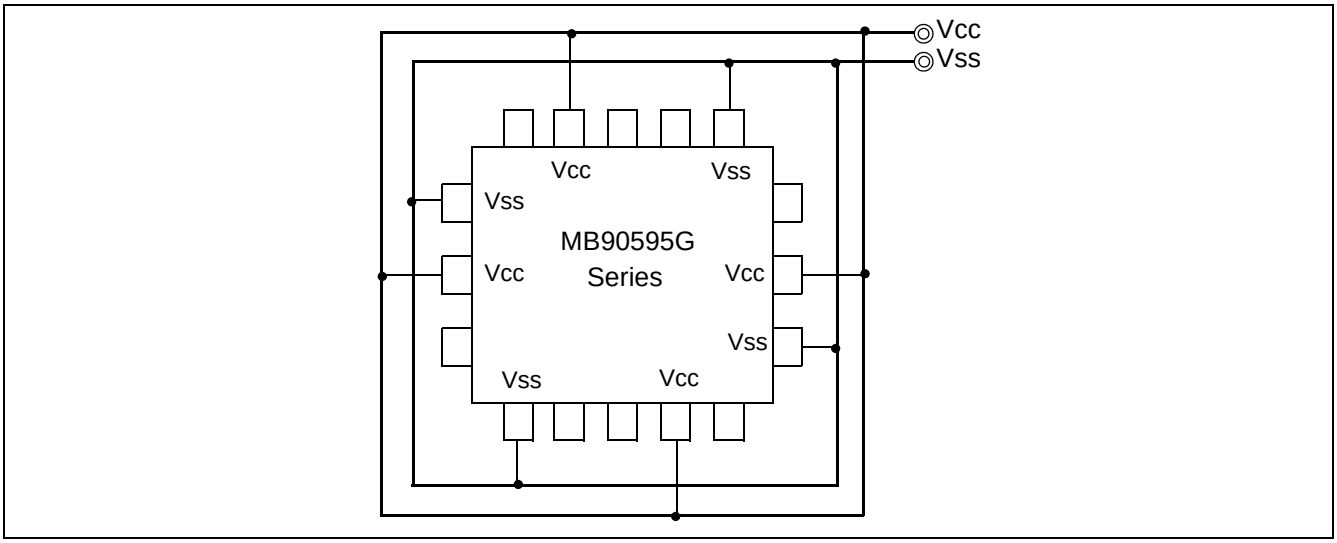


(4) Power supply pins (Vcc/Vss)

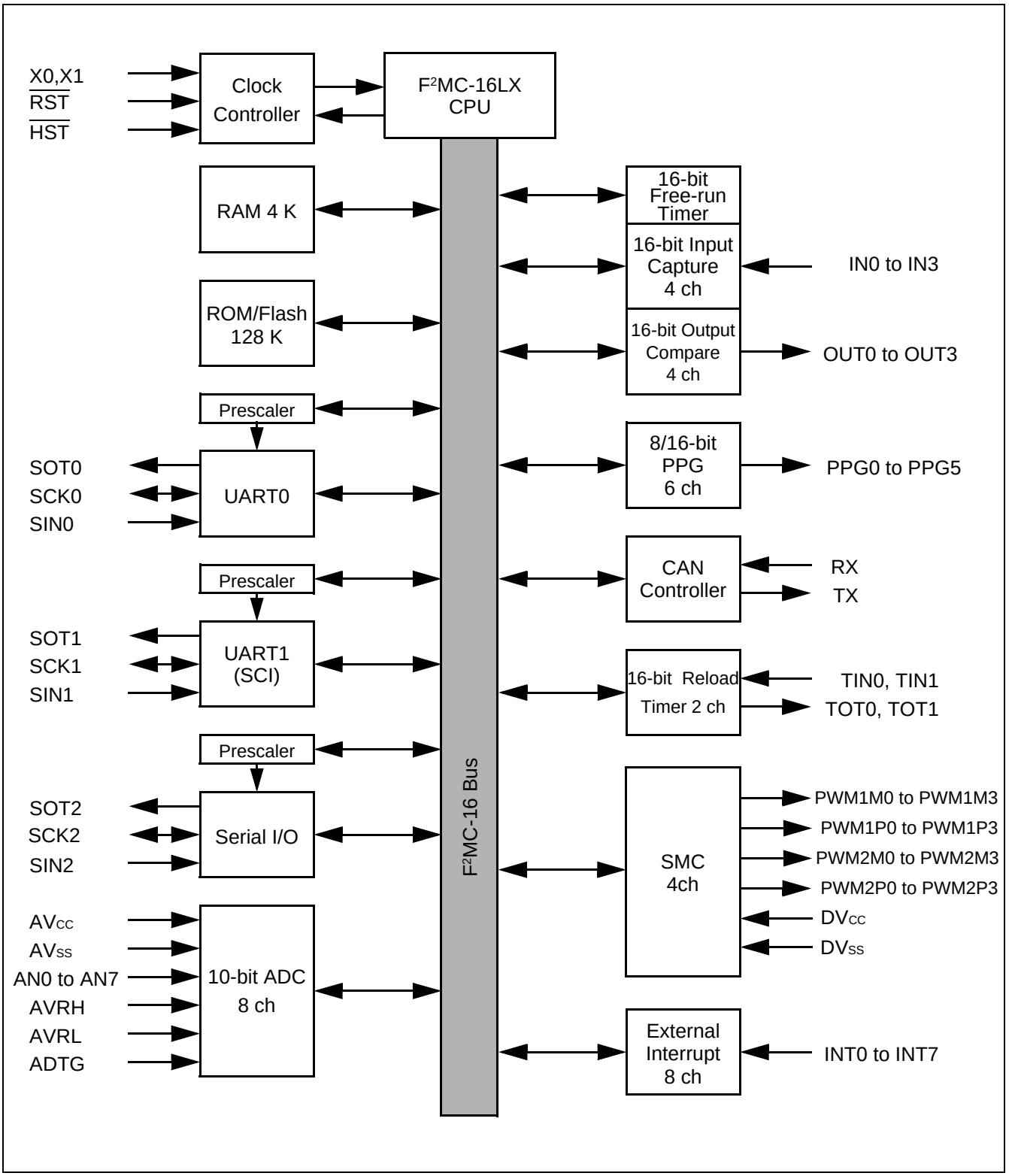
In products with multiple V_{cc} or V_{ss} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)

Make sure to connect V_{cc} and V_{ss} pins via lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between V_{cc} and V_{ss} pins near the device.



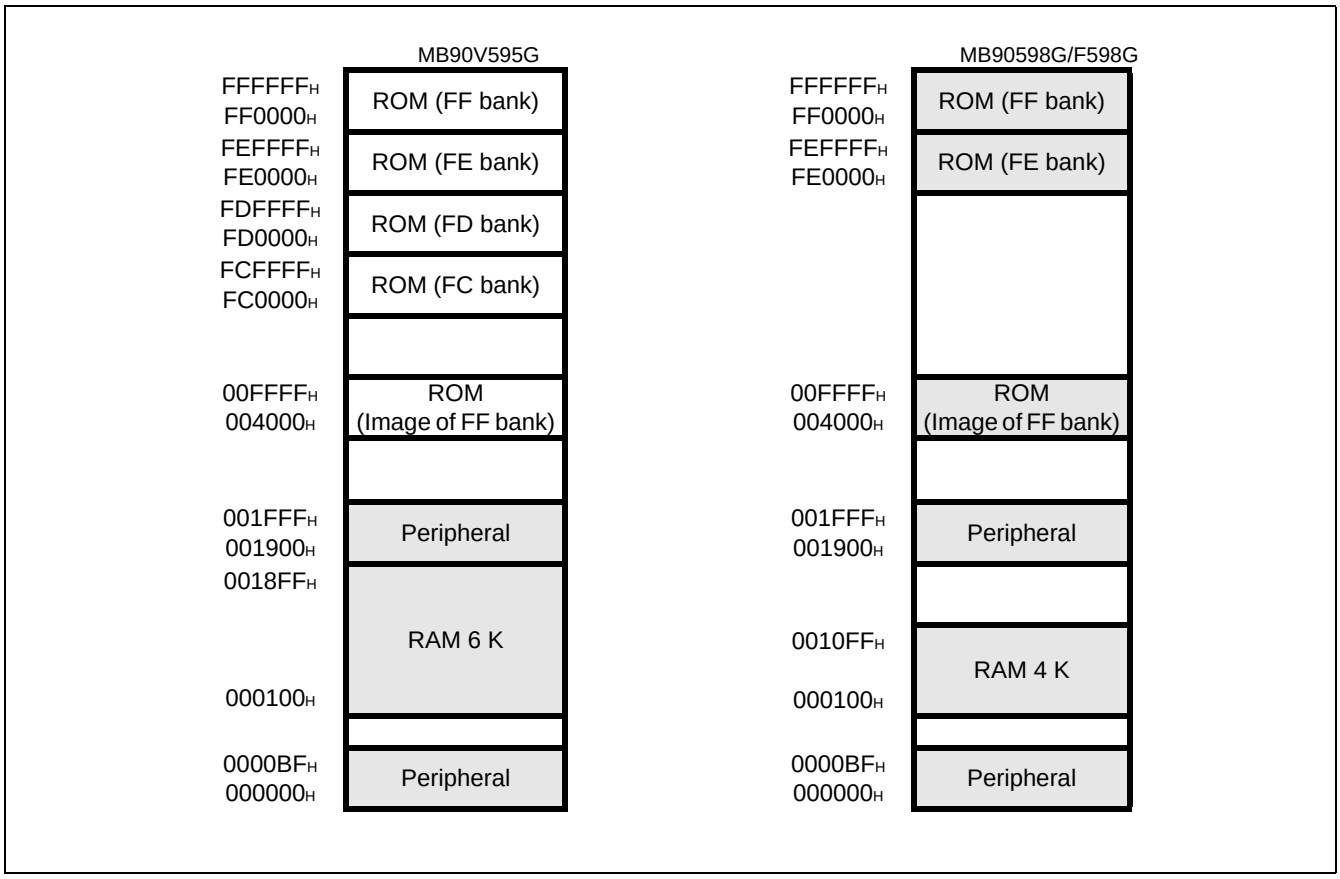
6. Block Diagram



7. Memory Space

The memory space of the MB90595G Series is shown below

Figure 1. Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access 00C000H , the contents of the ROM at FFC000H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H	Port 7 Data Register	PDR7	R/W	Port 7	$XXXXXXXX_B$
08_H	Port 8 Data Register	PDR8	R/W	Port 8	$XXXXXXXX_B$
09_H	Port 9 Data Register	PDR9	R/W	Port 9	$\_\_XXXXXX_B$
$0A_H$ to $0F_H$	Reserved				
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000_B
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000_B
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000_B
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
17_H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000_B
18_H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000_B
19_H	Port 9 Direction Register	DDR9	R/W	Port 9	$\_\_000000_B$
$1A_H$	Reserved				
$1B_H$	Analog Input Enable Register	ADER	R/W	Port 6, A/D	11111111_B
$1C_H$ to $1F_H$	Reserved				
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	00000100_B
21_H	Serial status Register 0	USR0	R/W		00010000_B
22_H	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W		$XXXXXXXX_B$
23_H	Rate and Data Register 0	URD0	R/W		$0000000X_B$
24_H	Serial Mode Register 1	SMR1	R/W	UART1	00000000_B
25_H	Serial Control Register 1	SCR1	R/W		00000100_B
26_H	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W		$XXXXXXXX_B$
27_H	Serial Status Register 1	SSR1	R/W		0001_00_B
28_H	UART1 Prescaler Control Register	U1CDCR	R/W		$0\_\_\_1111_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
29H to 2AH	Reserved				
2BH	Serial IO Prescaler	SCDCR	R/W	Serial IO	0 _ _ _ 1 1 1 1B
2CH	Serial Mode Control Register (low-order)	SMCS	R/W		_ _ _ _ 0 0 0 0B
2DH	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial Data Register	SDR	R/W		XXXXXXXXB
2FH	Edge Selector	SES	R/W		_ _ _ _ _ _ _ 0B
30H	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External Interrupt Request Register	EIRR	R/W		XXXXXXXXB
32H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D Data Register 0	ADCR0	R		XXXXXXXXB
37H	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0, 1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Reserved				
3CH	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1B
3DH	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2, 3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Reserved				
40H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4, 5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Reserved				
44H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6, 7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 _ _B
47H	Reserved				
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1B
4AH	PPG8, 9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 _ _B
4BH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
6F$_H$	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1$_B$
70$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
71$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
72$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0$_B$
73$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0$_B$
74$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
75$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
76$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0$_B$
77$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0$_B$
78$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
79$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
7A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0$_B$
7B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0$_B$
7C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
7D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
7E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0$_B$
7F$_H$	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 0$_B$
80$_H$ to 8F$_H$	CAN Controller. Refer to section about CAN Controller				
90$_H$ to 9D$_H$	Reserved				
9E$_H$	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0$_B$
9F$_H$	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0$_B$
A0$_H$	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0$_B$
A1$_H$	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0$_B$
A2$_H$ to A7$_H$	Reserved				
A8$_H$	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1$_B$
A9$_H$	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 _ _ 0 0 1 0 0$_B$
AA$_H$ to AD$_H$	Reserved				
AE$_H$	Flash Memory Control Status Register (MB90F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0$_B$
AF$_H$	Reserved				

(Continued)

9. Can Controller

The CAN controller has the following features:

- Conforms to CAN Specification Version 2.0 Part A and B
  - - Supports transmission/reception in standard frame and extended frame formats
- Supports transmission of data frames by receiving remote frames
- 16 transmitting/receiving message buffers
  - 29-bit ID and 8-byte data
  - Multi-level message buffer configuration
- Provides full-bit comparison, full-bit mask, acceptance register 0/acceptance register 1 for each message buffer as ID acceptance mask
  - Two acceptance mask registers in either standard frame format or extended frame format
- Bit rate programmable from 10 kbps to 2 Mbps (when input clock is at 16 MHz)

9.1 List of Control Registers

Address	Register	Abbreviation	Access	Initial Value
000080H	Message buffer valid register	BVALR	R/W	00000000 00000000B
000081H				
000082H	Transmit request register	TREQR	R/W	00000000 00000000B
000083H				
000084H	Transmit cancel register	TCANR	W	00000000 00000000B
000085H				
000086H	Transmit complete register	TCR	R/W	00000000 00000000B
000087H				
000088H	Receive complete register	RCR	R/W	00000000 00000000B
000089H				
00008AH	Remote request receiving register	RRTRR	R/W	00000000 00000000B
00008BH				
00008CH	Receive overrun register	ROVRR	R/W	00000000 00000000B
00008DH				
00008EH	Receive interrupt enable register	RIER	R/W	00000000 00000000B
00008FH				
001B00H	Control status register	CSR	R/W, R	00---000 0----0-1B
001B01H				
001B02H	Last event indicator register	LEIR	R/W	-------- 000-0000B
001B03H				
001B04H	Receive/transmit error counter	RTEC	R	00000000 00000000B
001B05H				
001B06H	Bit timing register	BTR	R/W	-1111111 11111111B
001B07H				

(Continued)

Address	Register	Abbreviation	Access	Initial Value
001A2C$_H$	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX$_B$
001A2D$_H$				
001A2E$_H$				XXXXX--- XXXXXXXX$_B$
001A2F$_H$				
001A30$_H$	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX$_B$
001A31$_H$				
001A32$_H$				XXXXX--- XXXXXXXX$_B$
001A33$_H$				
001A34$_H$	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX$_B$
001A35$_H$				
001A36$_H$				XXXXX--- XXXXXXXX$_B$
001A37$_H$				
001A38$_H$	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX$_B$
001A39$_H$				
001A3A$_H$				XXXXX--- XXXXXXXX$_B$
001A3B$_H$				
001A3C$_H$	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX$_B$
001A3D$_H$				
001A3E$_H$				XXXXX--- XXXXXXXX$_B$
001A3F$_H$				

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics

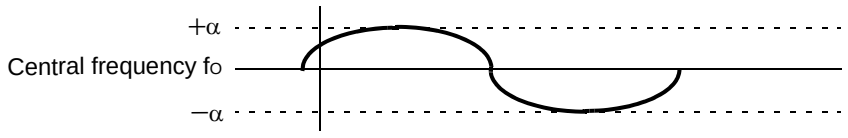
11.4.1 Clock Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

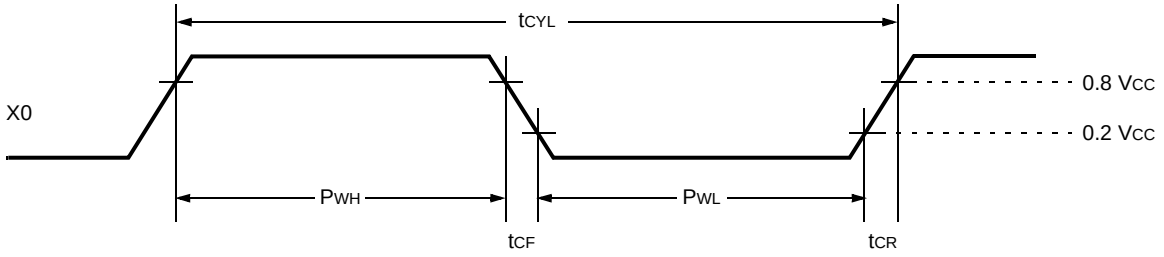
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	5	MHz	When using oscillation circuit
Oscillation cycle time	t_{CYL}	X0, X1	200	—	333	ns	When using oscillation circuit
External clock frequency	f_C	X0, X1	3	—	16	MHz	When using external clock
External clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using external clock
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash Read cycle time	t_{CYL}	—	—	2*t_{CP}	—	ns	When Flash is accessed via CPU

*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

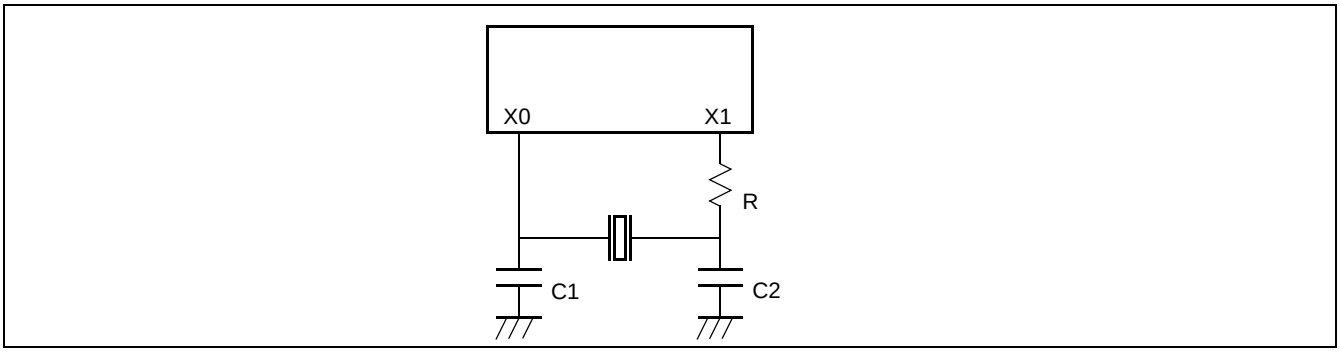
$$\Delta f = \frac{|\alpha|}{fo} \times 100\%$$



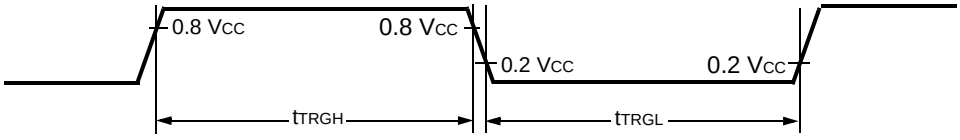
- **Clock Timing**



■ Example of Oscillation circuit



- **Trigger Input Timing**



11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	150	ns	

- Slew Rate Output Timing

$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

11.5 A/D Converter

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V,3.0 V ≤ AVRH − AVRL, T_A = −40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	V	
Conversion time	—	—	—	352t_{CP}	—	ns	
Sampling time	—	—	—	64t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	−10	—	10	µA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	

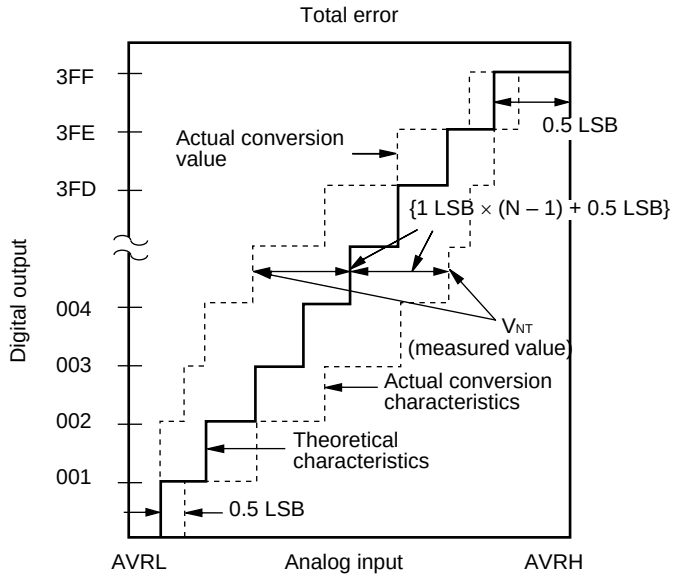
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

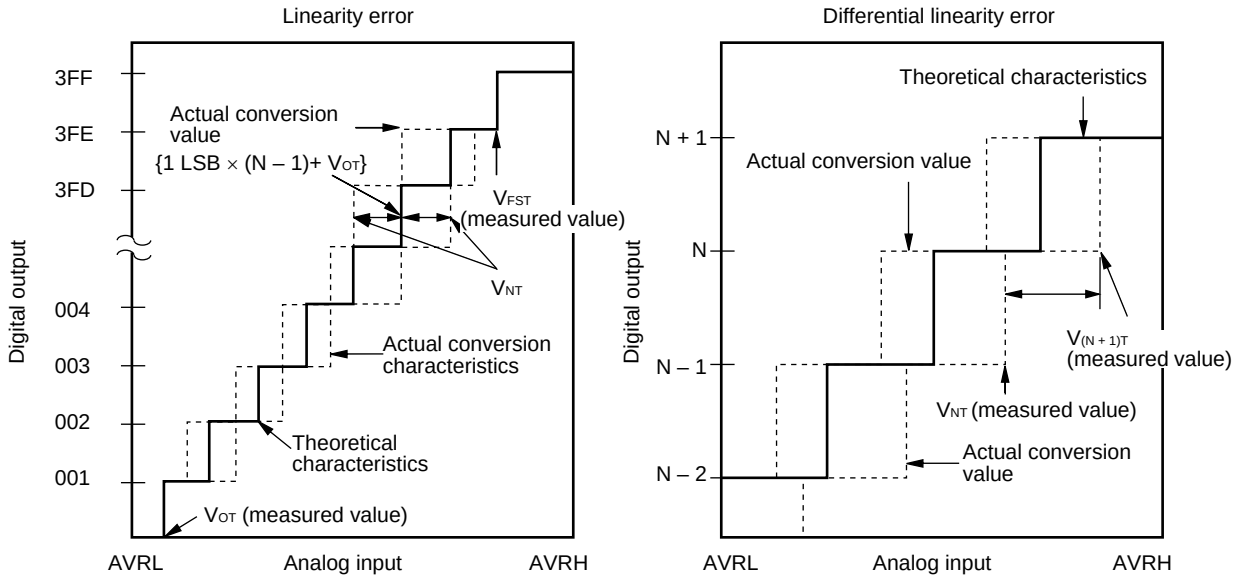
V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at transition of digital output from "000_H" to "001_H"
V_{FST}: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

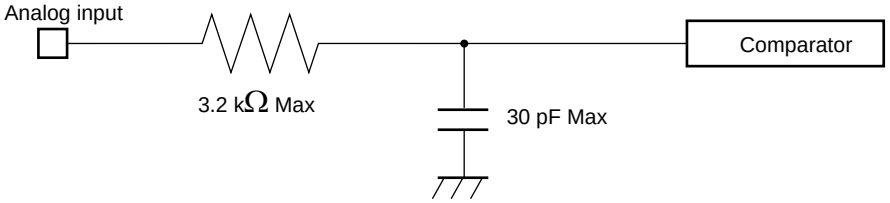
11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions,:

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**

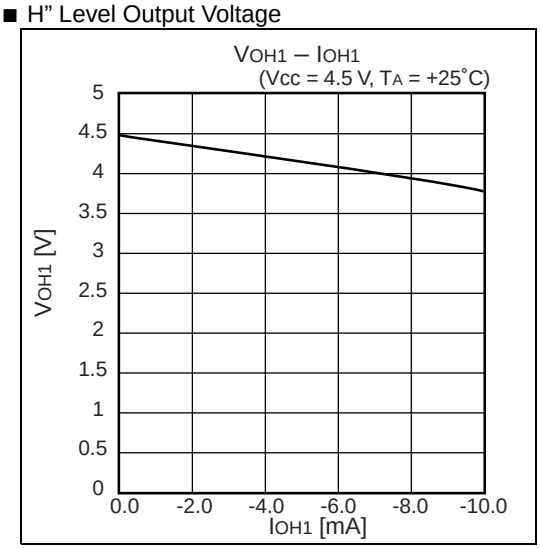


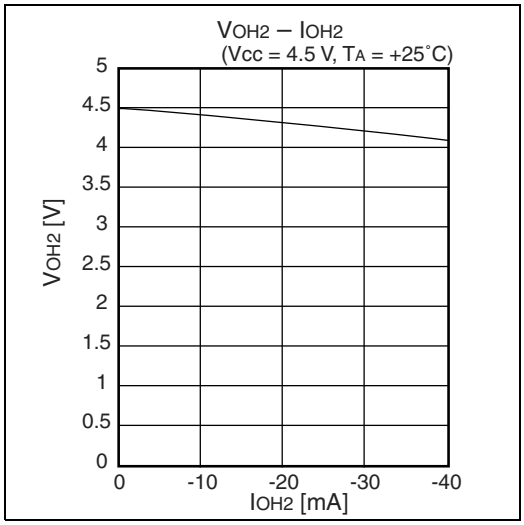
■ Error

The smaller the | AVRH − AVRL |, the greater the error would become relatively.

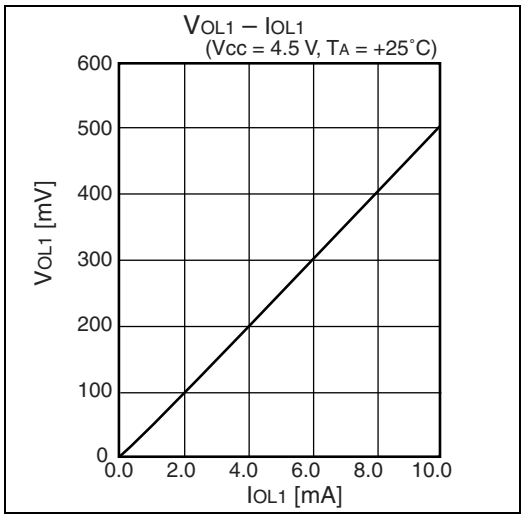
12. Example Characteristics

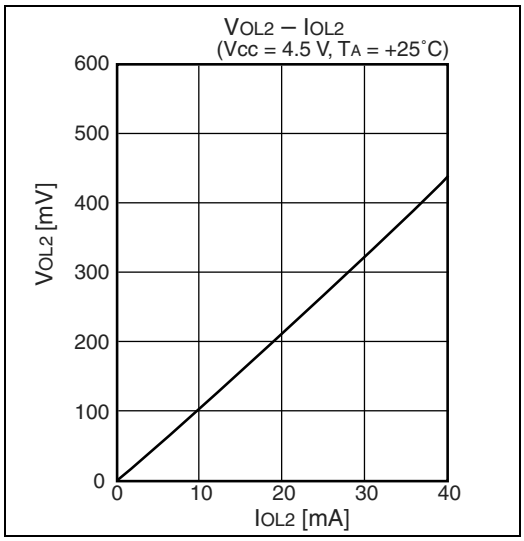
■ H" Level Output Voltage



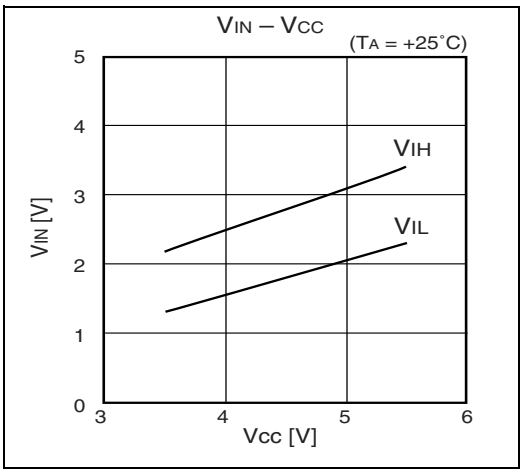


■ L" Level Input Voltage

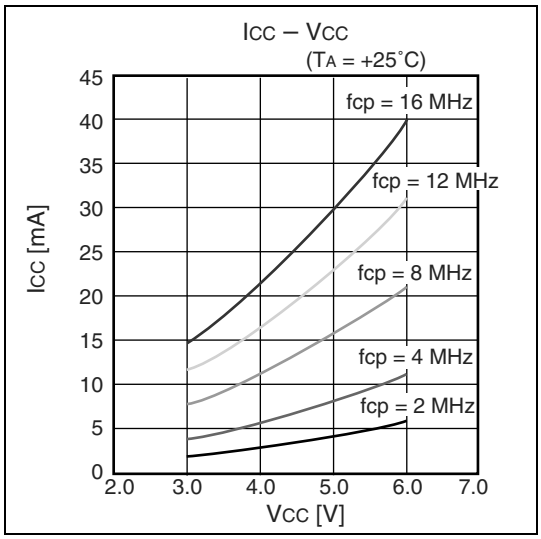


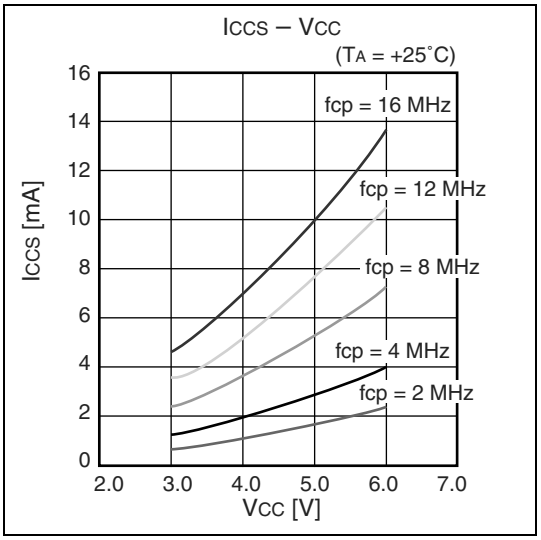


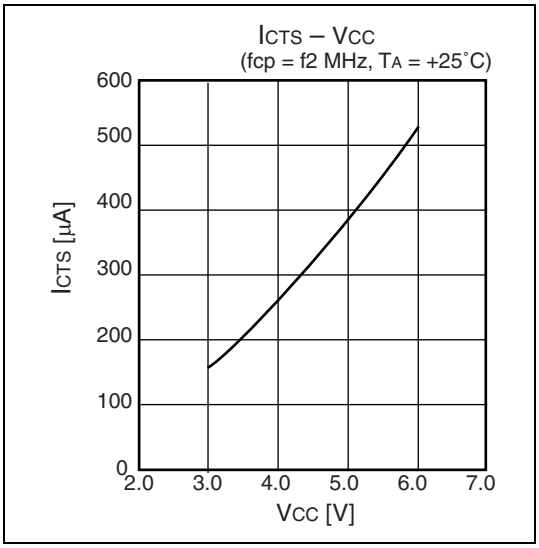
■ H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

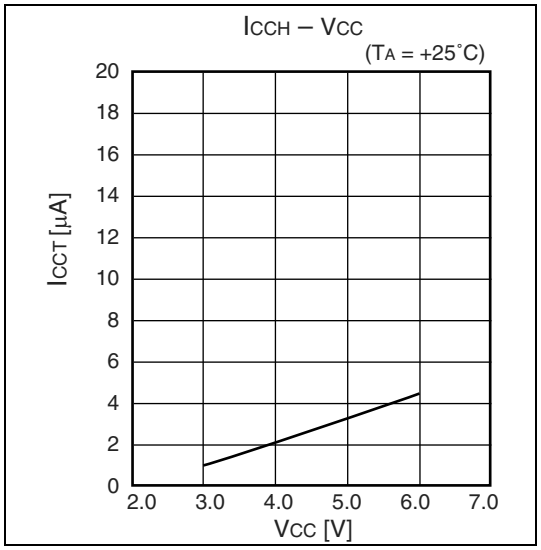


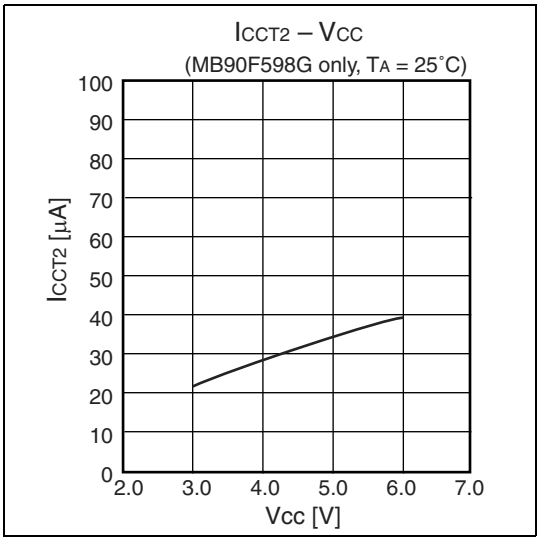
Supply Current











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