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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-166-er

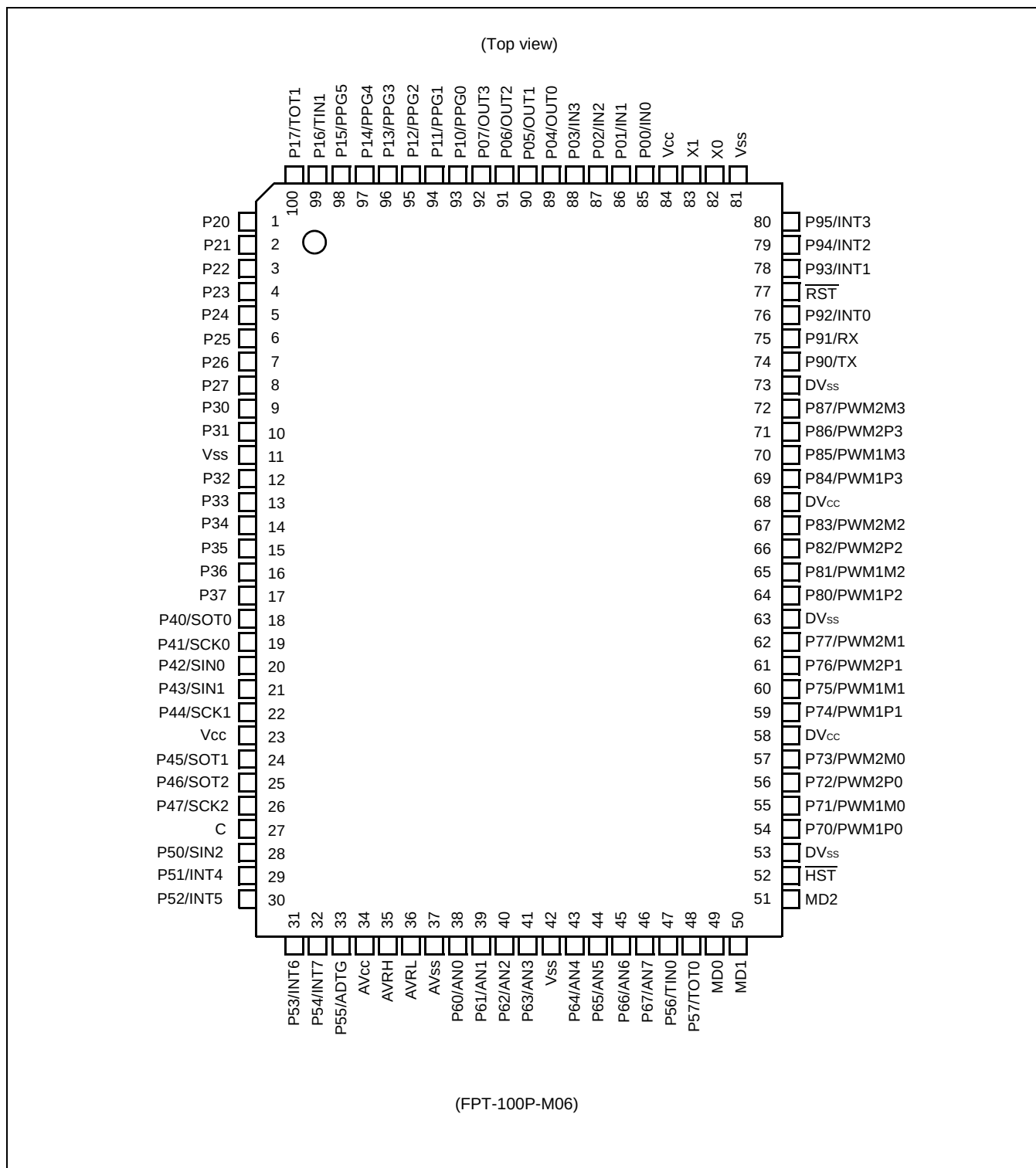
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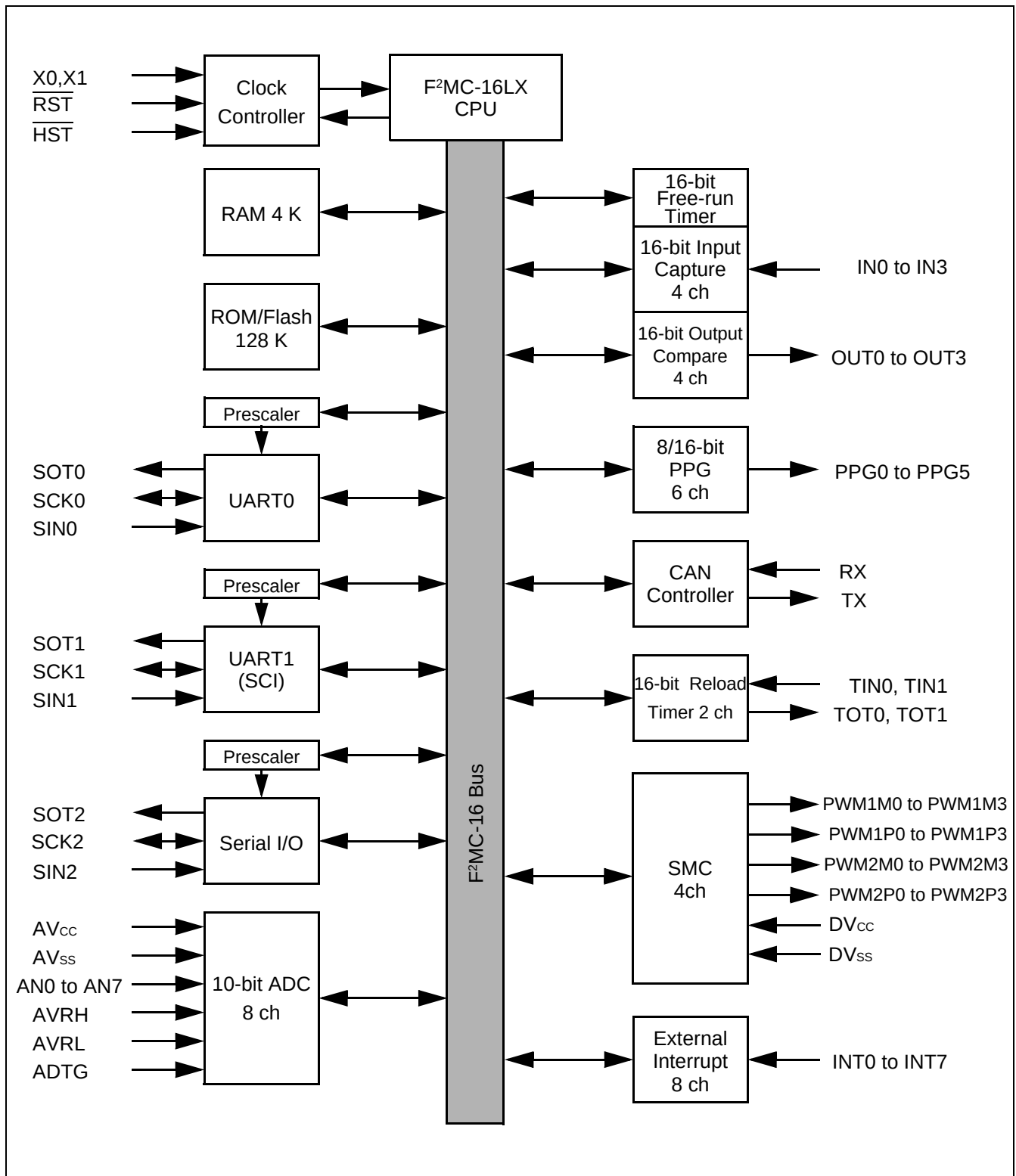
1. Product Lineup

Features		MB90598G	MB90F598G	MB90V595G
Classification		Mask ROM product	Flash ROM product	Evaluation product
ROM size		128 Kbytes	128 Kbytes Boot block Hard-wired reset vector	None
RAM size		4 Kbytes	4 Kbytes	6 Kbytes
Emulator-specific power supply *1		—		None
CPU functions		The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine clock frequency of 16 MHz) Interrupt processing time: 1.5 μs (at machine clock frequency of 16 MHz, minimum value)		
UART0		Clock synchronized transmission (500 K/1 M/2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 MHz) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
UART1(SCI)		Clock synchronized transmission (62.5 K/125 K/250 K/500 K/1 Mbps) Clock asynchronized transmission (1202/2404/4808/9615/31250 bps) Transmission can be performed by bi-directional serial transmission or by master/slave connection.		
8/10-bit A/D converter		Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)		
8/16-bit PPG timers (6 channels)		Number of channels: 6 (8/16-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: fsys, fsys/2 ¹ , fsys/2 ² , fsys/2 ³ , fsys/2 ⁴ (fsys = system clock frequency) 128μs (fosc = 4MHz: oscillation clock frequency)		
16-bit Reload timer		Number of channels: 2 Operation clock frequency: fsys/2 ¹ , fsys/2 ³ , fsys/2 ⁵ (fsys = System clock frequency) Supports External Event Count function		
16-bit I/O timer	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register		
	Input captures	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)		

2. Pin Assignment



6. Block Diagram



8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00 _H	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXX _B
01 _H	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXX _B
02 _H	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXX _B
03 _H	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXX _B
04 _H	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXX _B
05 _H	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXX _B
06 _H	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXX _B
07 _H	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXX _B
08 _H	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXX _B
09 _H	Port 9 Data Register	PDR9	R/W	Port 9	__ XXXXXX _B
0A _H to 0F _H	Reserved				
10 _H	Port 0 Direction Register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0 _B
11 _H	Port 1 Direction Register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0 _B
12 _H	Port 2 Direction Register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0 _B
13 _H	Port 3 Direction Register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0 _B
14 _H	Port 4 Direction Register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0 _B
15 _H	Port 5 Direction Register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0 _B
16 _H	Port 6 Direction Register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0 _B
17 _H	Port 7 Direction Register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0 _B
18 _H	Port 8 Direction Register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0 _B
19 _H	Port 9 Direction Register	DDR9	R/W	Port 9	__ 0 0 0 0 0 0 _B
1A _H	Reserved				
1B _H	Analog Input Enable Register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1 _B
1C _H to 1F _H	Reserved				
20 _H	Serial Mode Control Register 0	UMC0	R/W	UART0	0 0 0 0 0 1 0 0 _B
21 _H	Serial status Register 0	USR0	R/W		0 0 0 1 0 0 0 0 _B
22 _H	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W		XXXXXXXX _B
23 _H	Rate and Data Register 0	URD0	R/W		0 0 0 0 0 0 0 X _B
24 _H	Serial Mode Register 1	SMR1	R/W	UART1	0 0 0 0 0 0 0 0 _B
25 _H	Serial Control Register 1	SCR1	R/W		0 0 0 0 0 1 0 0 _B
26 _H	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W		XXXXXXXX _B
27 _H	Serial Status Register 1	SSR1	R/W		0 0 0 0 1 _ 0 0 _B
28 _H	UART1 Prescaler Control Register	U1CDCR	R/W		0 _ _ _ 1 1 1 1 _B

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
6F _H	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	_____1 _B
70 _H	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX _B
71 _H	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX _B
72 _H	PWM1 Select Register 0	PWS10	R/W		__ 0 0 0 0 0 _B
73 _H	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 _B
74 _H	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX _B
75 _H	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX _B
76 _H	PWM1 Select Register 1	PWS11	R/W		__ 0 0 0 0 0 _B
77 _H	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 _B
78 _H	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX _B
79 _H	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX _B
7A _H	PWM1 Select Register 2	PWS12	R/W		__ 0 0 0 0 0 _B
7B _H	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 _B
7C _H	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX _B
7D _H	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX _B
7E _H	PWM1 Select Register 3	PWS13	R/W		__ 0 0 0 0 0 _B
7F _H	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 _B
80 _H to 8F _H	CAN Controller. Refer to section about CAN Controller				
90 _H to 9D _H	Reserved				
9E _H	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 _B
9F _H	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	_____0 _B
A0 _H	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 _B
A1 _H	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 _B
A2 _H to A7 _H	Reserved				
A8 _H	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
A9 _H	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 __ 0 0 1 0 _B
AA _H to AD _H	Reserved				
AE _H	Flash Memory Control Status Register (MB90F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 _B
AF _H	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
B0 _H	Interrupt Control Register 00	ICR00	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B1 _H	Interrupt Control Register 01	ICR01	R/W		0 0 0 0 0 1 1 1 _B
B2 _H	Interrupt Control Register 02	ICR02	R/W		0 0 0 0 0 1 1 1 _B
B3 _H	Interrupt Control Register 03	ICR03	R/W		0 0 0 0 0 1 1 1 _B
B4 _H	Interrupt Control Register 04	ICR04	R/W	Interrupt controller	0 0 0 0 0 1 1 1 _B
B5 _H	Interrupt Control Register 05	ICR05	R/W		0 0 0 0 0 1 1 1 _B
B6 _H	Interrupt Control Register 06	ICR06	R/W		0 0 0 0 0 1 1 1 _B
B7 _H	Interrupt Control Register 07	ICR07	R/W		0 0 0 0 0 1 1 1 _B
B8 _H	Interrupt Control Register 08	ICR08	R/W		0 0 0 0 0 1 1 1 _B
B9 _H	Interrupt Control Register 09	ICR09	R/W		0 0 0 0 0 1 1 1 _B
BA _H	Interrupt Control Register 10	ICR10	R/W		0 0 0 0 0 1 1 1 _B
BB _H	Interrupt Control Register 11	ICR11	R/W		0 0 0 0 0 1 1 1 _B
BC _H	Interrupt Control Register 12	ICR12	R/W		0 0 0 0 0 1 1 1 _B
BD _H	Interrupt Control Register 13	ICR13	R/W		0 0 0 0 0 1 1 1 _B
BE _H	Interrupt Control Register 14	ICR14	R/W		0 0 0 0 0 1 1 1 _B
BF _H	Interrupt Control Register 15	ICR15	R/W		0 0 0 0 0 1 1 1 _B
C0 _H to FF _H	Reserved				
1900 _H	Reload Register L	PRL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX _B
1901 _H	Reload Register H	PRLH0	R/W		XXXXXXXX _B
1902 _H	Reload Register L	PRL1	R/W		XXXXXXXX _B
1903 _H	Reload Register H	PRLH1	R/W		XXXXXXXX _B
1904 _H	Reload Register L	PRL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX _B
1905 _H	Reload Register H	PRLH2	R/W		XXXXXXXX _B
1906 _H	Reload Register L	PRL3	R/W		XXXXXXXX _B
1907 _H	Reload Register H	PRLH3	R/W		XXXXXXXX _B
1908 _H	Reload Register L	PRL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX _B
1909 _H	Reload Register H	PRLH4	R/W		XXXXXXXX _B
190A _H	Reload Register L	PRL5	R/W		XXXXXXXX _B
190B _H	Reload Register H	PRLH5	R/W		XXXXXXXX _B
190C _H	Reload Register L	PRL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX _B
190D _H	Reload Register H	PRLH6	R/W		XXXXXXXX _B
190E _H	Reload Register L	PRL7	R/W		XXXXXXXX _B
190F _H	Reload Register H	PRLH7	R/W		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910 _H	Reload Register L	PRL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXX _B
1911 _H	Reload Register H	PRLH8	R/W		XXXXXXXX _B
1912 _H	Reload Register L	PRL9	R/W		XXXXXXXX _B
1913 _H	Reload Register H	PRLH9	R/W		XXXXXXXX _B
1914 _H	Reload Register L	PRLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX _B
1915 _H	Reload Register H	PRLHA	R/W		XXXXXXXX _B
1916 _H	Reload Register L	PRLB	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXX _B
1917 _H	Reload Register H	PRLHB	R/W		XXXXXXXX _B
1918 _H to 191F _H	Reserved				
1920 _H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXX _B
1921 _H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXX _B
1922 _H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXX _B
1923 _H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXX _B
1924 _H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXX _B
1925 _H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXX _B
1926 _H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXX _B
1927 _H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXX _B
1928 _H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXX _B
1929 _H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXX _B
192A _H	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXX _B
192B _H	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXX _B

(Continued)

Address	Register	Abbreviation	Access	Initial Value
001A2C _H	ID register 3	IDR3	R/W	XXXXXXXX XXXXXXXX _B
001A2D _H				
001A2E _H				XXXXX--- XXXXXXXX _B
001A2F _H				
001A30 _H	ID register 4	IDR4	R/W	XXXXXXXX XXXXXXXX _B
001A31 _H				
001A32 _H				XXXXX--- XXXXXXXX _B
001A33 _H				
001A34 _H	ID register 5	IDR5	R/W	XXXXXXXX XXXXXXXX _B
001A35 _H				
001A36 _H				XXXXX--- XXXXXXXX _B
001A37 _H				
001A38 _H	ID register 6	IDR6	R/W	XXXXXXXX XXXXXXXX _B
001A39 _H				
001A3A _H				XXXXX--- XXXXXXXX _B
001A3B _H				
001A3C _H	ID register 7	IDR7	R/W	XXXXXXXX XXXXXXXX _B
001A3D _H				
001A3E _H				XXXXX--- XXXXXXXX _B
001A3F _H				

(Continued)

9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60 _H	DLC register 0	DLCR0	R/W	----XXXX _B
001A61 _H				
001A62 _H	DLC register 1	DLCR1	R/W	----XXXX _B
001A63 _H				
001A64 _H	DLC register 2	DLCR2	R/W	----XXXX _B
001A65 _H				
001A66 _H	DLC register 3	DLCR3	R/W	----XXXX _B
001A67 _H				
001A68 _H	DLC register 4	DLCR4	R/W	----XXXX _B
001A69 _H				
001A6A _H	DLC register 5	DLCR5	R/W	----XXXX _B
001A6B _H				
001A6C _H	DLC register 6	DLCR6	R/W	----XXXX _B
001A6D _H				
001A6E _H	DLC register 7	DLCR7	R/W	----XXXX _B
001A6F _H				
001A70 _H	DLC register 8	DLCR8	R/W	----XXXX
001A71 _H				
001A72 _H	DLC register 9	DLCR9	R/W	----XXXX _B
001A73 _H				
001A74 _H	DLC register 10	DLCR10	R/W	----XXXX _B
001A75 _H				
001A76 _H	DLC register 11	DLCR11	R/W	----XXXX _B
001A77 _H				
001A78 _H	DLC register 12	DLCR12	R/W	----XXXX _B
001A79 _H				
001A7A _H	DLC register 13	DLCR13	R/W	----XXXX _B
001A7B _H				
001A7C _H	DLC register 14	DLCR14	R/W	----XXXX _B
001A7D _H				
001A7E _H	DLC register 15	DLCR15	R/W	----XXXX _B
001A7F _H				
001A80 _H to 001A87 _H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXX _B to XXXXXXXX _B

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
001A88 _H to 001A8F _H	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX _B to XXXXXXXX _B
001A90 _H to 001A97 _H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX _B to XXXXXXXX _B
001A98 _H to 001A9F _H	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX _B to XXXXXXXX _B
001AA0 _H to 001AA7 _H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX _B to XXXXXXXX _B
001AA8 _H to 001AAF _H	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX _B to XXXXXXXX _B
001AB0 _H to 001AB7 _H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX _B to XXXXXXXX _B
001AB8 _H to 001ABF _H	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX _B to XXXXXXXX _B
001AC0 _H to 001AC7 _H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX _B to XXXXXXXX _B
001AC8 _H to 001ACF _H	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX _B to XXXXXXXX _B
001AD0 _H to 001AD7 _H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX _B to XXXXXXXX _B
001AD8 _H to 001ADF _H	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX _B to XXXXXXXX _B
001AE0 _H to 001AE7 _H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX _B to XXXXXXXX _B
001AE8 _H to 001AEF _H	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX _B to XXXXXXXX _B
001AF0 _H to 001AF7 _H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX _B to XXXXXXXX _B
001AF8 _H to 001AFF _H	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX _B to XXXXXXXX _B

(Continued)

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV_{CC} , AV_{SS} , $AVRH$, $AVRL$, V_{CC} , V_{SS} , DV_{CC} , DV_{SS} , P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	k Ω	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	k Ω	

* : The power supply current testing conditions are when using the external clock.

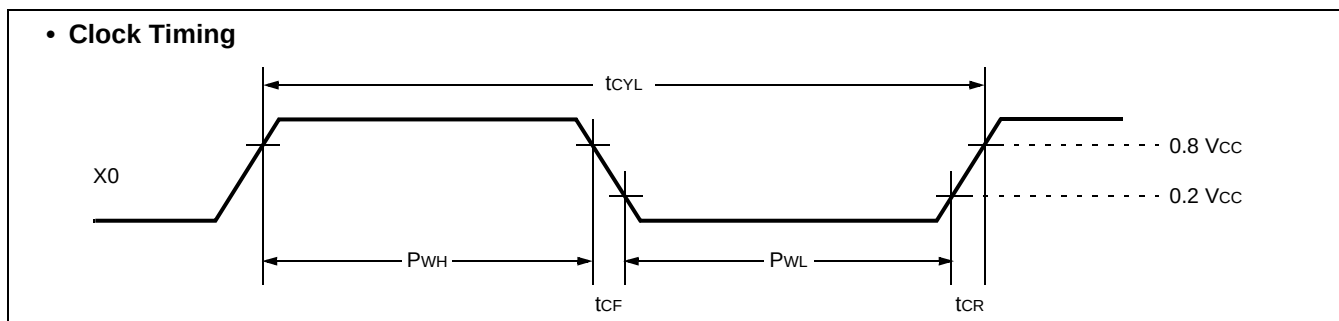
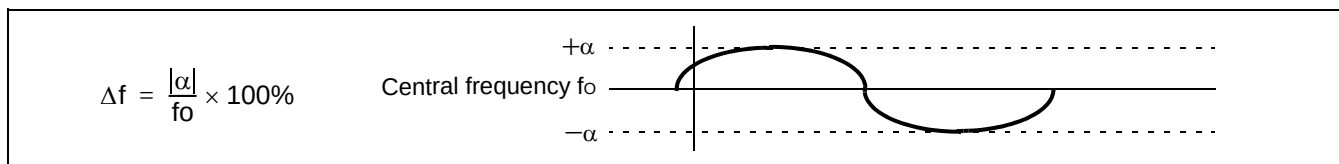
11.4 AC Characteristics

11.4.1 Clock Timing

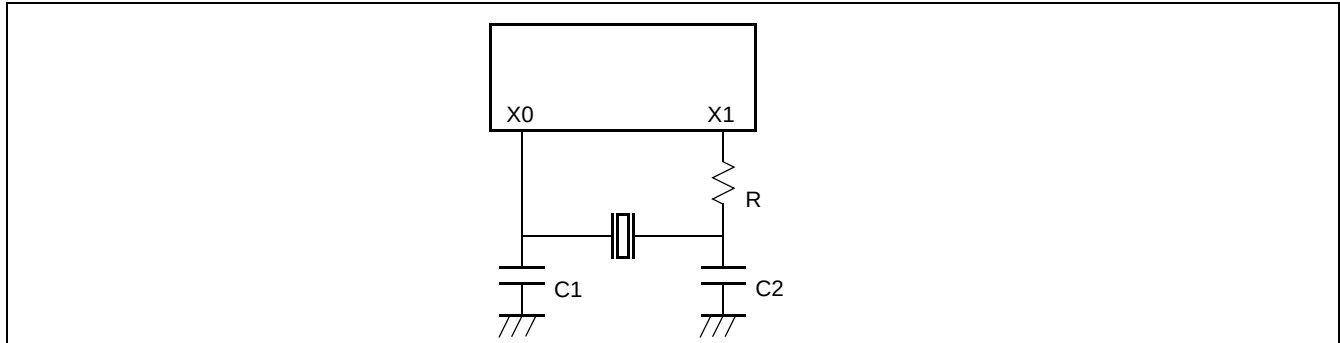
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_c	X0, X1	3	—	5	MHz	When using oscillation circuit
Oscillation cycle time	t_{CYL}	X0, X1	200	—	333	ns	When using oscillation circuit
External clock frequency	f_c	X0, X1	3	—	16	MHz	When using external clock
External clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using external clock
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH} , P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR} , t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash Read cycle time	t_{CYL}	—	—	$2 \cdot t_{CP}$	—	ns	When Flash is accessed via CPU

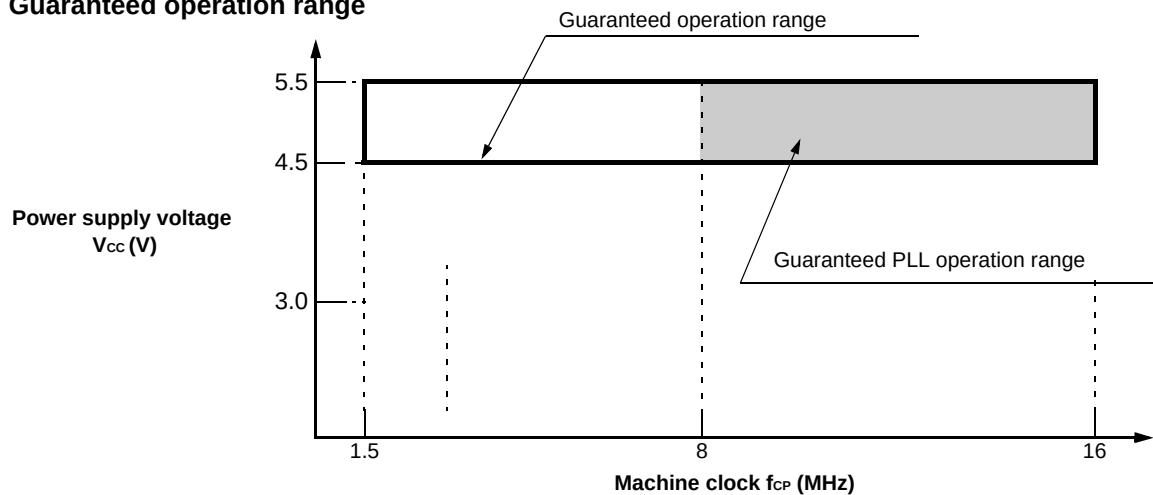
*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.



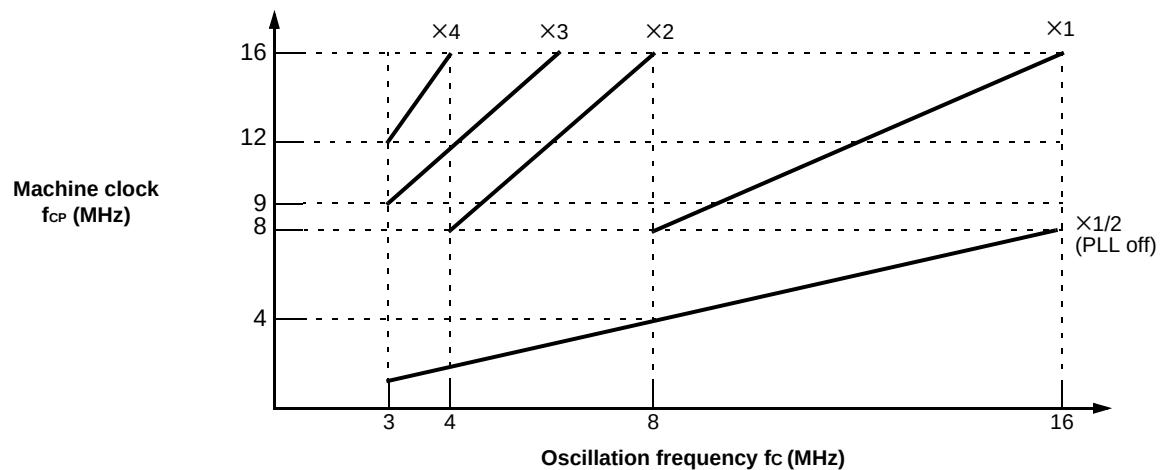
■ Example of Oscillation circuit



• **Guaranteed operation range**



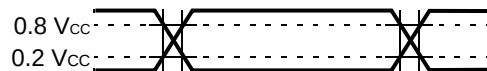
• **Oscillation frequency and machine clock frequency**



AC characteristics are set to the measured reference voltage values below.

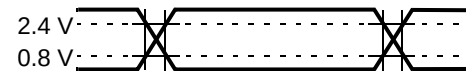
• **Input signal waveform**

Hysteresis Input Pin



• **Output signal waveform**

Output Pin



11.4.3 Power On Reset

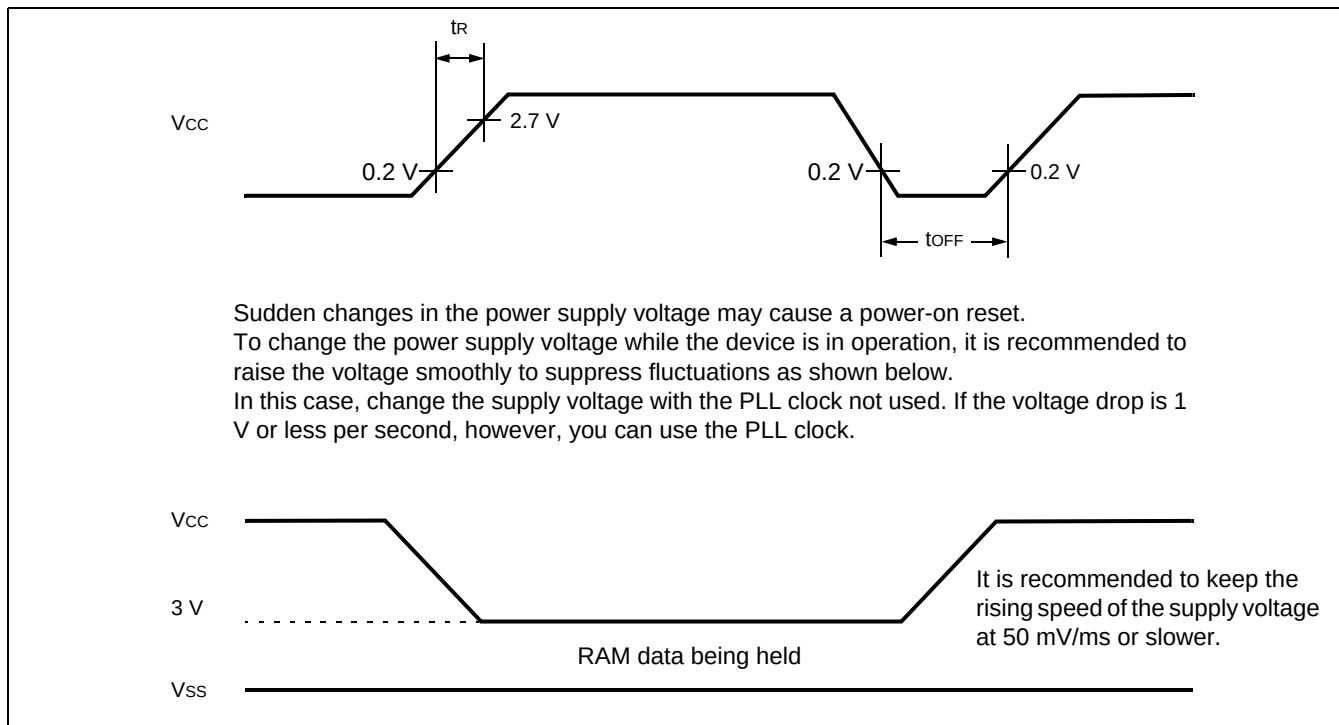
($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

*: V_{CC} must be kept lower than 0.2 V before power-on.

Notes:

- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn on the power supply using the above values.

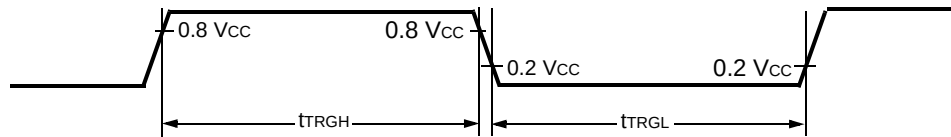


11.4.4 UART0/1, Serial I/O Timing

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are $C_L = 80\text{ pF} + 1\text{ TTL}$.	$8\ t_{CP}$	—	ns	
SCK $\downarrow \Rightarrow$ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		-80	80	ns	
Valid SIN $\Rightarrow$ SCK $\uparrow$	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK $\uparrow \Rightarrow$ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

• Trigger Input Timing



11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)

($V_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	150	ns	

• Slew Rate Output Timing



$$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$$

$$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$$

11.5 A/D Converter

($V_{CC} = AV_{CC} = 5.0\text{ V} \pm 10\%$, $V_{SS} = AV_{SS} = 0.0\text{ V}$, $3.0\text{ V} \leq AV_{RH} - AV_{RL}$, $T_A = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$)

Parameter	Sym- bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	± 5.0	LSB	
Nonlinearity error	—	—	—	—	± 2.5	LSB	
Differential linearity error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	$AV_{RL} - 3.5\text{ LSB}$	$AV_{RL} + 0.5\text{ LSB}$	$AV_{RL} + 4.5\text{ LSB}$	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	$AV_{RH} - 6.5\text{ LSB}$	$AV_{RH} - 1.5\text{ LSB}$	$AV_{RH} + 1.5\text{ LSB}$	V	
Conversion time	—	—	—	$352t_{CP}$	—	ns	
Sampling time	—	—	—	$64t_{CP}$	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	-10	—	10	μA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AV_{RL}	—	AV_{RH}	V	

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	—	AVRH	AVRL + 3.0	—	AV _{CC}	V	
	—	AVRL	0	—	AVRH – 3.0	V	
Power supply current	I _A	AV _{CC}	—	5	—	mA	
	I _{AH}	AV _{CC}	—	—	5	μA	*
Reference voltage current	I _R	AVRH	—	400	600	μA	MB90V595G, MB90F598G
			—	140	600	μA	MB90598G
	I _{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current ($V_{CC} = AV_{CC} = AVRH = 5.0$ V) when the CPU is stopped.

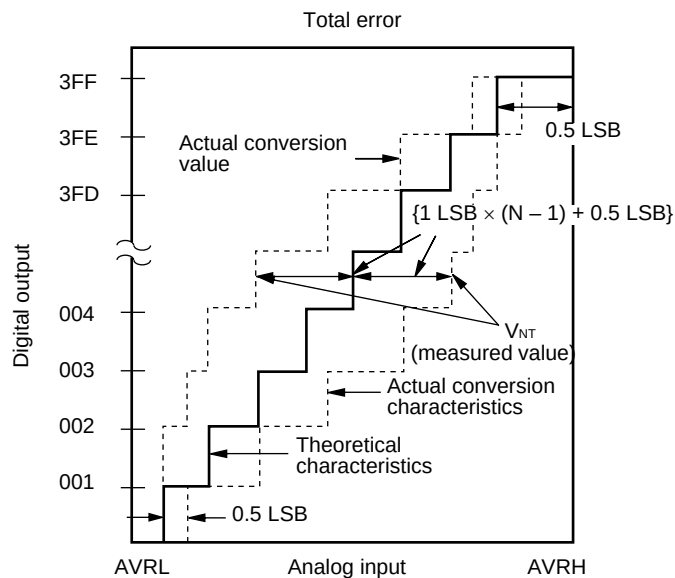
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point ("00 0000 0000" ↔ "00 0000 0001") with the full-scale transition point ("11 1111 1110" ↔ "11 1111 1111") from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1 \text{ LSB} = (\text{Theoretical value}) \frac{AVRH - AVRL}{1024} \text{ [V]}$$

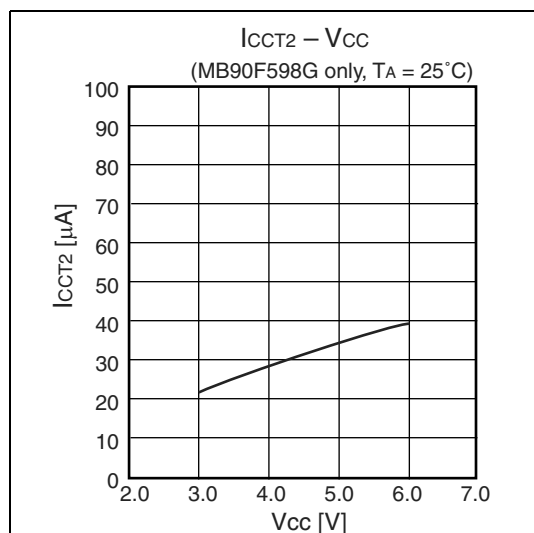
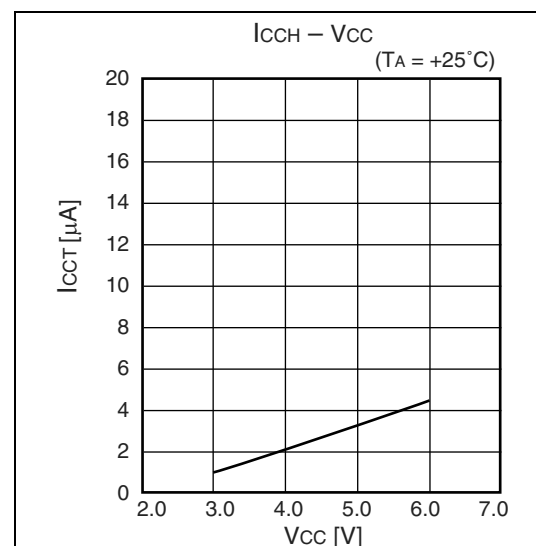
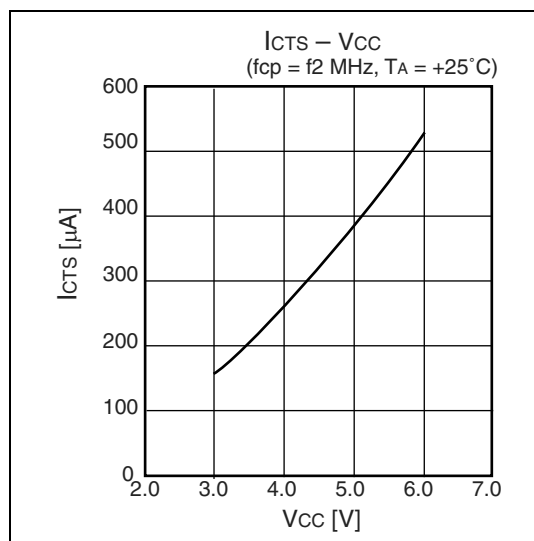
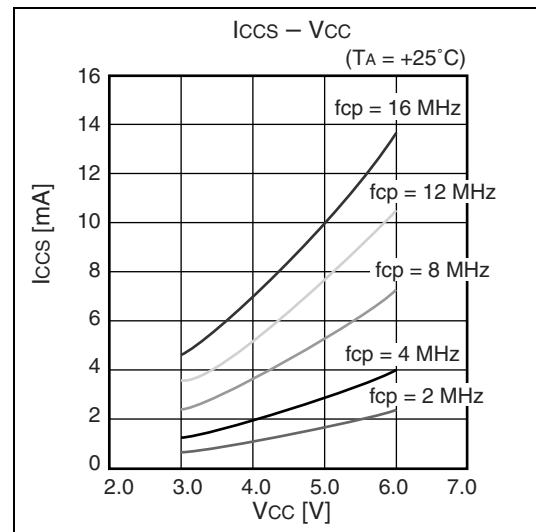
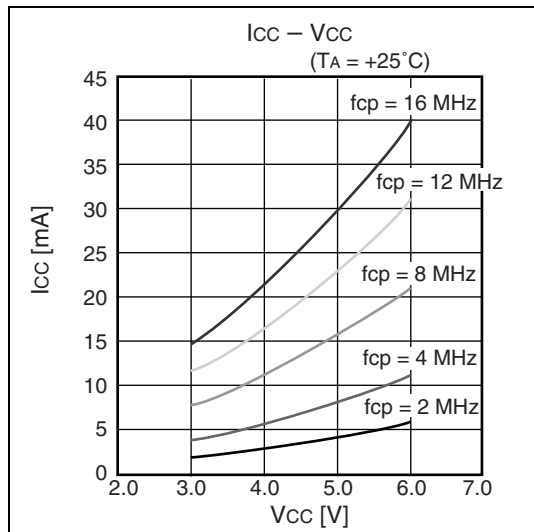
$$V_{OT} (\text{Theoretical value}) = AVRL + 0.5 \text{ LSB [V]}$$

$$V_{FST} (\text{Theoretical value}) = AVRH - 1.5 \text{ LSB [V]}$$

$$\text{Total error for digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times (N - 1) + 0.5 \text{ LSB}\}}{1 \text{ LSB}} \text{ [LSB]}$$

V_{NT} : Voltage at a transition of digital output from $(N - 1)$ to N

(Continued)

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