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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-178e1





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3. Pin Description

Pin no.	Pin name	Circuit type	Function			
82	X0					
83	X1	А	Oscillator pin			
77	RST	В	Reset input			
52	HST	С	Hardware standby input			
05 to 00	P00 to P03	0	Reset input Hardware standby input General purpose IO Inputs for the Input Captures General purpose IO Outputs for the Output Compares. General purpose IO Outputs for the Programmable Pulse Generators General purpose IO TIN input for the 16-bit Reload Timer 1 General purpose IO TOT output for the 16-bit Reload Timer 1 General purpose IO SOT output for UART 0 General purpose IO SCK input/output for UART 0 General purpose IO SIN input for UART 1 General purpose IO SIN input for UART 1 General purpose IO SCK input/output for UART 1 General purpose IO SCK input/output for UART 1 General purpose IO SCK input/output for UART 1 General purpose IO SOT output for UART 1			
85 to 88	IN0 to IN3	G	Inputs for the Input Captures			
89 to 92	P04 to P07	0	General purpose IO			
89 10 92	OUT0 to OUT3	G	Outputs for the Output Compares.			
00 to 00	P10 to P15	5	General purpose IO			
93 to 98	PPG0 to PPG5	D	Outputs for the Programmable Pulse Generators			
00	P16	5	General purpose IO			
99	TIN1	D	TIN input for the 16-bit Reload Timer 1			
400	P17	5	General purpose IO			
100	TOT1	D	General purpose IO TOT output for the 16-bit Reload Timer 1 General purpose IO			
1 to 8	P20 to P27	G				
9 to 10	P30 to P31	G	General purpose IO			
12 to 16	P32 to P36	G				
17	P37	D	General purpose IO General purpose IO			
40	P40	0	General purpose IO			
18	SOT0	G	SOT output for UART 0			
40	P41	0	General purpose IO			
19	SCK0	G	SCK input/output for UART 0			
200	P42	0	General purpose IO			
20	SIN0	G	SIN input for UART 0			
04	P43	0	General purpose IO			
21	SIN1	G	SIN input for UART 1			
00	P44	0	General purpose IO			
22	SCK1	G	SCK input/output for UART 1			
24	P45		General purpose IO			
24	SOT1	G	SOT output for UART 1			
O.F.	P46		General purpose IO			
25	SOT2	G	SOT output for the Serial IO			
oe.	P47		General purpose IO			
26	SCK2	G	SCK input/output for the Serial IO			



(5) Pull-up/down resistors

The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (Vcc).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AVcc (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to AVcc = Vcc, AVss = AVRH = DVcc = Vss.

(9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

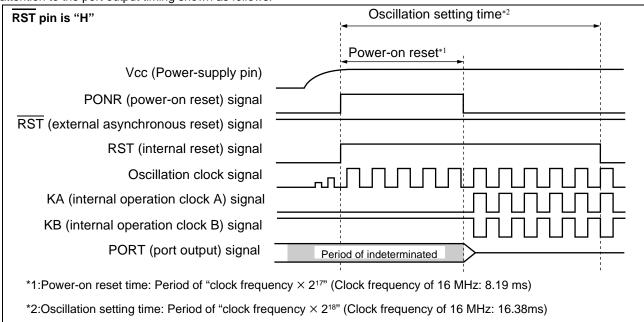
(10) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at $50 \mu s$ or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)

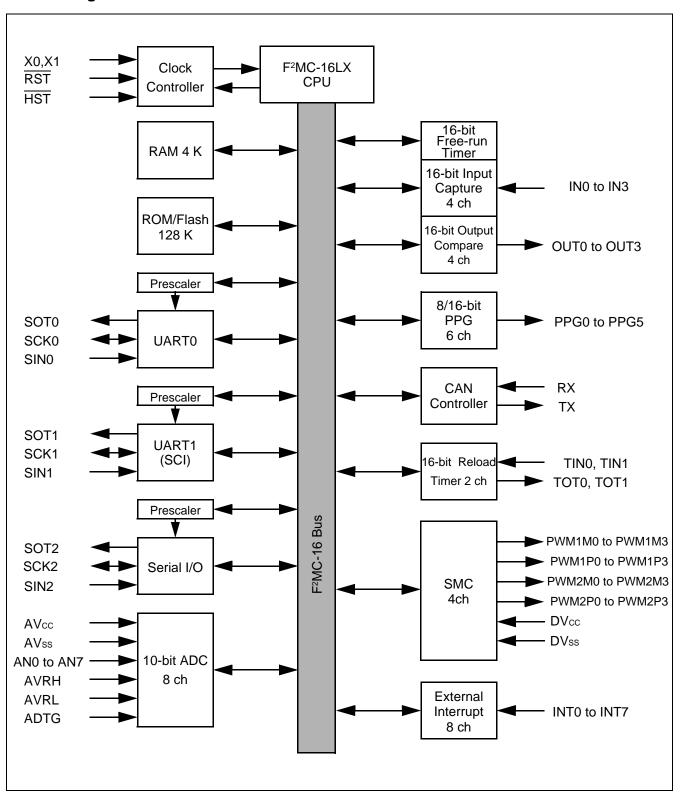
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If RST pin is "H", the outputs become indeterminate.
- If RST pin is "L", the outputs become high-impedance. Pay attention to the port output timing shown as follows.





6. Block Diagram





Address	Register	Abbreviation	Access	Peripheral	Initial value
29н to 2Ан		Reserved			
2Вн	Serial IO Prescaler	SCDCR	R/W		01111в
2Сн	Serial Mode Control Register (low-order)	SMCS	R/W		0000в
2Dн	Serial Mode Control Register (high-order)	SMCS	R/W	Serial IO	0 0 0 0 0 0 1 Ов
2Ен	Serial Data Register	SDR	R/W		XXXXXXXX
2Fн	Edge Selector	SES	R/W		Ов
30н	External Interrupt Enable Register	ENIR	R/W		0 0 0 0 0 0 0 0в
31н	External Interrupt Request Register	EIRR	R/W	Fortament laster was unit	XXXXXXXXB
32н	External Interrupt Level Register	ELVR	R/W	External Interrupt	0 0 0 0 0 0 0 0 В
33н	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0 В
34н	A/D Control Status Register 0	ADCS0	R/W		0 0 0 0 0 0 0 0 В
35н	A/D Control Status Register 1	ADCS1	R/W	A/D Converter	0 0 0 0 0 0 0 0 В
36н	A/D Data Register 0	ADCR0	R	A/D Conventer	XXXXXXXXB
37н	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 _ XX _B
38н	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable	0_0001в
39н	PPG1 Operation Mode Control Register	PPGC1	R/W	Pulse	0_00001в
ЗАн	PPG0, 1 Output Pin Control Register	PPG01	R/W	Generator 0/1	0 0 0 0 0 0B
3Вн		Reserved	İ		
3Сн	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable	0_0001в
3Dн	PPG3 Operation Mode Control Register	PPGC3	R/W	Pulse	0_00001в
3Ен	PPG2, 3 Output Pin Control Register	PPG23	R/W	Generator 2/3	000000в
3Fн		Reserved			
40н	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable	0_0001в
41н	PPG5 Operation Mode Control Register	PPGC5	R/W	Pulse	0_00001в
42н	PPG4, 5 Output Pin Control Register	PPG45	R/W	Generator 4/5	000000в
43н		Reserved		-	
44н	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable	0_0001в
45н	PPG7 Operation Mode Control Register	PPGC7	R/W	Pulse	0_00001в
46н	PPG6, 7 Output Pin Control Register	PPG67	R/W	Generator 6/7	000000в
47н		Reserved	<u> </u>	1	
48н	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable	0_0001в
49н	PPG9 Operation Mode Control Register	PPGC9	R/W	Pulse	0_00001в
4Ан	PPG8, 9 Output Pin Control Register	PPG89	R/W	Generator 8/9	0 0 0 0 0 0B
4Вн		Reserved	<u> </u> 	l .	



Address	Register	Abbreviation	Access	Peripheral	Initial value
6 Fн	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	1в
70н	PWM1 Compare Register 0	PWC10	R/W		XXXXXXXX
71н	PWM2 Compare Register 0	PWC20	R/W	Stepping Motor	XXXXXXXX
72н	PWM1 Select Register 0	PWS10	R/W	Controller 0	0 0 0 0 0 0 _B
73н	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0 _B
74н	PWM1 Compare Register 1	PWC11	R/W		XXXXXXXX
75н	PWM2 Compare Register 1	PWC21	R/W	Stepping Motor	XXXXXXXX
76н	PWM1 Select Register 1	PWS11	R/W	Controller 1	0 0 0 0 0 0 _B
77н	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0 0в
78н	PWM1 Compare Register 2	PWC12	R/W		XXXXXXXX
79н	PWM2 Compare Register 2	PWC22	R/W	Stepping Motor	XXXXXXXX
7Ан	PWM1 Select Register 2	PWS12	R/W	Controller 2	0 0 0 0 0 0 _B
7Вн	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0
7Сн	PWM1 Compare Register 3	PWC13	R/W		XXXXXXXX
7Dн	PWM2 Compare Register 3	PWC23	R/W	Stepping Motor	XXXXXXXX
7Ен	PWM1 Select Register 3	PWS13	R/W	Controller 3	000000
7 Fн	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 0
80н to 8Fн	CAN Controll	er. Refer to section	about CAN	Controller	
90н to 9Dн		Reserved			
9Ен	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0
9Fн	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	0i
А0н	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 O
А1н	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 Oı
А2н to А7н		Reserved	l .		
А8н	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1 _B
А9н	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	100100i
ААн to ADн		Reserved	ı		
АЕн	Flash Memory Control Status Register (MB90F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	000X0000
АҒн		Reserved			



Address	Register	Abbreviation	Access	Peripheral	Initial value
ВОн	Interrupt Control Register 00	ICR00	R/W		00000111в
В1н	Interrupt Control Register 01	ICR01	R/W	latera at controller	00000111в
В2н	Interrupt Control Register 02	ICR02	R/W	Interrupt controller	00000111в
ВЗн	Interrupt Control Register 03	ICR03	R/W		00000111в
В4н	Interrupt Control Register 04	ICR04	R/W		00000111в
В5н	Interrupt Control Register 05	ICR05	R/W		00000111в
В6н	Interrupt Control Register 06	ICR06	R/W	Interrupt controller	00000111в
В7н	Interrupt Control Register 07	ICR07	R/W		00000111в
В8н	Interrupt Control Register 08	ICR08	R/W		00000111в
В9н	Interrupt Control Register 09	ICR09	R/W		00000111в
ВАн	Interrupt Control Register 10	ICR10	R/W		00000111в
ВВн	Interrupt Control Register 11	ICR11	R/W		00000111в
ВСн	Interrupt Control Register 12	ICR12	R/W		00000111в
ВОн	Interrupt Control Register 13	ICR13	R/W		00000111в
ВЕн	Interrupt Control Register 14	ICR14	R/W		00000111В
ВГн	Interrupt Control Register 15	ICR15	R/W		00000111в
C0н to FFн		Resei	rved		
1900н	Reload Register L	PRLL0	R/W		XXXXXXXX
1901н	Reload Register H	PRLH0	R/W	16-bit Programmable Pulse	XXXXXXXX
1902н	Reload Register L	PRLL1	R/W	Generator 0/1	XXXXXXXX
1903н	Reload Register H	PRLH1	R/W		XXXXXXXX
1904н	Reload Register L	PRLL2	R/W		XXXXXXXX
1905н	Reload Register H	PRLH2	R/W	16-bit Programmable Pulse	XXXXXXXX
1906н	Reload Register L	PRLL3	R/W	Generator 2/3	XXXXXXXX
1907н	Reload Register H	PRLH3	R/W		XXXXXXXX
1908н	Reload Register L	PRLL4	R/W		XXXXXXXX
1909н	Reload Register H	PRLH4	R/W	16-bit Programmable	XXXXXXXX
190Ан	Reload Register L	PRLL5	R/W	Pulse Generator 4/5	XXXXXXXXB
190Вн	Reload Register H	PRLH5	R/W		XXXXXXXX
190Сн	Reload Register L	PRLL6	R/W		XXXXXXXXB
190Он	Reload Register H	PRLH6	R/W	16-bit Programmable	XXXXXXXX
190Ен	Reload Register L	PRLL7	R/W	Pulse Generator 6/7	XXXXXXXXB
190Fн	Reload Register H	PRLH7	R/W		XXXXXXXX



Address	Register	Abbreviation	Access	Peripheral	Initial value
1910н	Reload Register L	PRLL8	R/W		XXXXXXX
1911н	Reload Register H	PRLH8	R/W	16-bit Programmable Pulse	XXXXXXXXB
1912н	Reload Register L	PRLL9	R/W	Generator 8/9	XXXXXXXXB
1913н	Reload Register H	PRLH9	R/W		XXXXXXXXB
1914н	Reload Register L	PRLLA	R/W	16-bit Programmable Pulse	XXXXXXXXB
1915н	Reload Register H	PRLHA	R/W	Generator A/B	XXXXXXXXB
1916н	Reload Register L	PRLLB	R/W	16-bit Programmable Pulse	XXXXXXXXB
1917н	Reload Register H	PRLHB	R/W	Generator A/B	XXXXXXXXB
1918н to 191Fн		Re	served		
1920н	Input Capture Register 0 (low-order)	IPCP0	R		XXXXXXX
1921н	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXX
1922н	Input Capture Register 1 (low-order)	IPCP1	R	Input Capture 0/1	XXXXXXX
1923н	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXX
1924н	Input Capture Register 2 (low-order)	IPCP2	R		XXXXXXXX
1925н	Input Capture Register 2 (high-order)	IPCP2	R	January Continue 2/2	XXXXXXX
1926н	Input Capture Register 3 (low-order)	IPCP3	R	Input Capture 2/3	XXXXXXXXB
1927н	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXXB
1928н	Output Compare Register 0 (low-order)	OCCP0	R/W		XXXXXXXXB
1929н	Output Compare Register 0 (high-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
192Ан	Output Compare Register 1 (low-order)	OCCP1	R/W	Output Compare 0/1	XXXXXXXXB
192Вн	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB



Address	Register	Abbreviation	Access	Peripheral	Initial value	
192Сн	Output Compare Register 2 (low-order)	OCCP2	R/W		XXXXXXXX	
192Dн	Output Compare Register 2 (high-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX	
192Ен	Output Compare Register 3 (low-order)	OCCP3	R/W	Output Compare 2/3	XXXXXXXX	
192Fн	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX	
1930н to 19FFн	Reserved					
1A00н to 1AFFн	CAN	Controller. Refer to	section abou	ut CAN Controller		
1В00н to 1ВFFн	CAN	Controller. Refer to	section abou	ut CAN Controller		
1С00н to 1EFFн		Re	served			
1FF0н	Program Address Detection Register 0 (low-order)			about CAN Controller about CAN Controller	XXXXXXXX	
1FF1н	Program Address Detection Register 0 (middle-order)	PADR0	R/W		XXXXXXXXB	
1FF2н	Program Address Detection Register 0 (high-order)			Address Match	XXXXXXXX	
1FF3н	Program Address Detection Register 1 (low-order)			Detection Function	XXXXXXXX	
1FF4н	Program Address Detection Register 1 (middle-order)	PADR1	R/W		XXXXXXXXB	
1FF5н	Program Address Detection Register 1 (high-order)				XXXXXXXXB	
1FF6н to 1FFFн		Re	served			

■ Description for Read/Write R/W : Readable/writable

R : Read only W : Write only

■ Description of initial value

0 : the initial value of this bit is "0".
1 : the initial value of this bit is "1".

X: the initial value of this bit is undefined.

_ : this bit is unused. the initial value is undefined.

Note: : Addresses in the range of 0000_H to 00FF_H, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading "X", and any write access should not be performed.



Address	Register	Abbreviation	Access	Initial Value		
001А60н	DLC register 0	DI CDO	DAM	VVV-		
001А61н	- DLC register 0	DLCRU		XXXX _B		
001А62н	DLC register 1	DI CP1	DAM.	XXXX _B		
001А63н	DLC register 0 DLC register 1 DLC register 2 DLC register 3 DLC register 4 DLC register 5 DLC register 6 DLC register 7 DLC register 8 DLC register 9 DLC register 10 DLC register 11 DLC register 12 DLC register 13 DLC register 14	DLCKT	R/VV	\ \\\\		
001А64н	DLC register 2	DI CR2	RW	ХХХХв		
001А65н	DEG Tegister 2	DEGINZ	1077	70000		
001А66н	DLC register 3	DLCR3	RW	XXXX _B		
001А67н	DEC register o	BEONO	1077	70000		
001А68н	DLC register 4	DI CR4	RW	XXXX _B		
001А69н	220 Tog.ioto. 1	5251(1	1011	7000		
001А6Ан	DLC register 5	DI CR5	R/W	XXXX _B		
001А6Вн	220 reg.etc. 0	320.10		AAAAB		
001А6Сн	DLC register 6	DI CR6	R/W	XXXX _B		
001А6Dн	220 reg.etc. 0	320.10		7.000		
001А6Ен	DLC register 7	DLCR7	R/W	XXXX _B		
001А6Fн			.,,,,			
001А70н	DLC register 8	DLCR8	R/W	XXXX		
001А71н	ŭ					
001А72н	DLC register 9	DLCR9	R/W	XXXX _B		
001А73н						
001А74н	DLC register 10	DLCR10	R/W	XXXX _B		
001А75н	-					
001А76н	DLC register 11	DLCR11	R/W	XXXX _B		
001А77н						
001А78н	DLC register 12	DLCR12	R/W	XXXX _B		
001А79н						
001А7Ан	DLC register 13	DLCR13	R/W	XXXX _B		
001A7Вн						
001A7CH	DLC register 14	DLCR14	R/W	XXXX _B		
001A7DH						
001A7Eн	DLC register 15	DLCR15	R/W	XXXX _B		
001A7Fн 001A80н						
to	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXX _B to		
001А87н				XXXXXXXXB		



10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

lutarroot	El ² OS	Interru	pt vector	Interrupt co	ntrol register
Interrupt source	clear	Number	Address	Number	Address
Reset	N/A	# 08	FFFFDCH		
INT9 instruction	N/A	# 09	FFFFD8 _H		
Exception	N/A	# 10	FFFFD4 _H		
CAN RX	N/A	# 11	FFFFD0 _H	10000	000000
CAN TX/NS	N/A	# 12	FFFFCCH	ICR00	0000В0н
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8 _H	10004	0000004
Time Base Timer	N/A	# 14	FFFFC4 _H	ICR01	0000В1н
16-bit Reload Timer 0	*1	# 15	FFFFC0 _H	ICDOS	000000
8/10-bit A/D Converter	*1	# 16	FFFFBCH	ICR02	0000В2н
16-bit Free-run Timer	N/A	# 17	FFFFB8 _H	IODOO	000000
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4 _H	ICR03	0000ВЗн
Serial I/O	*1	# 19	FFFFB0н	ICD04	0000004
External Interrupt (INT4/INT5)	*1	# 20	FFFFACH	ICR04	0000В4н
Input Capture 0	*1	# 21	FFFFA8 _H	ICDOE	000000
8/16-bit PPG 0/1	N/A	# 22	FFFFA4 _H	ICR05	0000В5н
Output Compare 0	*1	# 23	FFFFA0 _H	ICDOC	000000
8/16-bit PPG 2/3	N/A	# 24	FFFF9C _H	ICR06	0000В6н
External Interrupt (INT6/INT7)	*1	# 25	FFFF98⊦	10007	000007
Input Capture 1	*1	# 26	FFFF94 _H	ICR07	0000В7н
8/16-bit PPG 4/5	N/A	# 27	FFFF90⊦	ICDOS	000000
Output Compare 1	*1	# 28	FFFF8C _H	ICR08	0000В8н
8/16-bit PPG 6/7	N/A	# 29	FFFF88 _H	ICDOO	000000
Input Capture 2	*1	# 30	FFFF84 _H	ICR09	0000В9н
8/16-bit PPG 8/9	N/A	# 31	FFFF80 _H	ICD40	00000
Output Compare 2	*1	# 32	FFFF7C _H	ICR10	0000ВАн
Input Capture 3	*1	# 33	FFFF78 _H	ICR11	000000
8/16-bit PPG A/B	N/A	# 34	FFFF74 _H	ICKTI	0000ВВн
Output Compare 3	*1	# 35	FFFF70⊦	ICD40	000000
16-bit Reload Timer 1	*1	# 36	FFFF6C _H	ICR12	0000ВСн
UART 0 RX	*2	# 37	FFFF68⊦	ICP42	OOODD
UART 0 TX	*1	# 38	FFFF64 _H	ICR13	0000ВDн
UART 1 RX	*2	# 39	FFFF60 _H	ICB14	0000PF
UART 1 TX	*1	# 40	FFFF5C _H	ICR14	0000ВЕн
Flash Memory	N/A	# 41	FFFF58⊦	ICD45	00000
Delayed interrupt	N/A	# 42	FFFF54 _H	ICR15	0000ВFн

^{*1:} The interrupt request flag is cleared by the El²OS interrupt clear signal.

N/A:The interrupt request flag is not cleared by the El²OS interrupt clear signal.

^{*2:} The interrupt request flag is cleared by the El²OS interrupt clear signal. A stop request is available.



11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(Vss = AVss = 0.0 V)

Parameter	Cumbal	Symbol Rating		Unit	Remarks	
Parameter	Symbol	Min	Max	Unit	Kemarks	
	Vcc	Vss - 0.3	Vss + 6.0	V		
	AVcc	Vss - 0.3	Vss + 6.0	V	Vcc = AVcc	*1
Power supply voltage	AVRH, AVRL	Vss - 0.3	Vss + 6.0	V	AVcc ≥ AVRH/L, AVRH ≥ AVRL	*1
	DVcc	Vss - 0.3	Vss + 6.0	V	Vcc ≥ DVcc	
Input voltage	Vı	Vss - 0.3	Vss + 6.0	V		*2
Output voltage	Vo	Vss - 0.3	Vss + 6.0	V		*2
Maximum Clamp Current	ICLAMP	-2.0	2.0	mA	*6	
Maximum Total Clamp Current	Σ ICLAMP	_	20	mA	*6	
"L" level Max. output current	lo _{L1}	_	15	mA	Normal output	*3
"L" level Avg. output current	lolav1	_	4	mA	Normal output, average value	*4
"L" level Max. output current	lol2	_	40	mA	High current output	*3
"L" level Avg. output current	lolav2	_	30	mA	High current output, average value	*4
"L" level Max. overall output current	∑ l ol1	_	100	mA	Total normal output	
"L" level Max. overall output current	∑lol2	_	330	mA	Total high current output	
"L" level Avg. overall output current	∑lolav1	_	50	mA	Total normal output, average value	*5
"L" level Avg. overall output current	∑lolav2	_	250	mA	Total high current output, average value	*5
"H" level Max. output current	Іон1	_	-15	mA	Normal output	*3
"H" level Avg. output current	lohav1	_	-4	mA	Normal output, average value	*4
"H" level Max. output current	Іон2	_	-40	mA	High current output	*3
"H" level Avg. output current	lohav2	_	-30	mA	High current output, average value	*4
"H" level Max. overall output current	∑Іон1	_	-100	mA	Total normal output	
"H" level Max. overall output current	∑loн2	_	-330	mA	Total high current output	
"H" level Avg. overall output current	∑ I ohav1	_	-50	mA	Total normal output, average value	*5
"H" level Avg. overall output current	∑Iohav2	_	-250	mA	Total high current output, average value	*5
Dower consumption	Pp	_	500	mW	MB90F598G	
Power consumption	PD	_	400	mW	MB90598G	
Operating temperature	TA	-40	+85	°C		
Storage temperature	Тѕтс	- 55	+150	°C		

^{*1:} AVcc, AVRH, AVRL and DVcc shall not exceed Vcc. AVRH and AVRL shall not exceed AVcc. Also, AVRL shall never exceed AVRH.

*6:

- Applicable to pins: P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

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^{*2:} VI and Vo should not exceed Vcc + 0.3V. VI should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the Iclamp rating supersedes the VI rating.

^{*3:} The maximum output current is a peak value for a corresponding pin.

^{*4:} Average output current is an average current value observed for a 100 ms period for a corresponding pin.

^{*5:} Total average current is an average current value observed for a 100 ms period for all corresponding pins.



Donomotor	Cumbal	Pin name	Condition		Value		Unit	Remarks
Parameter	Symbol	Pin name	Condition	Min	Тур	Max	Oill	Remarks
Input leak current	lı∟		Vcc = 5.5 V, Vss < Vı < Vcc	- 5	_	5	μА	
	lcc		Vcc = 5.0 V±10%, Internal frequency:		35	60	mA	MB90598G
Power supply current *	icc		16 MHz, At normal operating	_	40	60	mA	MB90F598G
	Iccs	Vcc	Vcc = 5.0 V±10%, Internal frequency: 16 MHz, At sleep	_	11	18	mA	
	Істѕ		Vcc = 5.0 V±1%, Internal frequency: 2 MHz, At timer mode	_	0.3	0.6	mA	
	Іссн		Vcc = 5.0 V±10%, At stop, T _A = 25°C	_	_	20	μА	
	Іссн2		Vcc = 5.0 V±10%, At Hardware stand-	_	_	20	μА	MB90598G
	ICCH2		by mode, T _A = 25°C	_	50	100	μА	MB90F598G



(Vcc = 5.0 V
$$\pm$$
10%, Vss = AVss = 0.0 V, T_A = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition		Value	Unit	Remarks	
Farameter	Syllibol	Fili liallie	Condition	Min	Тур	Max	Onne	Remarks
Input capacity	Cin	Other than C, AVcc, AVss, AVRH, AVRL, Vcc, Vss, DVcc, DVss, P70 to P87	_	_	5	15	pF	
		P70 to P87	_	_	15	30	pF	
Pull-up resistance	Rup	RST	_	25	50	100	kΩ	
Pull-down resistance	RDOWN	MD2	<u> </u>	25	50	100	kΩ	

^{*:} The power supply current testing conditions are when using the external clock.

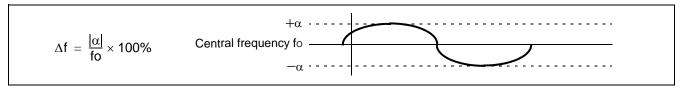
11.4 AC Characteristics

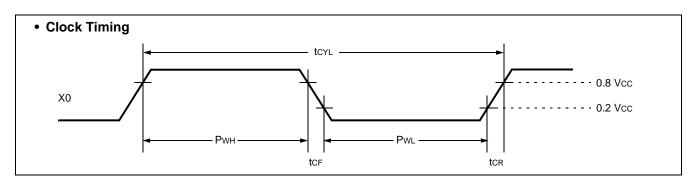
11.4.1 Clock Timing

(Vcc = 5.0 V±10%, Vss = AVss = 0.0 V, Ta = -40
$$^{\circ}\text{C}$$
 to +85 $^{\circ}\text{C})$

Parameter	neter Symbol Pin name Value			Unit	Remarks		
Parameter	Syllibol	Pili lialile	Min	Тур	Max	Onit	Remarks
Oscillation frequency	fc	X0, X1	3	_	5	MHz	When using oscillation circuit
Oscillation cycle time	tcyL	X0, X1	200	_	333	ns	When using oscillation circuit
External clock frequency	fc	X0, X1	3	_	16	MHz	When using external clock
External clock cycle time	tcyL	X0, X1	62.5	_	333	ns	When using external clock
Frequency deviation with PLL *	Δf	_	_	_	5	%	
Input clock pulse width	Pwh, PwL	X0	10	_	_	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	tcr, tcr	X0	_	_	5	ns	When using external clock
Machine clock frequency	fcp	_	1.5	_	16	MHz	
Machine clock cycle time	t CP	_	62.5	_	666	ns	
Flash Read cycle time	tcyL	_	_	2*tcp	_	ns	When Flash is accessed via CPU

^{*:} Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.







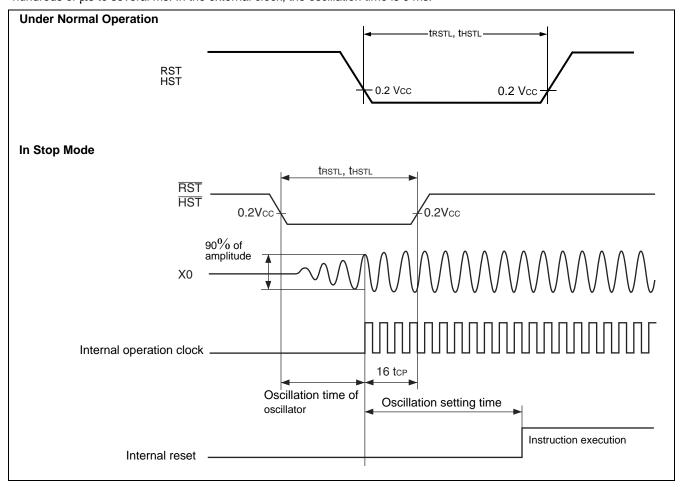
11.4.2 Reset and Hardware Standby Input

$(Vcc = 5.0 V \pm 10\%, Vss = AVss = 0.0 V, Ta = -40\%$	°C to +85	°C)
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Parameter	Symbol Pin nam		Value			Remarks
r ai ailletei	Symbol	riii iiaiiie	Min	Max	Unit	i i i i i i i i i i i i i i i i i i i
			16 tcp*1		ns	Under normal operation
Reset input time	t rstl	RST	Oscillation time of oscillator*2 + 16 tcp*1	_	ms	In stop mode
			16 tcp*1	_	ns	Under normal operation
Hardware standby input time	t HSTL	HST	Oscillation time of oscillator*2 + 16 tcp*1	_	ms	In stop mode

^{*1: &}quot;t_{cp}" represents one cycle time of the machine clock.No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

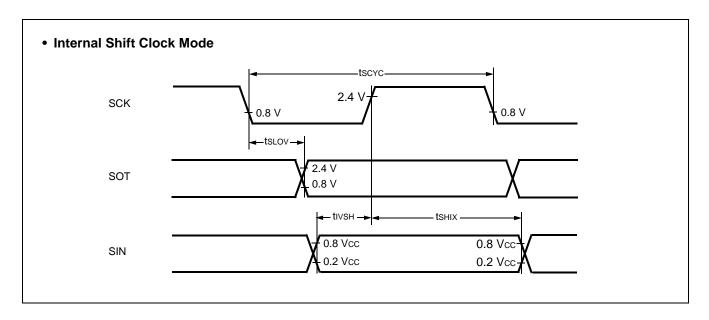




Parameter	Parameter Symbol Pin name Condi		Condition	Value		Unit	Remarks
Farameter			Condition	Min	Max	Oilit	Remarks
Serial clock "H" pulse width	t shsl	SCK0 to SCK2		4 tcp	_	ns	
Serial clock "L" pulse width	t slsh	SCK0 to SCK2		4 tcp	_	ns	
$SCK \downarrow \; \Rightarrow SOT \; delay \; time$	tsLov	SCK0 to SCK2, SOT0 to SOT2	External clock operation output pins are C _L = 80	_	150	ns	
Valid SIN ⇒ SCK ↑	tıvsн	SCK0 to SCK2, SIN0 to SIN2	pF + 1 TTL.	60	_	ns	
SCK↑ ⇒ Valid SIN hold time	tsнıx	SCK0 to SCK2, SIN0 to SIN2		60	_	ns	

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- tcp (external operation clock cycle time) : see Clock timing.





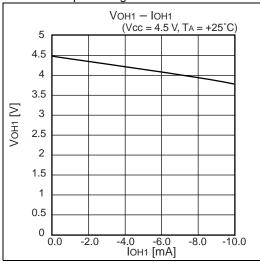
Parameter	Sym-	Pin name	Value				Remarks
Parameter	bol	Fill Hallie	Min	Тур	Max	Unit	Nemarks
Poforonco voltago rango	_	AVRH	AVRL + 3.0	_	AVcc	V	
Reference voltage range	_	AVRL	0	_	AVRH - 3.0	V	
Power supply current	lΑ	AVcc	_	5	_	mA	
Fower supply current	Іан	AVcc	_	_	5	μΑ	*
	IR	AVRH	_	400	600	μΑ	MB90V595G, MB90F598G
Reference voltage current			_	140	600	μΑ	MB90598G
	Iгн	AVRH			5	μΑ	*
Offset between input channels	_	AN0 to AN7	_	_	4	LSB	

^{*:} When not operating A/D converter, this is the current (Vcc = AVcc = AVRH = 5.0 V) when the CPU is stopped.

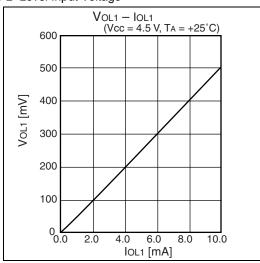


12. Example Characteristics

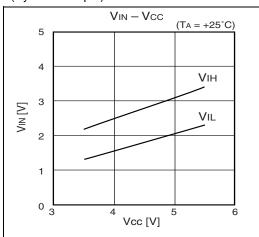
■ H" Level Output Voltage

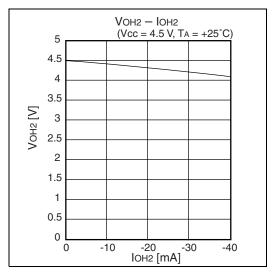


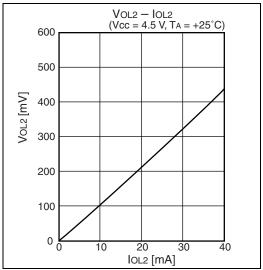
■ L" Level Input Voltage



■ H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)





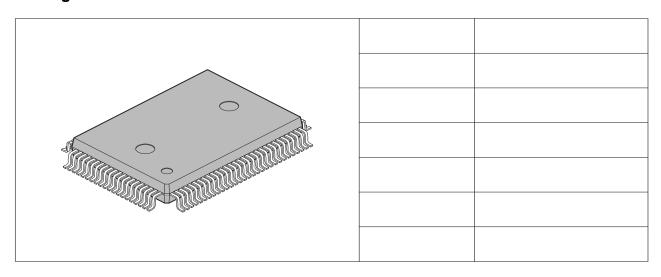


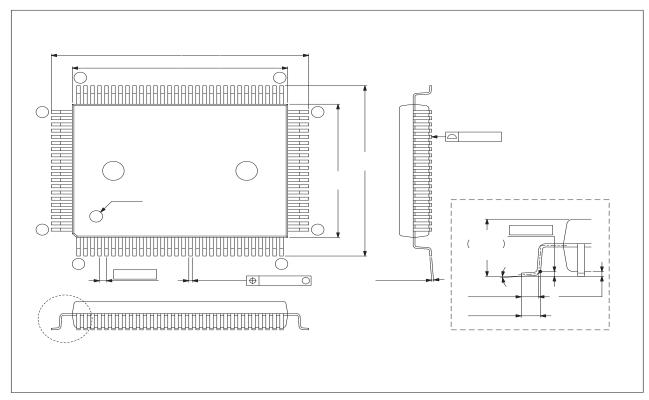


13. Ordering Information

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

14. Package Dimensions







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