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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-178e1

Contents

3. Pin Description

Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{\text{RST}}$	B	Reset input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

(5) Pull-up/down resistors
The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit
Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.
A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).
Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter
Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = DV_{CC} = V_{SS}$.

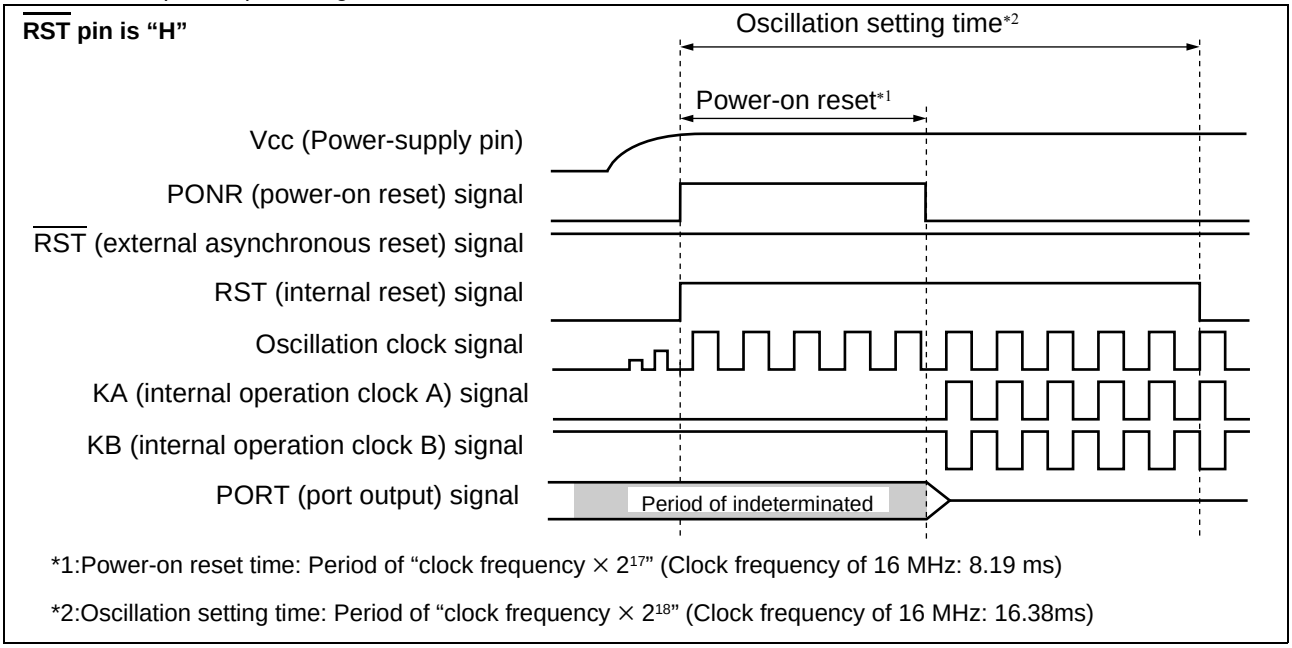
(9) N.C. Pin
The N.C. (internally connected) pin must be opened for use.

(10) Notes on Energization
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

■ If $\overline{RST}$ pin is “H”, the outputs become indeterminate.

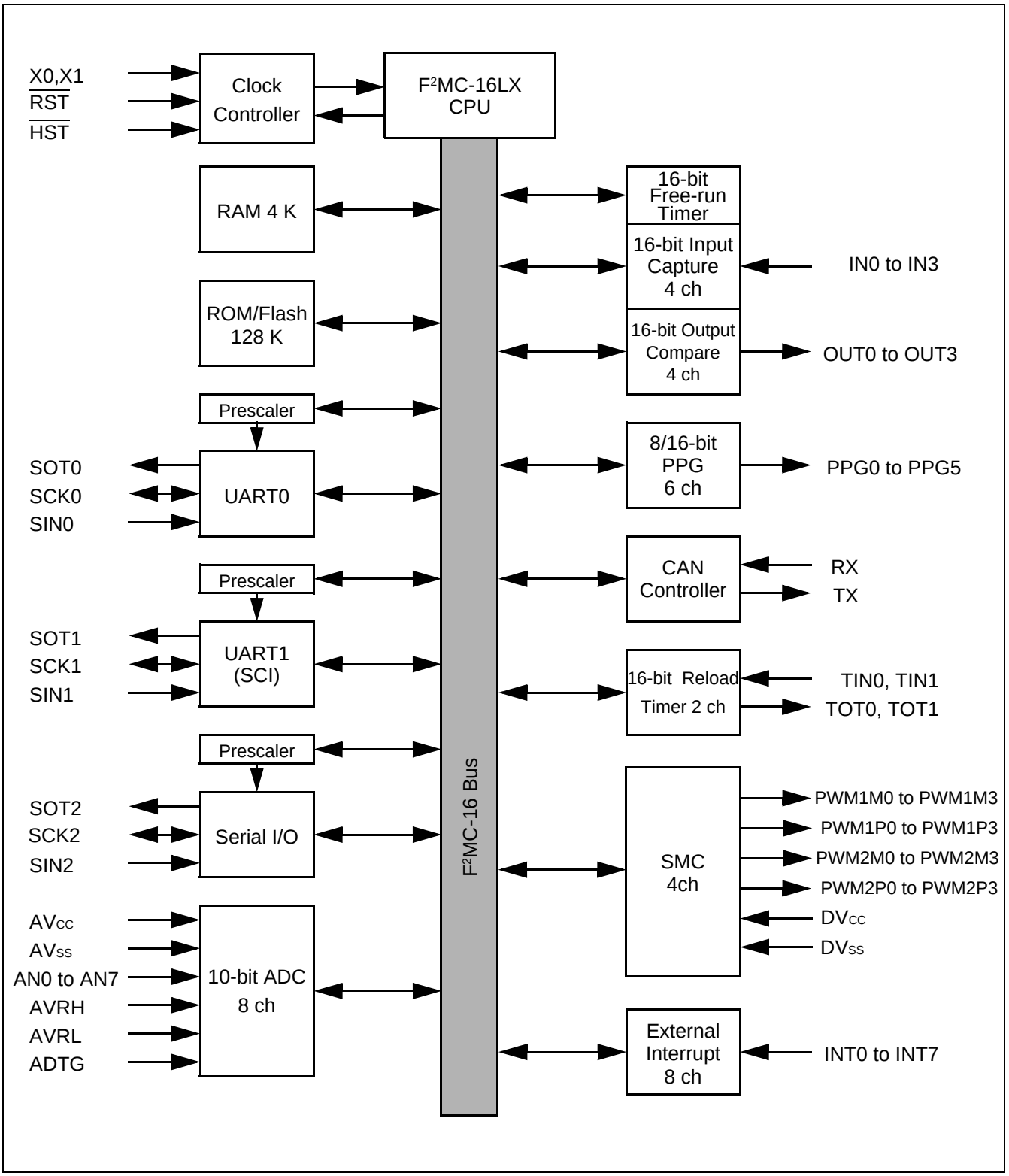
■ If $\overline{RST}$ pin is “L”, the outputs become high-impedance.
Pay attention to the port output timing shown as follows.



*1:Power-on reset time: Period of “clock frequency × 2^{17}” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × 2^{18}” (Clock frequency of 16 MHz: 16.38ms)

6. Block Diagram



Address	Register	Abbreviation	Access	Peripheral	Initial value
29H to 2AH	Reserved				
2BH	Serial IO Prescaler	SCDCR	R/W	Serial IO	0 _ _ _ 1 1 1 1B
2CH	Serial Mode Control Register (low-order)	SMCS	R/W		_ _ _ _ 0 0 0 0B
2DH	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial Data Register	SDR	R/W		XXXXXXXXB
2FH	Edge Selector	SES	R/W		_ _ _ _ _ _ _ 0B
30H	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External Interrupt Request Register	EIRR	R/W		XXXXXXXXB
32H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D Data Register 0	ADCR0	R		XXXXXXXXB
37H	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0, 1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Reserved				
3CH	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1B
3DH	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2, 3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Reserved				
40H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4, 5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Reserved				
44H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6, 7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 _ _B
47H	Reserved				
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1B
4AH	PPG8, 9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 _ _B
4BH	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
6F$_H$	ROM Mirror Function Selection Register	ROMM	R/W	ROM Mirror	_ _ _ _ _ _ _ 1$_B$
70$_H$	PWM1 Compare Register 0	PWC10	R/W	Stepping Motor Controller 0	XXXXXXXX$_B$
71$_H$	PWM2 Compare Register 0	PWC20	R/W		XXXXXXXX$_B$
72$_H$	PWM1 Select Register 0	PWS10	R/W		_ _ 0 0 0 0 0 0$_B$
73$_H$	PWM2 Select Register 0	PWS20	R/W		_ 0 0 0 0 0 0 0$_B$
74$_H$	PWM1 Compare Register 1	PWC11	R/W	Stepping Motor Controller 1	XXXXXXXX$_B$
75$_H$	PWM2 Compare Register 1	PWC21	R/W		XXXXXXXX$_B$
76$_H$	PWM1 Select Register 1	PWS11	R/W		_ _ 0 0 0 0 0 0$_B$
77$_H$	PWM2 Select Register 1	PWS21	R/W		_ 0 0 0 0 0 0 0$_B$
78$_H$	PWM1 Compare Register 2	PWC12	R/W	Stepping Motor Controller 2	XXXXXXXX$_B$
79$_H$	PWM2 Compare Register 2	PWC22	R/W		XXXXXXXX$_B$
7A$_H$	PWM1 Select Register 2	PWS12	R/W		_ _ 0 0 0 0 0 0$_B$
7B$_H$	PWM2 Select Register 2	PWS22	R/W		_ 0 0 0 0 0 0 0$_B$
7C$_H$	PWM1 Compare Register 3	PWC13	R/W	Stepping Motor Controller 3	XXXXXXXX$_B$
7D$_H$	PWM2 Compare Register 3	PWC23	R/W		XXXXXXXX$_B$
7E$_H$	PWM1 Select Register 3	PWS13	R/W		_ _ 0 0 0 0 0 0$_B$
7F$_H$	PWM2 Select Register 3	PWS23	R/W		_ 0 0 0 0 0 0 0$_B$
80$_H$ to 8F$_H$	CAN Controller. Refer to section about CAN Controller				
90$_H$ to 9D$_H$	Reserved				
9E$_H$	Program Address Detection Control Status Register	PACSR	R/W	Address Match Detection Function	0 0 0 0 0 0 0 0$_B$
9F$_H$	Delayed Interrupt/Request Register	DIRR	R/W	Delayed Interrupt	_ _ _ _ _ _ _ 0$_B$
A0$_H$	Low-Power Mode Control Register	LPMCR	R/W	Low Power Controller	0 0 0 1 1 0 0 0$_B$
A1$_H$	Clock Selection Register	CKSCR	R/W	Low Power Controller	1 1 1 1 1 1 0 0$_B$
A2$_H$ to A7$_H$	Reserved				
A8$_H$	Watchdog Timer Control Register	WDTC	R/W	Watchdog Timer	XXXXX 1 1 1$_B$
A9$_H$	Time Base Timer Control Register	TBTC	R/W	Time Base Timer	1 _ _ 0 0 1 0 0$_B$
AA$_H$ to AD$_H$	Reserved				
AE$_H$	Flash Memory Control Status Register (MB90F598G only. Otherwise reserved)	FMCS	R/W	Flash Memory	0 0 0 X 0 0 0 0$_B$
AF$_H$	Reserved				

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
$B0_H$	Interrupt Control Register 00	ICR00	R/W	Interrupt controller	00000111$_B$
$B1_H$	Interrupt Control Register 01	ICR01	R/W		00000111$_B$
$B2_H$	Interrupt Control Register 02	ICR02	R/W		00000111$_B$
$B3_H$	Interrupt Control Register 03	ICR03	R/W		00000111$_B$
$B4_H$	Interrupt Control Register 04	ICR04	R/W	Interrupt controller	00000111$_B$
$B5_H$	Interrupt Control Register 05	ICR05	R/W		00000111$_B$
$B6_H$	Interrupt Control Register 06	ICR06	R/W		00000111$_B$
$B7_H$	Interrupt Control Register 07	ICR07	R/W		00000111$_B$
$B8_H$	Interrupt Control Register 08	ICR08	R/W		00000111$_B$
$B9_H$	Interrupt Control Register 09	ICR09	R/W		00000111$_B$
BA_H	Interrupt Control Register 10	ICR10	R/W		00000111$_B$
BB_H	Interrupt Control Register 11	ICR11	R/W		00000111$_B$
BC_H	Interrupt Control Register 12	ICR12	R/W		00000111$_B$
BD_H	Interrupt Control Register 13	ICR13	R/W		00000111$_B$
BE_H	Interrupt Control Register 14	ICR14	R/W		00000111$_B$
BF_H	Interrupt Control Register 15	ICR15	R/W		00000111$_B$
$C0_H$ to FF_H	Reserved				
1900_H	Reload Register L	PRLL0	R/W	16-bit Programmable Pulse Generator 0/1	XXXXXXXX$_B$
1901_H	Reload Register H	PRLH0	R/W		XXXXXXXX$_B$
1902_H	Reload Register L	PRLL1	R/W		XXXXXXXX$_B$
1903_H	Reload Register H	PRLH1	R/W		XXXXXXXX$_B$
1904_H	Reload Register L	PRLL2	R/W	16-bit Programmable Pulse Generator 2/3	XXXXXXXX$_B$
1905_H	Reload Register H	PRLH2	R/W		XXXXXXXX$_B$
1906_H	Reload Register L	PRLL3	R/W		XXXXXXXX$_B$
1907_H	Reload Register H	PRLH3	R/W		XXXXXXXX$_B$
1908_H	Reload Register L	PRLL4	R/W	16-bit Programmable Pulse Generator 4/5	XXXXXXXX$_B$
1909_H	Reload Register H	PRLH4	R/W		XXXXXXXX$_B$
$190A_H$	Reload Register L	PRLL5	R/W		XXXXXXXX$_B$
$190B_H$	Reload Register H	PRLH5	R/W		XXXXXXXX$_B$
$190C_H$	Reload Register L	PRLL6	R/W	16-bit Programmable Pulse Generator 6/7	XXXXXXXX$_B$
$190D_H$	Reload Register H	PRLH6	R/W		XXXXXXXX$_B$
$190E_H$	Reload Register L	PRLL7	R/W		XXXXXXXX$_B$
$190F_H$	Reload Register H	PRLH7	R/W		XXXXXXXX$_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
1910H	Reload Register L	PRLL8	R/W	16-bit Programmable Pulse Generator 8/9	XXXXXXXXB
1911H	Reload Register H	PRLH8	R/W		XXXXXXXXB
1912H	Reload Register L	PRLL9	R/W		XXXXXXXXB
1913H	Reload Register H	PRLH9	R/W		XXXXXXXXB
1914H	Reload Register L	PRLLA	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1915H	Reload Register H	PRLHA	R/W		XXXXXXXXB
1916H	Reload Register L	PRLLB	R/W	16-bit Programmable Pulse Generator A/B	XXXXXXXXB
1917H	Reload Register H	PRLHB	R/W		XXXXXXXXB
1918H to 191FH	Reserved				
1920H	Input Capture Register 0 (low-order)	IPCP0	R	Input Capture 0/1	XXXXXXXXB
1921H	Input Capture Register 0 (high-order)	IPCP0	R		XXXXXXXXB
1922H	Input Capture Register 1 (low-order)	IPCP1	R		XXXXXXXXB
1923H	Input Capture Register 1 (high-order)	IPCP1	R		XXXXXXXXB
1924H	Input Capture Register 2 (low-order)	IPCP2	R	Input Capture 2/3	XXXXXXXXB
1925H	Input Capture Register 2 (high-order)	IPCP2	R		XXXXXXXXB
1926H	Input Capture Register 3 (low-order)	IPCP3	R		XXXXXXXXB
1927H	Input Capture Register 3 (high-order)	IPCP3	R		XXXXXXXXB
1928H	Output Compare Register 0 (low-order)	OCCP0	R/W	Output Compare 0/1	XXXXXXXXB
1929H	Output Compare Register 0 (high-order)	OCCP0	R/W		XXXXXXXXB
192AH	Output Compare Register 1 (low-order)	OCCP1	R/W		XXXXXXXXB
192BH	Output Compare Register 1 (high-order)	OCCP1	R/W		XXXXXXXXB

(Continued)

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Address	Register	Abbreviation	Access	Peripheral	Initial value
192C$_H$	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX$_B$
192D$_H$	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX$_B$
192E$_H$	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX$_B$
192F$_H$	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX$_B$
1930$_H$ to 19FF$_H$	Reserved				
1A00$_H$ to 1AFF$_H$	CAN Controller. Refer to section about CAN Controller				
1B00$_H$ to 1BFF$_H$	CAN Controller. Refer to section about CAN Controller				
1C00$_H$ to 1EFF$_H$	Reserved				
1FF0$_H$	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX$_B$
1FF1$_H$	Program Address Detection Register 0 (middle-order)				XXXXXXXX$_B$
1FF2$_H$	Program Address Detection Register 0 (high-order)				XXXXXXXX$_B$
1FF3$_H$	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX$_B$
1FF4$_H$	Program Address Detection Register 1 (middle-order)				XXXXXXXX$_B$
1FF5$_H$	Program Address Detection Register 1 (high-order)				XXXXXXXX$_B$
1FF6$_H$ to 1FFF$_H$	Reserved				

■ Description for Read/Write
R/W : Readable/writable
R : Read only
W : Write only

■ Description of initial value
0 : the initial value of this bit is "0".
1 : the initial value of this bit is "1".
X : the initial value of this bit is undefined.
_ : this bit is unused. the initial value is undefined.

Note: : Addresses in the range of 0000$_H$ to 00FF$_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60H	DLC register 0	DLCR0	R/W	----XXXXB
001A61H				
001A62H	DLC register 1	DLCR1	R/W	----XXXXB
001A63H				
001A64H	DLC register 2	DLCR2	R/W	----XXXXB
001A65H				
001A66H	DLC register 3	DLCR3	R/W	----XXXXB
001A67H				
001A68H	DLC register 4	DLCR4	R/W	----XXXXB
001A69H				
001A6AH	DLC register 5	DLCR5	R/W	----XXXXB
001A6BH				
001A6CH	DLC register 6	DLCR6	R/W	----XXXXB
001A6DH				
001A6EH	DLC register 7	DLCR7	R/W	----XXXXB
001A6FH				
001A70H	DLC register 8	DLCR8	R/W	----XXXX
001A71H				
001A72H	DLC register 9	DLCR9	R/W	----XXXXB
001A73H				
001A74H	DLC register 10	DLCR10	R/W	----XXXXB
001A75H				
001A76H	DLC register 11	DLCR11	R/W	----XXXXB
001A77H				
001A78H	DLC register 12	DLCR12	R/W	----XXXXB
001A79H				
001A7AH	DLC register 13	DLCR13	R/W	----XXXXB
001A7BH				
001A7CH	DLC register 14	DLCR14	R/W	----XXXXB
001A7DH				
001A7EH	DLC register 15	DLCR15	R/W	----XXXXB
001A7FH				
001A80H to 001A87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

Interrupt source	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	# 08	FFFFDC$_H$	——	——
INT9 instruction	N/A	# 09	FFFFD8$_H$	——	——
Exception	N/A	# 10	FFFFD4$_H$	——	——
CAN RX	N/A	# 11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN TX/NS	N/A	# 12	FFFFCC$_H$		
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8$_H$	ICR01	0000B1$_H$
Time Base Timer	N/A	# 14	FFFFC4$_H$		
16-bit Reload Timer 0	*1	# 15	FFFFC0$_H$	ICR02	0000B2$_H$
8/10-bit A/D Converter	*1	# 16	FFFFBC$_H$		
16-bit Free-run Timer	N/A	# 17	FFFFB8$_H$	ICR03	0000B3$_H$
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4$_H$		
Serial I/O	*1	# 19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt (INT4/INT5)	*1	# 20	FFFFAC$_H$		
Input Capture 0	*1	# 21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	# 22	FFFFA4$_H$		
Output Compare 0	*1	# 23	FFFFA0$_H$	ICR06	0000B6$_H$
8/16-bit PPG 2/3	N/A	# 24	FFFF9C$_H$		
External Interrupt (INT6/INT7)	*1	# 25	FFFF98$_H$	ICR07	0000B7$_H$
Input Capture 1	*1	# 26	FFFF94$_H$		
8/16-bit PPG 4/5	N/A	# 27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 1	*1	# 28	FFFF8C$_H$		
8/16-bit PPG 6/7	N/A	# 29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2	*1	# 30	FFFF84$_H$		
8/16-bit PPG 8/9	N/A	# 31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 2	*1	# 32	FFFF7C$_H$		
Input Capture 3	*1	# 33	FFFF78$_H$	ICR11	0000BB$_H$
8/16-bit PPG A/B	N/A	# 34	FFFF74$_H$		
Output Compare 3	*1	# 35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	# 36	FFFF6C$_H$		
UART 0 RX	*2	# 37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	# 38	FFFF64$_H$		
UART 1 RX	*2	# 39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	# 40	FFFF5C$_H$		
Flash Memory	N/A	# 41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	# 42	FFFF54$_H$		

*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

N/A:The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} − 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/L, AVRH ≥ AVRL *1
	DV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} ≥ DV_{CC}
Input voltage	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Maximum Clamp Current	I_{CLAMP}	−2.0	2.0	mA	*6
Maximum Total Clamp Current	$\sum \lvert I_{CLAMP} \rvert$	—	20	mA	*6
“L” level Max. output current	I_{OL1}	—	15	mA	Normal output *3
“L” level Avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
“L” level Max. output current	I_{OL2}	—	40	mA	High current output *3
“L” level Avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
“L” level Max. overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
“L” level Max. overall output current	$\sum I_{OL2}$	—	330	mA	Total high current output
“L” level Avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
“L” level Avg. overall output current	$\sum I_{OLAV2}$	—	250	mA	Total high current output, average value *5
“H” level Max. output current	I_{OH1}	—	−15	mA	Normal output *3
“H” level Avg. output current	I_{OHAV1}	—	−4	mA	Normal output, average value *4
“H” level Max. output current	I_{OH2}	—	−40	mA	High current output *3
“H” level Avg. output current	I_{OHAV2}	—	−30	mA	High current output, average value *4
“H” level Max. overall output current	$\sum I_{OH1}$	—	−100	mA	Total normal output
“H” level Max. overall output current	$\sum I_{OH2}$	—	−330	mA	Total high current output
“H” level Avg. overall output current	$\sum I_{OHAV1}$	—	−50	mA	Total normal output, average value *5
“H” level Avg. overall output current	$\sum I_{OHAV2}$	—	−250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F598G
		—	400	mW	MB90598G
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1: AV_{CC}, AVRH, AVRL and DV_{CC} shall not exceed V_{CC}. AVRH and AVRL shall not exceed AV_{CC}. Also, AVRL shall never exceed AVRH.

*2: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

*6:

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}		V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	
Power supply current *	I_{CC}	V_{CC}	V_{CC} = 5.0 V±10%, Internal frequency: 16 MHz, At normal operating	—	35	60	mA	MB90598G
				—	40	60	mA	MB90F598G
	I_{CCS}		V_{CC} = 5.0 V±10%, Internal frequency: 16 MHz, At sleep	—	11	18	mA	
	I_{CTS}		V_{CC} = 5.0 V±1%, Internal frequency: 2 MHz, At timer mode	—	0.3	0.6	mA	
	I_{CCH}		V_{CC} = 5.0 V±10%, At stop, T_A = 25°C	—	—	20	µA	
	I_{CCH2}		V_{CC} = 5.0 V±10%, At Hardware stand-by mode, T_A = 25°C	—	—	20	µA	MB90598G
				—	50	100	µA	MB90F598G

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input capacity	C_{IN}	Other than C, AV_{CC}, AV_{SS}, AVRH, AVRL, V_{CC}, V_{SS}, DV_{CC}, DV_{SS}, P70 to P87	—	—	5	15	pF	
		P70 to P87	—	—	15	30	pF	
Pull-up resistance	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistance	R_{DOWN}	MD2	—	25	50	100	kΩ	

* : The power supply current testing conditions are when using the external clock.

11.4 AC Characteristics

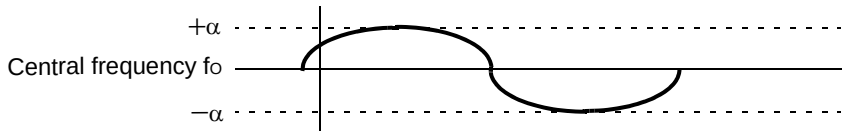
11.4.1 Clock Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

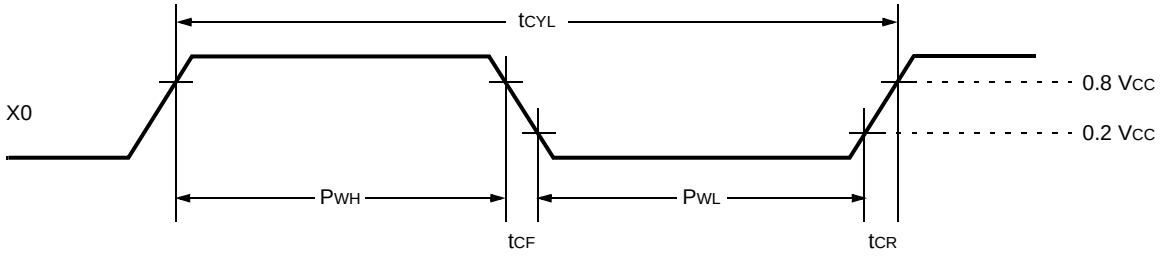
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Oscillation frequency	f_C	X0, X1	3	—	5	MHz	When using oscillation circuit
Oscillation cycle time	t_{CYL}	X0, X1	200	—	333	ns	When using oscillation circuit
External clock frequency	f_C	X0, X1	3	—	16	MHz	When using external clock
External clock cycle time	t_{CYL}	X0, X1	62.5	—	333	ns	When using external clock
Frequency deviation with PLL *	Δf	—	—	—	5	%	
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Duty ratio is about 30 to 70%.
Input clock rise and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When using external clock
Machine clock frequency	f_{CP}	—	1.5	—	16	MHz	
Machine clock cycle time	t_{CP}	—	62.5	—	666	ns	
Flash Read cycle time	t_{CYL}	—	—	2*t_{CP}	—	ns	When Flash is accessed via CPU

*: Frequency deviation indicates the maximum frequency difference from the target frequency when using a multiplied clock.

$$\Delta f = \frac{|\alpha|}{fo} \times 100\%$$



- **Clock Timing**



11.4.2 Reset and Hardware Standby Input

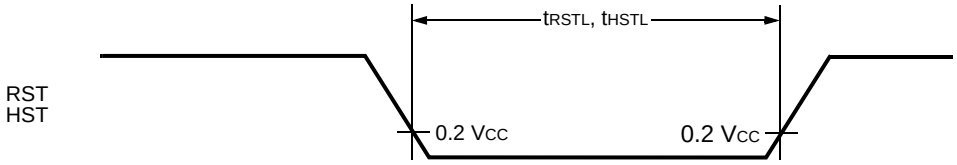
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode
Hardware standby input time	t_{HSTL}	$\overline{HST}$	16 t_{CP}*1	—	ns	Under normal operation
			Oscillation time of oscillator*2 + 16 t_{CP}*1	—	ms	In stop mode

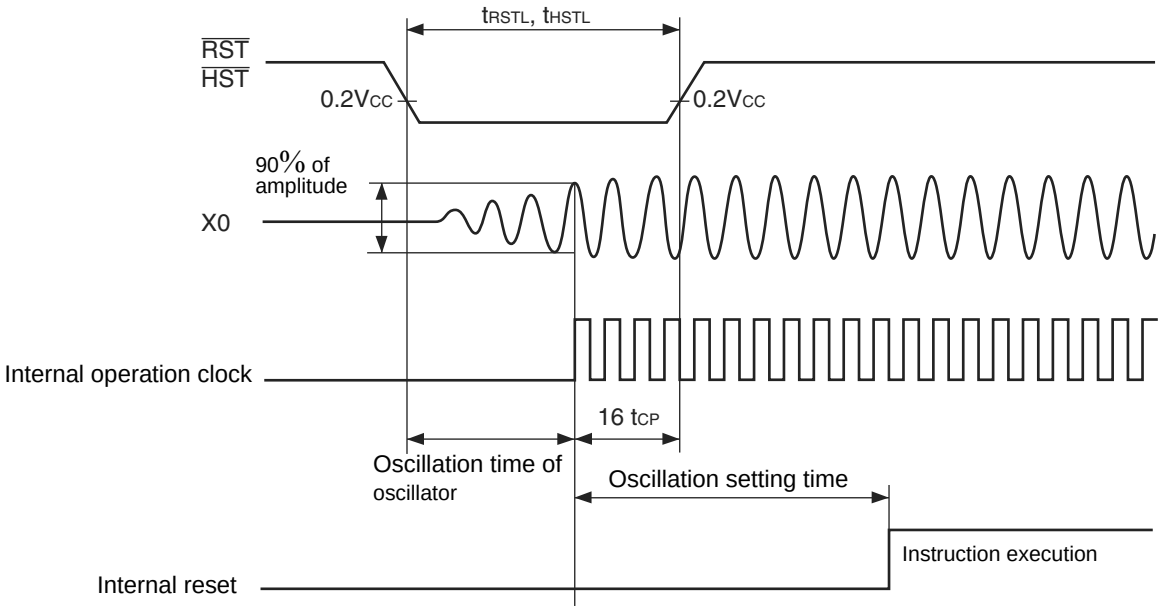
*1: "t_{cp}" represents one cycle time of the machine clock.
No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.

Under Normal Operation



In Stop Mode

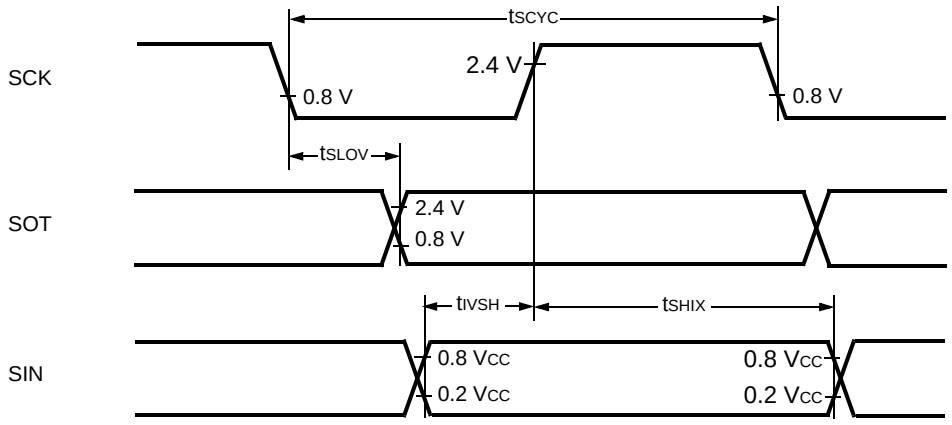


Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock “H” pulse width	t_{SHSL}	SCK0 to SCK2	External clock operation output pins are C_L = 80 pF + 1 TTL.	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0 to SCK2		4 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		—	150	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is load capacity value of pins when testing.
- t_{cp} (external operation clock cycle time) : see Clock timing.

- **Internal Shift Clock Mode**

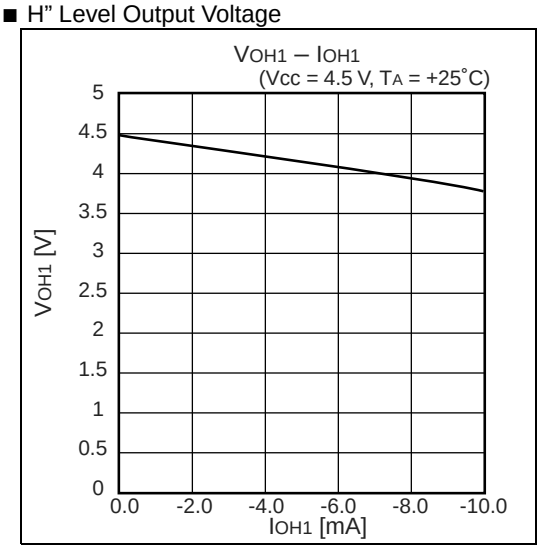


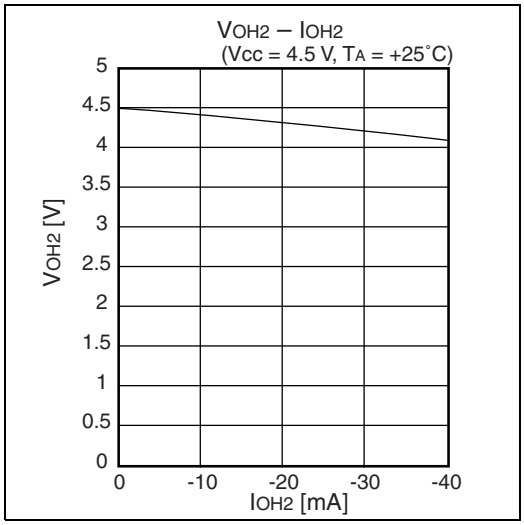
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	—	AVRH	AVRL + 3.0	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 3.0	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage current	I_R	AVRH	—	400	600	µA	MB90V595G, MB90F598G
			—	140	600	µA	MB90598G
	I_{RH}	AVRH	—	—	5	µA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

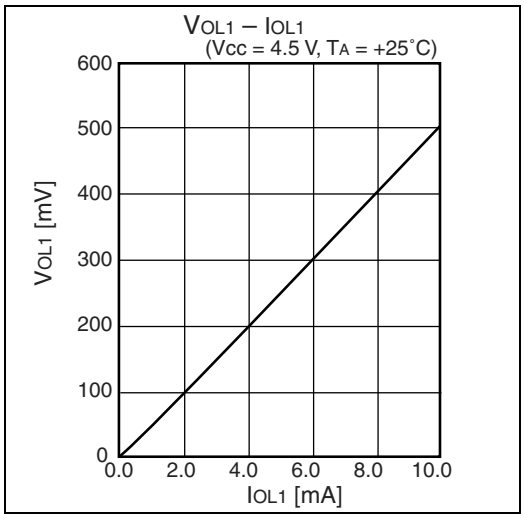
12. Example Characteristics

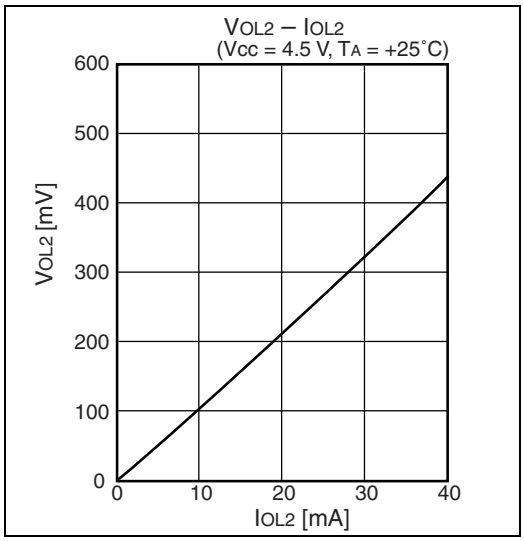
■ H" Level Output Voltage



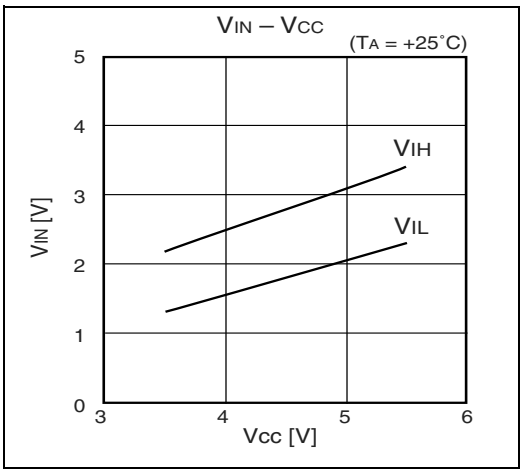


■ L" Level Input Voltage





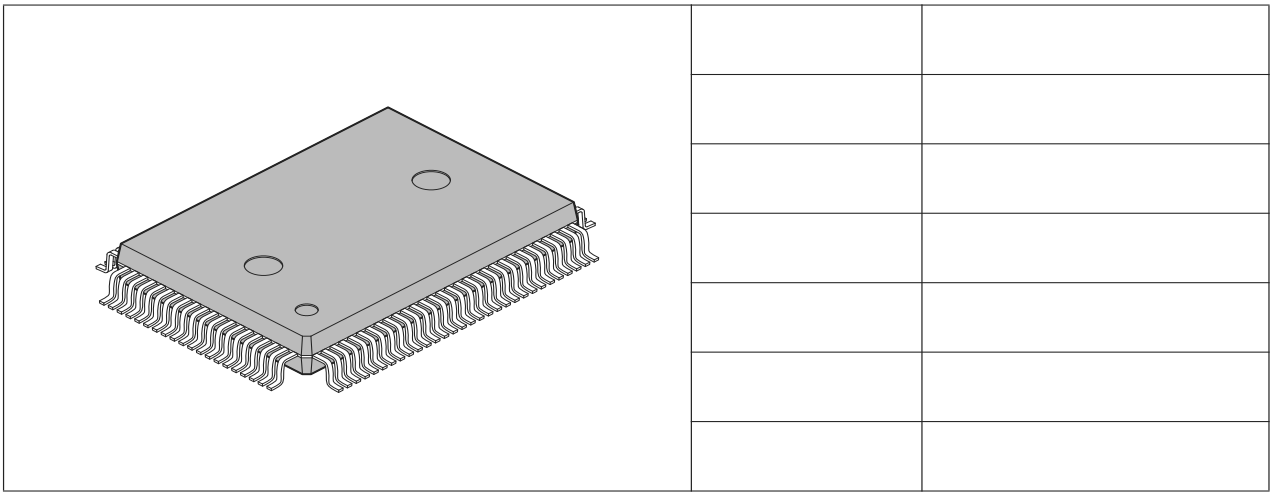
■ H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

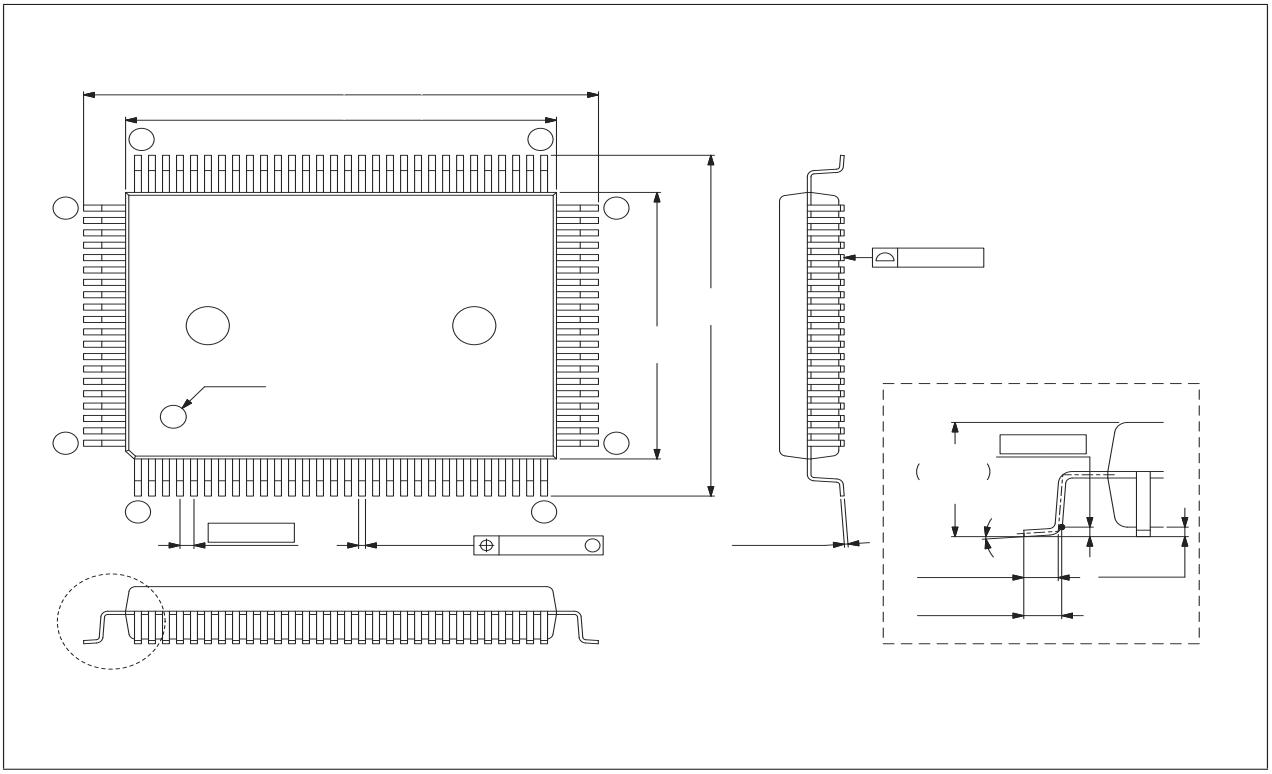


13. Ordering Information

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

14. Package Dimensions





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