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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	F ² MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-187-jne1





Contents

Pin Assignment	6
Pin Description	
1 III Description	_
I/O Circuit Type	ಶ
Handling Devices1	1
Block Diagram1	4
Memory Space1	
I/O Map10	6
Can Controller2	
List of Control Registers2	3
List of Message Buffers (ID Registers)2	
List of Message Buffers (DLC Registers and	
Data Registers) 2	7
Interrupt Source, Interrupt Vector, and Interrupt	
Control Register2	9

Electrical Characteristics	31
Absolute Maximum Ratings	31
Recommended Conditions	33
DC Characteristics	33
AC Characteristics	35
A/D Converter	42
A/D Converter Glossary	44
Notes on Using A/D Converter	45
Flash memory	46
Example Characteristics	47
Ordering Information	49
Package Dimensions	49
Major Changes	



1. Product Lineup

Features		Features MB90598G		MB90V595G		
Classific	ation	Mask ROM product Flash ROM product		Evaluation product		
ROM size		128 Kbytes	128 Kbytes Boot block Hard-wired reset vector	None		
RAM siz	е	4 Kbytes	4 Kbytes	6 Kbytes		
Emulato	r-specific power supply	-		None		
CPU fun	ctions	The number of instructions: 351 Instruction bit length: 8 bits, 16 bits Instruction length: 1 byte to 7 bytes Data bit length: 1 bit, 8 bits, 16 bits Minimum execution time: 62.5 ns (at machine Interrupt processing time: 1.5 µs (at machine co	e clock frequency of 16 MHz) clock frequency of 16 MHz, minim	num value)		
UARTO Clock synchronized transmission (500 K/1 M/2 Mbps) Clock asynchronized transmission (4808/5208/9615/10417/19230/38460/62500 /500000 bps at machine clock frequency of 16 Transmission can be performed by bi-directional serial transmission or by master/slave				ency of 16 MHz)		
UART1(SCI) Clock synchronized transmission (62.5 K/125 K/250 K/500 K/1 Mbps) Clock asynchronized transmission (1202/2404/4808/9615/31250 bps) Transmission can be performed by bi-directional serial transmission or by master/slave control or c						
Conversion precision: 8/10-bit can be selectively used. Number of inputs: 8 One-shot conversion mode (converts selected channel once only) Scan conversion mode (converts two or more successive channels and can program up to 8 channels) Continuous conversion mode (converts selected channel continuously) Stop conversion mode (converts selected channel and stop operation repeatedly)						
Number of channels: 6 (8/16-bit × 6 channels) 8/16-bit PPG timers (6 channels) Number of channels: 6 (8/16-bit × 6 channels) PPG operation of 8-bit or 16-bit A pulse wave of given intervals and given duty ratios can be output. Pulse interval: fsys, fsys/2², fsys/2³, fsys/2³, fsys/2⁴ (fsys = system clock frequency) 128μs (fosc = 4MHz: oscillation clock frequency)						
16-bit Reload timer		Number of channels: 2 Operation clock frequency: fsys/2¹, fsys/2³, fsys/2⁵ (fsys = System clock frequency) Supports External Event Count function				
16-bit	16-bit Output compares	Number of channels: 4 Pin input factor: A match signal of compare register				
I/O tim- er	Input captures	Number of channels: 4 Rewriting a register value upon a pin input (rising, falling, or both edges)				



Features	MB90598G MB90F598G MB90V595				
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90598G/F598G:TSEG2 ≥ RSJW				
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel				
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" le	evel input, or an "L" level input.			
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first				
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57 (at oscillation of 4 MHz, minimum value)	7.23 ms, 458.75 ms			
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics, Inc.				
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by				
Process	CMOS				
Power supply voltage for operation*2	+5 V±10 %				
Package	QFP-100 PGA-256				

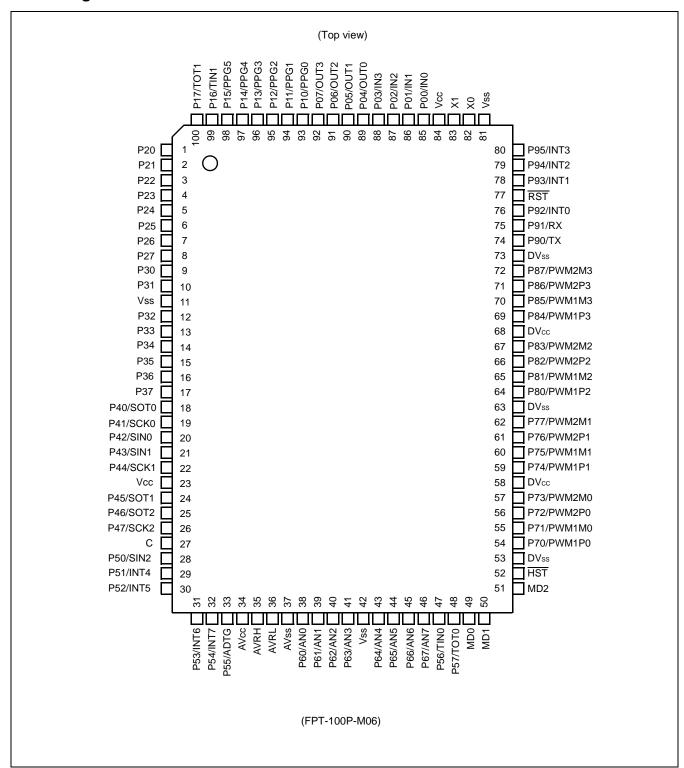
^{*1:} It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.

Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

^{*2:} Varies with conditions such as the operating frequency. (See "Electrical Characteristics.")



2. Pin Assignment





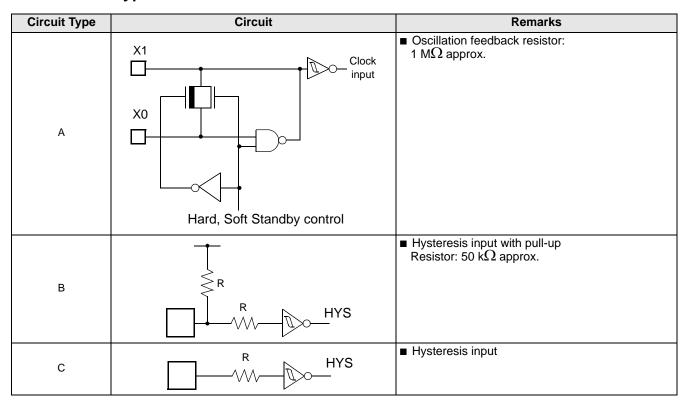
3. Pin Description

Pin no.	Pin name	Circuit type	Function			
82	X0					
83	X1	А	Oscillator pin			
77	RST	В	Reset input			
52	HST	С	Hardware standby input			
05 to 00	P00 to P03	0	General purpose IO			
85 to 88	IN0 to IN3	G	Inputs for the Input Captures			
89 to 92	P04 to P07	0	General purpose IO			
89 10 92	OUT0 to OUT3	G	Outputs for the Output Compares.			
00 to 00	P10 to P15	5	General purpose IO			
93 to 98	PPG0 to PPG5	D	Outputs for the Programmable Pulse Generators			
00	P16	5	General purpose IO			
99	TIN1	D	TIN input for the 16-bit Reload Timer 1			
400	P17	5	General purpose IO			
100	TOT1	D	TOT output for the 16-bit Reload Timer 1			
1 to 8	P20 to P27	G	General purpose IO			
9 to 10	P30 to P31	G	General purpose IO			
12 to 16	P32 to P36	G	General purpose IO			
17	P37	D	General purpose IO			
40	P40	0	General purpose IO			
18	SOT0	G	SOT output for UART 0			
40	P41	0	General purpose IO			
19	SCK0	G	SCK input/output for UART 0			
200	P42	0	General purpose IO			
20	SIN0	G	SIN input for UART 0			
04	P43	0	General purpose IO			
21	SIN1	G	SIN input for UART 1			
00	P44	0	General purpose IO			
22	SCK1	G	SCK input/output for UART 1			
P45 General purpose IO		General purpose IO				
24	SOT1	G	SOT output for UART 1			
P46 General purpose IO		General purpose IO				
25	SOT2	G	SOT output for the Serial IO			
oe.	P47		General purpose IO			
26	SCK2		SCK input/output for the Serial IO			



Pin no.	Pin name	Circuit type	Function	
76	P92	D	General purpose IO	
76	INT0		External interrupt input for INT0	
78 to 80	P93 to P95	D	General purpose IO	
78 10 80	INT1 to INT3	D	External interrupt input for INT1 to INT3	
58, 68	DVcc	_	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)	
53, 63, 73	DVss	_	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)	
34	AVcc	Power supply	Dedicated power supply pin for the A/D Converter	
37	AVss	Power supply	Dedicated ground pin for the A/D Converter	
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter	
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter	
49, 50	MD0 MD1	С	Operating mode selection input pins. These pins should be connected to Vcc or V	
51	MD2	Н	Operating mode selection input pin. This pin should be connected to Vcc or Vss.	
27	С	_	External capacitor pin. A capacitor of 0.1μF should be connected to this pin and Vss.	
23, 84	Vcc	Power supply	Power supply pins (5.0 V).	
11, 42, 81	Vss	Power supply	Ground pins (0.0 V).	

4. I/O Circuit Type





Circuit Type	Circuit	Remarks
	V	■ CMOS high current output
F	P-ch High current N-ch HYS	■ CMOS Hysteresis input
		■ CMOS output
	Vcc	■ CMOS Hysteresis input
G	P-ch N-ch R HYS R T TTL	■ TTL input (MB90F598G, only in Flash mode)
Н	R HYS	■ Hysteresis input Pull-down Resistor: 50 kΩ approx. (except MB90F598G)



(5) Pull-up/down resistors

The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit

Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.

A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs

Make sure to turn on the A/D converter power supply (AVcc, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (Vcc).

Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AVcc (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter

Connect unused pins of A/D converter to AVcc = Vcc, AVss = AVRH = DVcc = Vss.

(9) N.C. Pin

The N.C. (internally connected) pin must be opened for use.

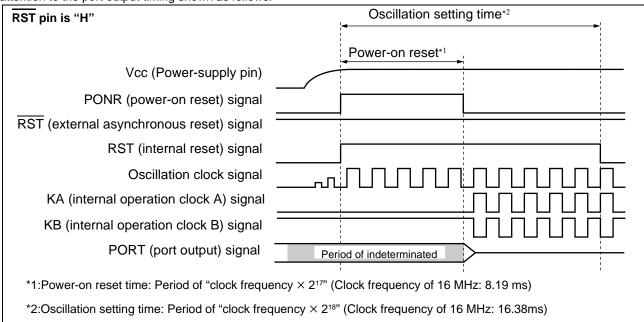
(10) Notes on Energization

To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at $50 \mu s$ or more (0.2 V to 2.7 V).

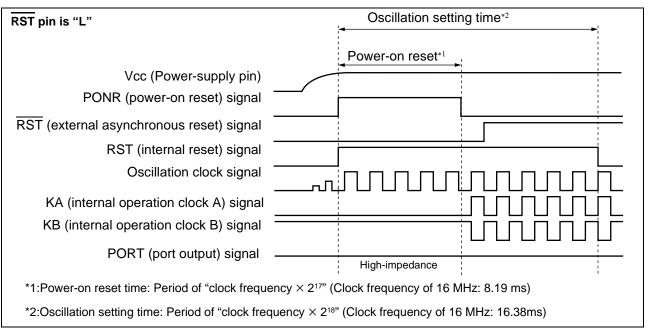
(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)

During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If RST pin is "H", the outputs become indeterminate.
- If RST pin is "L", the outputs become high-impedance. Pay attention to the port output timing shown as follows.







(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00H".

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than "00_H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

(14) Using REALOS

The use of El²OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.



8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00н	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXXB
01н	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXXB
02н	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
03н	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXXB
04н	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
05н	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
06н	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
07н	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXXB
08н	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
09н	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXB
0Ан to 0Fн		Reserv	ed		•
10н	Port 0 Direction Register	DDR0	R/W	Port 0	0 0 0 0 0 0 0 0в
11н	Port 1 Direction Register	DDR1	R/W	Port 1	0 0 0 0 0 0 0 0в
12н	Port 2 Direction Register	DDR2	R/W	Port 2	0 0 0 0 0 0 0 0в
13н	Port 3 Direction Register	DDR3	R/W	Port 3	0 0 0 0 0 0 0 0в
14н	Port 4 Direction Register	DDR4	R/W	Port 4	0 0 0 0 0 0 0 0в
15н	Port 5 Direction Register	DDR5	R/W	Port 5	0 0 0 0 0 0 0 0в
16н	Port 6 Direction Register	DDR6	R/W	Port 6	0 0 0 0 0 0 0 0в
17н	Port 7 Direction Register	DDR7	R/W	Port 7	0 0 0 0 0 0 0 0в
18н	Port 8 Direction Register	DDR8	R/W	Port 8	0 0 0 0 0 0 0 0в
19н	Port 9 Direction Register	DDR9	R/W	Port 9	000000
1Ан		Reserv	ed		
1Вн	Analog Input Enable Register	ADER	R/W	Port 6, A/D	11111111
1Сн to 1Fн		Reserv	ed		
20н	Serial Mode Control Register 0	UMC0	R/W		0 0 0 0 0 1 0 0в
21н	Serial status Register 0	USR0	R/W	UART0	0 0 0 1 0 0 0 0в
22н	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W	UARTO	XXXXXXXXB
23н	Rate and Data Register 0	URD0	R/W		0 0 0 0 0 0 0 X _B
24н	Serial Mode Register 1	SMR1	R/W		0 0 0 0 0 0 0 0в
25н	Serial Control Register 1	SCR1	R/W		0 0 0 0 0 1 0 0в
26н	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W	UART1	XXXXXXXXB
27н	Serial Status Register 1	SSR1	R/W		0 0 0 0 1 _ 0 Ов
28н	UART1 Prescaler Control Register	U1CDCR	R/W		01111в



Address	Register	Abbreviation	Access	Peripheral	Initial value			
4Сн	PPGA Operation Mode Control Register	PPGCA	R/W	16-bit	0_0001в			
4Dн	PPGB Operation Mode Control Register	PPGCB	R/W	Programmable Pulse	0_00001в			
4Ен	PPGA, B Output Pin Control Register	PPGAB	R/W	Generator A/B	0 0 0 0 0 0B			
4 Fн	Reserved							
50н	Timer Control Status Register 0	TMCSR0	R/W	16-bit	0 0 0 0 0 0 0 0в			
51н	Timer Control Status Register 0	TMCSR0	R/W		0000в			
52н	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W	Reload Timer 0	XXXXXXXXB			
53н	Timer 0/Reload Register 0	TMR0/TMRLR0	R/W		XXXXXXXX			
54н	Timer Control Status Register 1	TMCSR1	R/W		0 0 0 0 0 0 0 0 _B			
55н	Timer Control Status Register 1	TMCSR1	R/W	16-bit	0000 _B			
56н	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W	Reload Timer 1	XXXXXXXXB			
57н	Timer Register 1/Reload Register 1	TMR1/TMRLR1	R/W		XXXXXXXXB			
58н	Output Compare Control Status Register 0	OCS0	R/W	Output Compare 0/1	0 0 0 0 0 0 _B			
59н	Output Compare Control Status Register 1	OCS1	R/W		00000в			
5Ан	Output Compare Control Status Register 2	OCS2	R/W	Output Compare 2/3	0 0 0 0 0 Ов			
5Вн	Output Compare Control Status Register 3	OCS3	R/W		00000 _B			
5Сн	Input Capture Control Status Register 0/1	ICS01	R/W	Input Capture 0/1	0 0 0 0 0 0 0 0 _B			
5Dн	Input Capture Control Status Register 2/3	ICS23	R/W	Input Capture 2/3	0 0 0 0 0 0 0 0 В			
5Ен	PWM Control Register 0	PWC0	R/W	Stepping Motor Controller 0	0 0 0 0 0 Ов			
5 Fн		Reserved	•					
60н	PWM Control Register 1	PWC1	R/W	Stepping Motor Controller 1	0 0 0 0 0 0в			
61н		Reserved						
62н	PWM Control Register 2	PWC2	R/W	Stepping Motor Controller 2	0 0 0 0 0 0в			
63н		Reserved						
64н	PWM Control Register 3	PWC3	R/W	Stepping Motor Controller 3	0 0 0 0 0 0в			
65н		Reserved		<u>'</u>				
66н	Timer Data Register (low-order)	TCDT	R/W		0 0 0 0 0 0 0 0 _B			
67н	Timer Data Register (high-order)	TCDT	R/W	16-bit Free-run Timer	0 0 0 0 0 0 0 0 _B			
68н	Timer Control Status Register	TCCS	R/W		0 0 0 0 0 0 0 0 _B			
69н to 6Eн	Reserved							



Address	Register	Abbreviation	Access	Peripheral	Initial value
ВОн	Interrupt Control Register 00	ICR00	R/W		00000111в
В1н	Interrupt Control Register 01	ICR01	R/W	latamont acatallan	00000111в
В2н	Interrupt Control Register 02	ICR02	R/W	Interrupt controller	00000111в
ВЗн	Interrupt Control Register 03	ICR03	R/W		00000111в
В4н	Interrupt Control Register 04	ICR04	R/W		00000111в
В5н	Interrupt Control Register 05	ICR05	R/W		00000111в
В6н	Interrupt Control Register 06	ICR06	R/W		00000111в
В7н	Interrupt Control Register 07	ICR07	R/W		00000111в
В8н	Interrupt Control Register 08	ICR08	R/W		00000111в
В9н	Interrupt Control Register 09	ICR09	R/W	latamont acatallan	00000111в
ВАн	Interrupt Control Register 10	ICR10	R/W	Interrupt controller	00000111в
ВВн	Interrupt Control Register 11	ICR11	R/W		00000111В
ВСн	Interrupt Control Register 12	ICR12	R/W		00000111В
ВОн	Interrupt Control Register 13	ICR13	R/W		00000111В
ВЕн	Interrupt Control Register 14	ICR14	R/W		00000111В
ВГн	Interrupt Control Register 15	ICR15	R/W		00000111В
C0н to FFн		Resei	ved		
1900н	Reload Register L	PRLL0	R/W		XXXXXXXXB
1901н	Reload Register H	PRLH0	R/W	16-bit Programmable Pulse	XXXXXXXXB
1902н	Reload Register L	PRLL1	R/W	Generator 0/1	XXXXXXXXB
1903н	Reload Register H	PRLH1	R/W		XXXXXXXXB
1904н	Reload Register L	PRLL2	R/W		XXXXXXXXB
1905н	Reload Register H	PRLH2	R/W	16-bit Programmable Pulse	XXXXXXXXB
1906н	Reload Register L	PRLL3	R/W	Generator 2/3	XXXXXXXXB
1907н	Reload Register H	PRLH3	R/W		XXXXXXXXB
1908н	Reload Register L	PRLL4	R/W		XXXXXXXXB
1909н	Reload Register H	PRLH4	R/W	16-bit Programmable	XXXXXXXXB
190Ан	Reload Register L	PRLL5	R/W	Pulse Generator 4/5	XXXXXXXXB
190Вн	Reload Register H	PRLH5	R/W		XXXXXXXXB
190Сн	Reload Register L	PRLL6	R/W		XXXXXXXXB
190Он	Reload Register H	PRLH6	R/W	16-bit Programmable Pulse	XXXXXXXXB
190Ен	Reload Register L	PRLL7	R/W	Generator 6/7	XXXXXXXXB
190Гн	Reload Register H	PRLH7	R/W		XXXXXXXX



Address	Register	Abbreviation	Access	Initial Value
001А40н				
001А41н	IB verietes 0	IDDo	DAM	XXXXXXXX XXXXXXXXB
001А42н	ID register 8	IDR8	R/W	VVVV VVVVVV
001А43н				XXXXX XXXXXXXXB
001А44н				· · · · · · · · · · · · · · · · · · ·
001А45н	ID register 0	IDDO	D/M	XXXXXXX XXXXXXXXB
001А46н	ID register 9	IDR9	R/W	VVVV VVVVVVV
001А47н				XXXXX XXXXXXXXB
001А48н				· · · · · · · · · · · · · · · · · · ·
001А49н	ID register 10	IDR10	R/W	XXXXXXX XXXXXXXXB
001А4Ан	- ID register 10	IDRIU	K/VV	VVVV VVVVVV-
001А4Вн				XXXXX XXXXXXXXB
001А4Сн				XXXXXXX XXXXXXX
001А4Dн	ID register 11	IDR11	R/W	AAAAAAA AAAAAAAB
001А4Ен	ID register 11	IDKII		XXXXX XXXXXXXXB
001А4Гн				VVVV VVVVVVV
001А50н			R/W	VVVVVVV VVVVVV-
001А51н	ID register 12	IDR12		XXXXXXXX XXXXXXXB
001А52н	To register 12	IDINIZ	10,00	XXXXX XXXXXXXXB
001А53н				XXXX XXXXXXXB
001А54н				XXXXXXXX XXXXXXXX
001А55н	ID register 13	IDR13	R/W	AAAAAAAAAAAAAA
001А56н	Tograter To	IDICIO		XXXXX XXXXXXXXB
001А57н				WWW WWWWW
001А58н				XXXXXXX XXXXXXX
001А59н	ID register 14	IDR14	R/W	,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,,
001А5Ан		ISIN'I	1.7/44	XXXXX XXXXXXXXB
001А5Вн				70000 7000000B
001А5Сн				XXXXXXX XXXXXXX
001А5Дн	ID register 15	IDR15	R/W	70000007000000000000000000000000000000
001А5Ен	15 15910101 10	IDI(10	17/44	XXXXX XXXXXXXXB
001А5Гн				70000 70000000



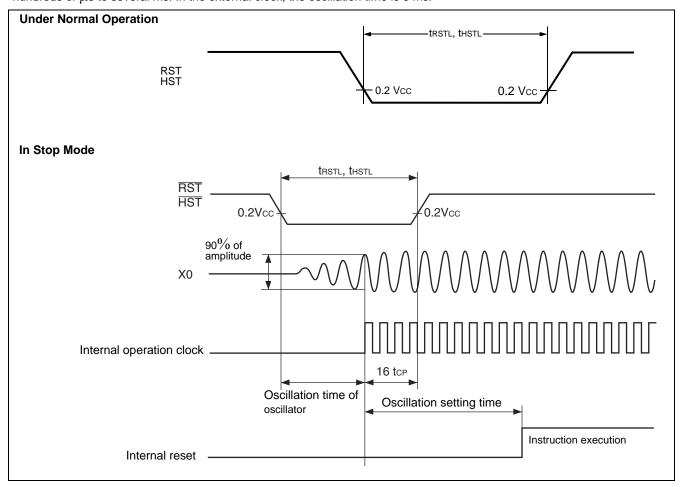
11.4.2 Reset and Hardware Standby Input

$(Vcc = 5.0 V \pm 10\%, Vss = AVss = 0.0 V, Ta = -40\%$	°C to +85	°C)
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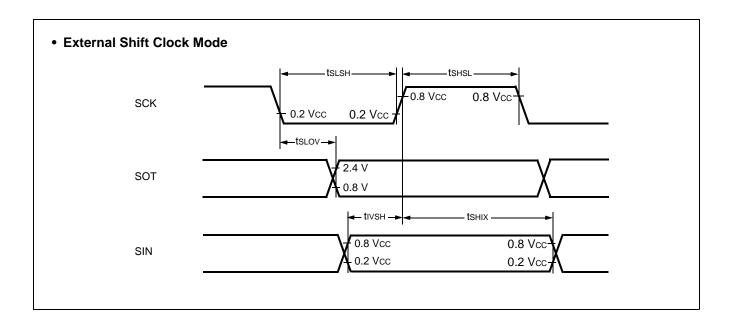
Parameter	Symbol	Pin name	Value		Unit	Remarks	
r ai ailletei	Symbol	Min Max		Oilit	Keniarks		
	t RSTL			16 tcp*1		ns	Under normal operation
Reset input time		RST	Oscillation time of oscillator*2 + 16 tcp*1	_	ms	In stop mode	
			16 tcp*1	_	ns	Under normal operation	
Hardware standby input time	t HSTL	HST		In stop mode			

^{*1: &}quot;t_{cp}" represents one cycle time of the machine clock.No reset can fully initialize the Flash Memory if it is performing the automatic algorithm.

*2: Oscillation time of oscillator is time that the amplitude reached the 90%.
In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of μs to several ms. In the external clock, the oscillation time is 0 ms.



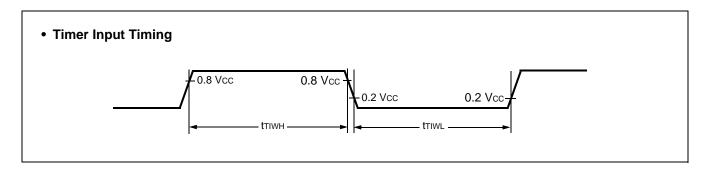




(5) Timer Input Timing

 $(Vcc = 5.0 V \pm 10\%, Vss = AVss = 0.0 V, T_A = -40 ^{\circ}C to +85 ^{\circ}C)$

Parameter	Symbol Pin name		Condition	Va	lue	Unit	Remarks
raiailletei	Зупівої	or Fin name Condition —	Min	Max	Oiiit	iveillat ka	
Input pulse width	t тıwн	TIN0, TIN1		4 tcp	_	ns	
input puise width	t⊤ıw∟	IN0 to IN3	_	4 ICP		115	

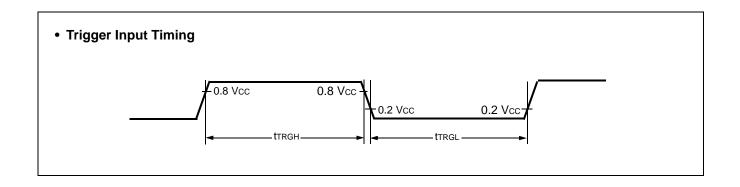


11.4.5 Trigger Input Timing

(Vcc = 5.0 V \pm 10%, Vss = AVss = 0.0 V, Ta = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Val	lue	Unit	Remarks	
raiailletei	Syllibol	Fill Hallie	Condition	Min		Offic	Nemarks	
Input pulse width	t trgh	INT0 to INT7,	_	5 tcp	_	ns	Under normal operation	
	input puise width	t TRGL	ADTG	_	1	_	μs	In stop mode

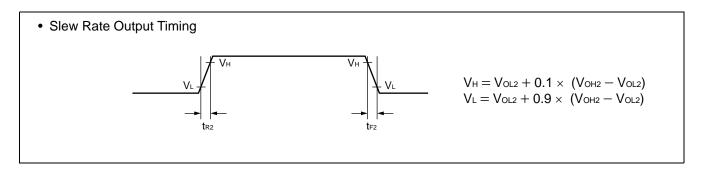




11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)

 $(V_{CC} = 5.0 \text{ V} \pm 10 \text{ %, Vss} = \text{AVss} = 0.0 \text{ V, T}_{A} = -40 ^{\circ}\text{C to } +85 ^{\circ}\text{C})$

Parameter	Symbol	Pin name	Condition		Value		Unit	Remarks
Farameter	Syllibol	riii iiaiiie	Condition	Min	Тур	Max	Oilit	i\ciliai k3
Output Rise/Fall time	t _{R2} Port P70 to P77, t _{F2} Port P80 to P87		_	15	40	150	ns	



11.5 A/D Converter

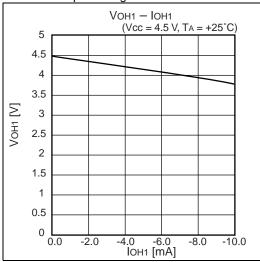
(Vcc = AVcc = 5.0 V±10%, Vss = AVss = 0.0 V,3.0 V \leq AVRH - AVRL, T_A = -40 $^{\circ}$ C to +85 $^{\circ}$ C)

Parameter	Sym-	Pin name	Value			Unit	Remarks
Parameter	bol	Pili lialile	Min	Тур	Max	Onn	Remarks
Resolution	_	_	_		10	bit	
Conversion error	_	_	_	_	±5.0	LSB	
Nonlinearity error	_	_	_	_	±2.5	LSB	
Differential linearity error	_	_	_	_	±1.9	LSB	
Zero transition voltage	Vот	AN0 to AN7	AVRL — 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	V _{FST}	AN0 to AN7	AVRH – 6.5 LSB	AVRH – 1.5 LSB	AVRH + 1.5 LSB	V	
Conversion time	_	_	_	352tcp	_	ns	
Sampling time	_	_	_	64tcp	_	ns	
Analog port input current	Iain	AN0 to AN7	-10	_	10	μА	
Analog input voltage range	VAIN	AN0 to AN7	AVRL	_	AVRH	V	

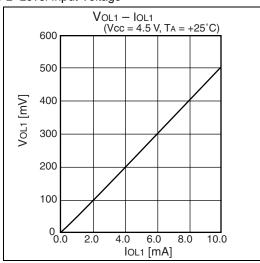


12. Example Characteristics

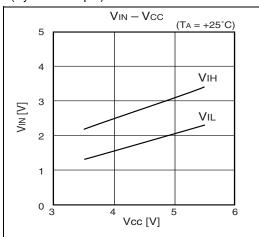
■ H" Level Output Voltage

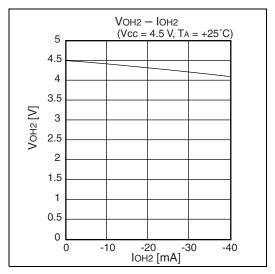


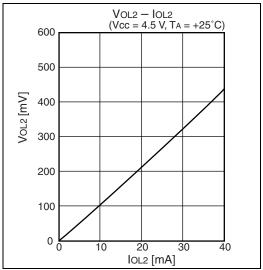
■ L" Level Input Voltage



■ H" Level Input Voltage/"L" Level Input Voltage (Hysteresis Input)

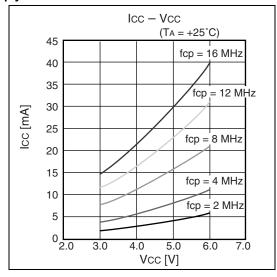


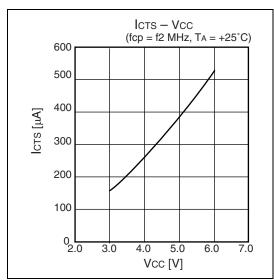


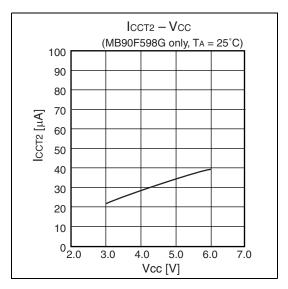


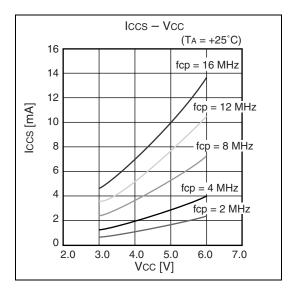


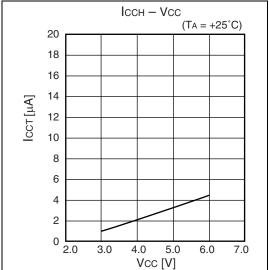
Supply Current













15. Major Changes

Spansion Publication Number: DS07-13705-7E

Section	Change Results
_	Deleted the old products, MB90598, MB90F598, and MB90V595.
_	Changed the series name; MB90595/595G series ? MB90595G series
_	Changed the following erroneous name. I/O timer → 16-bit Free-run Timer
PRODUCT LINEUP	One of Standby mode name is changed. Clock mode → Watch mode
I/O CIRCUIT TYPE	Changed Pull-down resistor value of circuit type H.
ELECTRICAL CHARACTERISTICS AC Characteristics	Add the "External clock input" and "Flash Read cycle time" in (1) Clock Timing
	Figure in (2) Reset and Hardware Standby Input RST/HST input level of "In Stop Mode" is changed. 0.6 Vcc 0.2 Vcc
ELECTRICAL CHARACTERISTICS 5. A/D Converter	Changed the items of "Zero transition voltage" and "Full scale transition voltage".

NOTE: Please see "Document History" about later revised information.

Document History

	Document Title: MB90598G/F598G/V595G F ² MC-16LX MB90595G Series CMOS 16-bit Proprietary Microcontroller Document Number: 002-07700								
Revision	ECN	Orig. of Change	Submission Date	Description of Change					
**	_	AKIH	09/26/2008	Migrated to Cypress and assigned document number 002-07700. No change to document contents or format.					
*A	5537128	AKIH	11/30/2016	Updated to Cypress template					

Document Number: 002-07700 Rev. *A Page 50 of 51



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Document Number: 002-07700 Rev. *A Revised November 30, 2016 Page 51 of 51