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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

### Details

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Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-192e1

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Features	MB90598G	MB90F598G	MB90V595G		
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90598G/F598G:TSEG2 ≥ RSJW				
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel				
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" le	evel input, or an "L" level input.			
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first				
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)				
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics, Inc.				
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by				
Process		CMOS			
Power supply voltage for opera- tion*2	+5 V±10 %				
Package	QFP-100		PGA-256		

\*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.

Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

\*2: Varies with conditions such as the operating frequency. (See "Electrical Characteristics.")



# 2. Pin Assignment





# 3. Pin Description

Pin no.	Pin name	Circuit type	Function			
82	X0	٨				
83	X1	A				
77	RST	В	Reset input			
52	HST	С	Hardware standby input			
95 to 99	P00 to P03	G	General purpose IO			
05 10 00	IN0 to IN3	G	Inputs for the Input Captures			
90 to 02	P04 to P07	C	General purpose IO			
09 10 92	OUT0 to OUT3	G	Outputs for the Output Compares.			
02 to 08	P10 to P15	P	General purpose IO			
93 10 96	PPG0 to PPG5		Outputs for the Programmable Pulse Generators			
00	P16	P	General purpose IO			
99	TIN1		TIN input for the 16-bit Reload Timer 1			
400	P17	P	General purpose IO			
100	TOT1		TOT output for the 16-bit Reload Timer 1			
1 to 8	P20 to P27	G	General purpose IO			
9 to 10	P30 to P31	G	General purpose IO			
12 to 16	P32 to P36	G	General purpose IO			
17	P37	D	General purpose IO			
P40		6	General purpose IO			
18 SOT0		G	SOT output for UART 0			
10	P41		General purpose IO			
19	SCK0	G	SCK input/output for UART 0			
00	P42	6	General purpose IO			
20	SIN0	G	SIN input for UART 0			
04	P43	6	General purpose IO			
21	SIN1	G	SIN input for UART 1			
	P44	6	General purpose IO			
22	SCK1	G	SCK input/output for UART 1			
04	P45	6	General purpose IO			
24	SOT1	G	SOT output for UART 1			
05	P46	6	General purpose IO			
25	SOT2	G	SOT output for the Serial IO			
	P47	â	General purpose IO			
20	SCK2	G	SCK input/output for the Serial IO			



Pin no.	Pin name	Circuit type	Function
76	P92	D	General purpose IO
70	INT0		External interrupt input for INT0
79 to 90	P93 to P95	D	General purpose IO
70 10 00	INT1 to INT3		External interrupt input for INT1 to INT3
58, 68	DVcc	_	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DVss	-	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AVcc	Power supply	Dedicated power supply pin for the A/D Converter
37	AVss	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter
49, 50	MD0 MD1	С	Operating mode selection input pins. These pins should be connected to $V_{\mbox{\scriptsize CC}}$ or $V_{\mbox{\scriptsize SS}}.$
51	MD2	н	Operating mode selection input pin. This pin should be connected to $V_{\mbox{\scriptsize CC}}$ or $V_{\mbox{\scriptsize SS}}.$
27	С	_	External capacitor pin. A capacitor of $0.1 \mu F$ should be connected to this pin and $V_{\mbox{\scriptsize SS}}.$
23, 84	Vcc	Power supply	Power supply pins (5.0 V).
11, 42, 81	Vss	Power supply	Ground pins (0.0 V).

# 4. I/O Circuit Type







Circuit Type	Circuit	Remarks		
		CMOS high current output		
		CMOS Hysteresis input		
	P-ch			
	High current			
F	N-ch			
	R			
	L <sub>VV</sub> ,T <sub>D</sub> HYS			
		CMOS output		
		CMOS Hysteresis input		
	P-ch	■ TTL input		
		(MB90F598G, only in Flash mode)		
G				
	R			
		■ Hysteresis input Pull down Resister: 50 kΩ approx		
	R HYS	(except MB90F598G)		
н	$\square \rightarrow_{R} \square$			
	$\geq$			
	, , ,			
		1		



# 8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00н	Port 0 Data Register	PDR0	R/W	Port 0	XXXXXXXXB
01н	Port 1 Data Register	PDR1	R/W	Port 1	XXXXXXXXB
02н	Port 2 Data Register	PDR2	R/W	Port 2	XXXXXXXXB
03н	Port 3 Data Register	PDR3	R/W	Port 3	XXXXXXXXB
04н	Port 4 Data Register	PDR4	R/W	Port 4	XXXXXXXXB
05н	Port 5 Data Register	PDR5	R/W	Port 5	XXXXXXXXB
06н	Port 6 Data Register	PDR6	R/W	Port 6	XXXXXXXXB
07н	Port 7 Data Register	PDR7	R/W	Port 7	XXXXXXXXB
08н	Port 8 Data Register	PDR8	R/W	Port 8	XXXXXXXXB
09н	Port 9 Data Register	PDR9	R/W	Port 9	XXXXXXB
0Ан to 0Fн		Reserv	ed		•
10н	Port 0 Direction Register	DDR0	R/W	Port 0	00000000
11н	Port 1 Direction Register	DDR1	R/W	Port 1	00000000
12н	Port 2 Direction Register	DDR2	R/W	Port 2	00000000
13н	Port 3 Direction Register	DDR3	R/W	Port 3	00000000
14н	Port 4 Direction Register	DDR4	R/W	Port 4	00000000
15н	Port 5 Direction Register	DDR5	R/W	Port 5	00000000
16н	Port 6 Direction Register	DDR6	R/W	Port 6	00000000
17н	Port 7 Direction Register	DDR7	R/W	Port 7	00000000
18 <sub>H</sub>	Port 8 Direction Register	DDR8	R/W	Port 8	00000000
19н	Port 9 Direction Register	DDR9	R/W	Port 9	000000в
1Ан		Reserv	ed	·	·
1Bн	Analog Input Enable Register	ADER	R/W	Port 6, A/D	1 1 1 1 1 1 1 1 <sub>B</sub>
1Cн to 1Fн		Reserv	ed	·	·
20н	Serial Mode Control Register 0	UMC0	R/W		00000100в
21н	Serial status Register 0	USR0	R/W		0001000в
22н	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W	UARTU	XXXXXXXXB
23н	Rate and Data Register 0	URD0	R/W		000000Хв
24н	Serial Mode Register 1	SMR1	R/W		00000000
25н	Serial Control Register 1	SCR1	R/W		00000100в
26н	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W	UART1	XXXXXXXXB
27н	Serial Status Register 1	SSR1	R/W		00001_00в
28н	UART1 Prescaler Control Register	U1CDCR	R/W		01111в

(Continued)



Address	Register	Abbreviation	Access	Peripheral	Initial value
29н to 2Ан		Reserved			
2Вн	Serial IO Prescaler	SCDCR	R/W		01111в
2Сн	Serial Mode Control Register (low-order)	SMCS	R/W		0000в
2Dн	Serial Mode Control Register (high-order)	SMCS	R/W	Serial IO	00000010в
2Ен	Serial Data Register	SDR	R/W		XXXXXXXXB
2 <b>F</b> н	Edge Selector	SES	R/W		0в
30н	External Interrupt Enable Register	ENIR	R/W		00000000
31н	External Interrupt Request Register	EIRR	R/W	External Interrupt	XXXXXXXXB
32н	External Interrupt Level Register	ELVR	R/W	External interrupt	00000000
33н	External Interrupt Level Register	ELVR	R/W		000000000
34н	A/D Control Status Register 0	ADCS0	R/W		00000000
35н	A/D Control Status Register 1	ADCS1	R/W	A/D Convertor	00000000
36н	A/D Data Register 0	ADCR0	R	A/D Conventer	XXXXXXXXB
37н	A/D Data Register 1	ADCR1	R/W		00001_XXв
38н	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable	0_000_1в
39н	PPG1 Operation Mode Control Register	PPGC1	R/W	Pulse	0_00001в
ЗАн	PPG0, 1 Output Pin Control Register	PPG01	R/W	Generator 0/1	000000B
3Вн		Reserved			
3Сн	PPG2 Operation Mode Control Register	PPGC2	R/W	16-hit Programmable	0_000_1в
3Dн	PPG3 Operation Mode Control Register	PPGC3	R/W	Pulse	0_00001в
3Ен	PPG2, 3 Output Pin Control Register	PPG23	R/W	Generator 2/3	00000в
3Fн		Reserved			
40н	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable	0_000_1в
41н	PPG5 Operation Mode Control Register	PPGC5	R/W	Pulse	0_00001в
42н	PPG4, 5 Output Pin Control Register	PPG45	R/W	Generator 4/5	000000в
43 <sub>H</sub>		Reserved		1	1
44 <sub>H</sub>	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable	0_000_1в
45 <sub>H</sub>	PPG7 Operation Mode Control Register	PPGC7	R/W	Pulse	0_00001в
<b>46</b> H	PPG6, 7 Output Pin Control Register	PPG67	R/W	Generator 6/7	00000в
<b>47</b> H		Reserved		1	1
48 <sub>H</sub>	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable	0_000_1в
<b>49</b> H	PPG9 Operation Mode Control Register	PPGC9	R/W	Pulse	0_00001в
<b>4</b> Ан	PPG8, 9 Output Pin Control Register	PPG89	R/W	Generator 8/9	000000в
4B⊦		Reserved	<u> </u>	1	



Address	Register	Abbreviation	Access	Initial Value	
001B08 <sub>H</sub>	IDE register	IDEP	D/M		
001B09н		IDER			
001В0Ан	Transmit RTR register	TPTPP	P/M		
001B0Bн				0000000 000000B	
001B0Cн	Romoto framo roceivo waiting register		D/M		
001B0DH	Kemole frame receive walling register	REWIR	r./ vv	~~~~~~~~~~~~~~~	
001B0Eн	Transmit interrupt anable register	TIED	D/M/	0000000 0000000-	
001B0Fн		HER	r./ vv	0000000 00000008	
001B10н			R/W		
001B11н					
001B12н	Acceptance mask select register	AIVISK			
001B13н					
001B14н					
001B15н			DAA	ΑΛΛΑΛΑΑΑ ΑΛΑΛΑΑΑΒ	
001B16н	Acceptance mask register 0	AWRU	R/VV		
001B17н	]			~~~~~ ~~~~~	
001B18н					
001B19н			5.44		
001В1Ан	Acceptance mask register 1	AMR1	K/VV		
001B1Bн	1			ΛΛΛΛΛ ΛΛΛΛΛΛΛΧΧΒ	

# 9.2 List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
001A00н to 001A1Fн	General-purpose RAM		R/W	XXXXXXXB to XXXXXXXB
001А20н				XXXXXXXX XXXXXXXx
001A21н	ID register 0		R/M	
001A22н		ibito		XXXXX XXXXXXXXx
001А23н				~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
001A24н			D/M	XXXXXXXX XXXXXXXB
001A25н	ID register 1	IDR1 R/W		
001А26н			XXXXX XXXXXXXXx	
001A27н				
001A28н				XXXXXXXX XXXXXXXx
001A29н	ID register 2	IDR2	R/M	
001A2Aн			11/11	×××××
001А2Вн				VVVVV VVVVVVVR



Address	Register	Abbreviation	Access	Initial Value
001A40н				XXXXXXXX XXXXXXXx
001A41н	ID register 8	IDR8		
001A42н		ibito	10,11	XXXXX XXXXXXXX <sub>B</sub>
001А43н				
001А44н				XXXXXXXX XXXXXXX
001A45н	ID register 9	IDR9	R/W	
001A46н	-			XXXXX XXXXXXXXB
001А47н				
001A48н	-			XXXXXXXX XXXXXXXX
001A49н	ID register 10	IDR10	R/W	
001A4Aн	-			XXXXX XXXXXXXXB
001A4BH				
001A4CH	-		IDR11 R/W	XXXXXXXX XXXXXXXXB
001A4DH	ID register 11	IDR11		XXXXX XXXXXXXXB
001А4Ен 001А4Fн	-			
001А50н				
001А51н			5.44	XXXXXXXX XXXXXXXB
001А52н	ID register 12	IDR12	R/W	
001А53н				XXXXX XXXXXXXXB
001А54н				
001А55н	ID register 13		D ///	~~~~~~~~~~~~
001А56н		IDK 15	IX/ VV	XXXXX XXXXXXXX
001А57н				
001A58н				XXXXXXXX XXXXXXXx
001A59н	ID register 14	IDR14	R M	
001А5Ан				XXXXX XXXXXXXXB
001А5Вн				
001A5CH	4			XXXXXXXX XXXXXXXX
001А5Dн	ID register 15	IDR15	R/W	
001А5Eн	-			XXXXX XXXXXXXXB
001А5Fн				



Address	Register	Abbreviation	Access	Initial Value
001А88н to 001А8Fн	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXB
001А90н to 001А97н	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXB to XXXXXXXB
001А98н to 001А9Fн	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXB to XXXXXXXB
001АА0н to 001АА7н	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXB to XXXXXXXB
001АА8н to 001ААFн	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXB to XXXXXXXB
001АВ0н to 001АВ7н	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXB to XXXXXXXB
001АВ8н to 001АВFн	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXB to XXXXXXXB
001AC0н to 001AC7н	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXB to XXXXXXXB
001AC8н to 001ACFн	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXB to XXXXXXXB
001AD0н to 001AD7н	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXB to XXXXXXXB
001AD8н to 001ADFн	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXB to XXXXXXXB
001АЕ0н to 001АЕ7н	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXB to XXXXXXXB
001АЕ8н to 001АЕFн	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXB
001АF0н to 001AF7н	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXB
001AF8н to 001AFFн	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXB



# 10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

	El <sup>2</sup> OS	Interru	pt vector	Interrupt control register		
interrupt source	clear	Number Address		Number	Address	
Reset	N/A	# 08	FFFFDCH			
INT9 instruction	N/A	# 09	FFFFD8H			
Exception	N/A	# 10	FFFFD4H			
CAN RX	N/A	# 11	FFFFD0H	ICB00	0000B0н	
CAN TX/NS	N/A	# 12	<b>FFFFCC</b> <sub>H</sub>	ICRUU		
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8H		0000B1	
Time Base Timer	N/A	# 14	FFFFC4H	ICRUI	UUUUB IH	
16-bit Reload Timer 0	*1	# 15	FFFFC0H	ICR02	0000B2	
8/10-bit A/D Converter	*1	# 16	<b>FFFFBC</b> H	ICR02	0000628	
16-bit Free-run Timer	N/A	# 17	FFFFB8H		0000B2	
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4H	ICRUS	0000В3н	
Serial I/O	*1	# 19	FFFFB0H		0000B4H	
External Interrupt (INT4/INT5)	*1	# 20	FFFFACH	ICR04		
Input Capture 0	*1	# 21	FFFFA8H		0000B5н	
8/16-bit PPG 0/1	N/A	# 22	FFFFA4H	ICK05		
Output Compare 0	*1	# 23	FFFFA0H		0000B6н	
8/16-bit PPG 2/3	N/A	# 24	FFFF9CH	ICK00		
External Interrupt (INT6/INT7)	*1	# 25	FFFF98н		0000 <b>B7</b> н	
Input Capture 1	*1	# 26	FFFF94н			
8/16-bit PPG 4/5	N/A	# 27	FFFF90 <sub>H</sub>		0000B8H	
Output Compare 1	*1	# 28	FFFF8CH			
8/16-bit PPG 6/7	N/A	# 29	FFFF88 <sub>H</sub>		000089	
Input Capture 2	*1	# 30	FFFF84 <sub>H</sub>	101(09	0000698	
8/16-bit PPG 8/9	N/A	# 31	FFFF80 <sub>H</sub>		000084	
Output Compare 2	*1	# 32	FFFF7C <sub>H</sub>		OOODAH	
Input Capture 3	*1	# 33	FFFF78⊦		0000RB	
8/16-bit PPG A/B	N/A	# 34	FFFF74 <sub>H</sub>	юкт		
Output Compare 3	*1	# 35	FFFF70н		0000BC	
16-bit Reload Timer 1	*1	# 36	FFFF6C <sub>H</sub>	101(12	000000	
UART 0 RX	*2	# 37	FFFF68 <sub>H</sub>			
UART 0 TX	*1	# 38	FFFF64н	101(13		
UART 1 RX	*2	# 39	FFFF60 <sub>H</sub>		0000BE	
UART 1 TX	*1	# 40	FFFF5CH			
Flash Memory	N/A	# 41	FFFF58 <sub>H</sub>			
Delayed interrupt	N/A	# 42	FFFF54H	ICK IS		

\*1: The interrupt request flag is cleared by the El<sup>2</sup>OS interrupt clear signal.

\*2: The interrupt request flag is cleared by the El<sup>2</sup>OS interrupt clear signal. A stop request is available.

N/A:The interrupt request flag is not cleared by the EI2OS interrupt clear signal.



Notes:

- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the El<sup>2</sup>OS interrupt clear signal.
- At the end of EI<sup>2</sup>OS, the EI<sup>2</sup>OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI<sup>2</sup>OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI<sup>2</sup>OS clear signal caused by the first event. So it is recommended not to use the EI<sup>2</sup>OS for this interrupt number.
- If EI<sup>2</sup>OS is enabled, EI<sup>2</sup>OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI<sup>2</sup>OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI<sup>2</sup>OS, the other interrupt should be disabled.



- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the Vcc pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :



Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.





Parameter	Symbol	Pin name	Condition		Value	Unit	Bomarka	
Falameter	Symbol	Finname	Condition	Min	Тур	Max	Onit	Remarks
Input leak current	١L		Vcc = 5.5 V, Vss < V1 < Vcc	-5	_	5	μΑ	
			Vcc = 5.0 V±10%, Internal frequency: 16 MHz, At normal operating	_	35	60	mA	MB90598G
	ice			—	40	60	mA	MB90F598G
	lccs		Vcc = 5.0 V±10%, Internal frequency: 16 MHz, At sleep	_	11	18	mA	
Power supply current *	Істѕ	Vcc	V <sub>cc</sub> = 5.0 V±1%, Internal frequency: 2 MHz, At timer mode	_	0.3	0.6	mA	
	Іссн		Vcc = 5.0 V±10%, At stop, T <sub>A</sub> = 25°C	_	_	20	μΑ	
	_	$V_{CC} = 5.0 V \pm 10\%$ , At Hardware stand-	_	_	20	μA	MB90598G	
	Іссна		by mode, T₄ = 25°C		50	100	μΑ	MB90F598G





1.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only) ( $V_{CC} = 5.0 V \pm 10 \%$ , $V_{SS} = AV_{SS} = 0.0 V$ , $T_A = -40 \degree C$ to +85 $\degree C$ )								35 °C)	
Parameter	Symbol	Pin name	Condition	Value Min Typ Max		Unit	Remarks		
Output Rise/Fall time	tr2 tF2	Port P70 to P77, Port P80 to P87	_	15	40	150	ns		



## 11.5 A/D Converter

 $(V_{CC} = AV_{CC} = 5.0 \text{ V} \pm 10\%, \text{ V}_{SS} = AV_{SS} = 0.0 \text{ V}, 3.0 \text{ V} \le AV_{RH} - AV_{RL}, \text{ T}_{A} = -40 \text{ }^{\circ}\text{C} \text{ to } +85 \text{ }^{\circ}\text{C})$ 

Paramatar	Sym- Bin name		Value				Bomarka
Faidilielei	bol	Fill Hallie	Min	Тур	Max	Unit	Remarks
Resolution	—	—	_		10	bit	
Conversion error	—	—	_	—	±5.0	LSB	
Nonlinearity error	—	—	_	—	±2.5	LSB	
Differential linearity error	—	—	_	—	±1.9	LSB	
Zero transition voltage	Vот	AN0 to AN7	AVRL — 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	Vfst	AN0 to AN7	AVRH — 6.5 LSB	AVRH — 1.5 LSB	AVRH + 1.5 LSB	V	
Conversion time	—	—		352tcp	—	ns	
Sampling time	—	—	_	64tcP	—	ns	
Analog port input current	IAIN	AN0 to AN7	-10		10	μA	
Analog input voltage range	VAIN	AN0 to AN7	AVRL	_	AVRH	V	





## 11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions,:

- Output impedance values of the external circuit of 15 k $\Omega$  or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period =  $4.00 \ \mu s$  @machine clock of 16 MHz).



## Error

The smaller the |AVRH - AVRL|, the greater the error would become relatively.



## **Supply Current**





# **13. Ordering Information**

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

# 14. Package Dimensions







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