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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-192e1

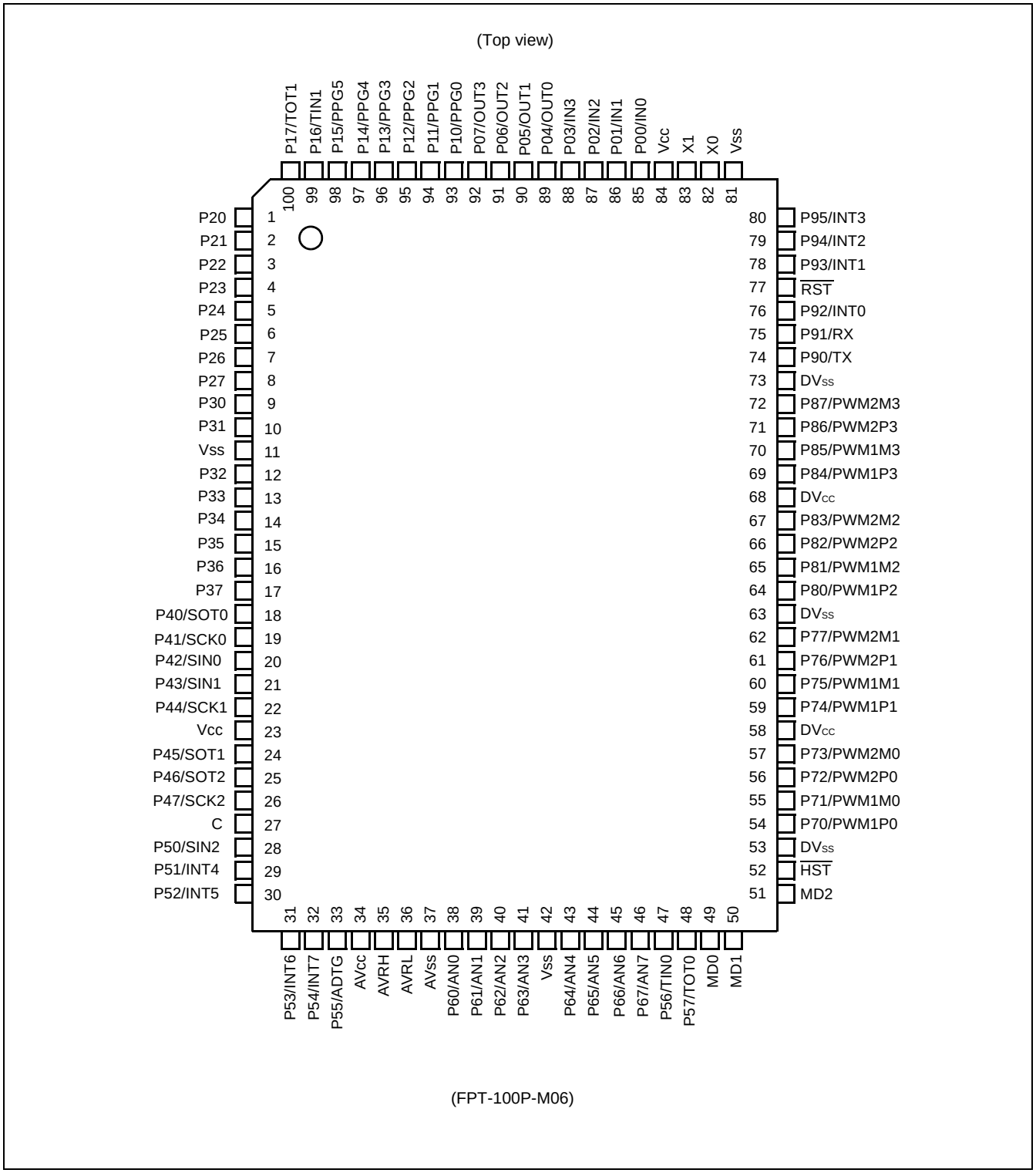
Contents

Features	MB90598G	MB90F598G	MB90V595G
CAN Interface	Number of channels: 1 Conforms to CAN Specification Version 2.0 Part A and B Automatic re-transmission in case of error Automatic transmission responding to Remote Frame Prioritized 16 message buffers for data and ID's Supports multiple messages Flexible configuration of acceptance filtering: Full bit compare / Full bit mask / Two partial bit masks Supports up to 1Mbps CAN bit timing setting: MB90598G/F598G:TSEG2 ≥ RSJW		
Stepping motor controller (4 channels)	Four high current outputs for each channel Synchronized two 8-bit PWM's for each channel		
External interrupt circuit	Number of inputs: 8 Started by a rising edge, a falling edge, an "H" level input, or an "L" level input.		
Serial IO	Clock synchronized transmission (31.25 K/62.5 K/125 K/500 K/1 Mbps at system clock frequency of 16 MHz) LSB first/MSB first		
Watchdog timer	Reset generation interval: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (at oscillation of 4 MHz, minimum value)		
Flash Memory	Supports automatic programming, Embedded Algorithm and Write/Erase/Erase-Suspend/Resume commands A flag indicating completion of the algorithm Hard-wired reset vector available in order to point to a fixed boot sector in Flash Memory Boot block configuration Erase can be performed on each block Block protection with external programming voltage Flash Writer from Minato Electronics, Inc.		
Low-power consumption (stand-by) mode	Sleep/stop/CPU intermittent operation/watch timer/hardware stand-by		
Process	CMOS		
Power supply voltage for operation*2	+5 V±10 %		
Package	QFP-100		PGA-256

*1: It is setting of DIP switch S2 when Emulation pod (MB2145-507) is used.
Please refer to the MB2145-507 hardware manual (2.7 Emulator-specific Power Pin) about details.

*2: Varies with conditions such as the operating frequency. (See "Electrical Characteristics.")

2. Pin Assignment

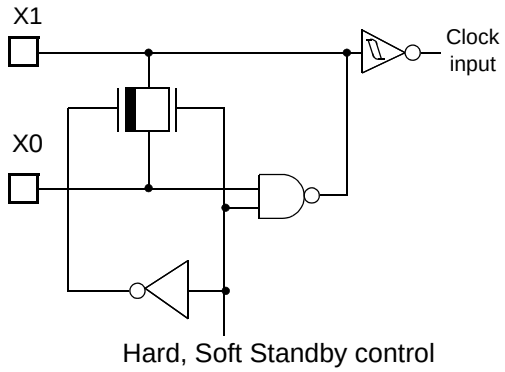
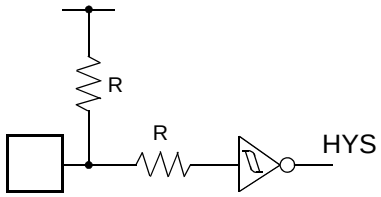
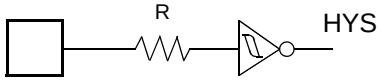


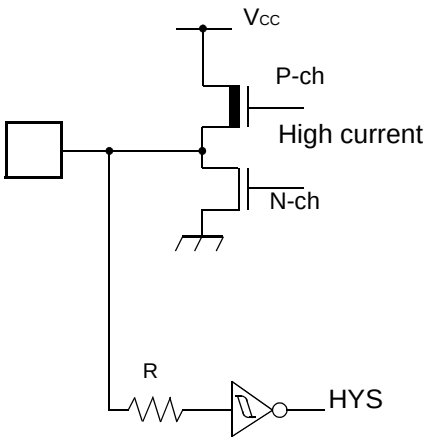
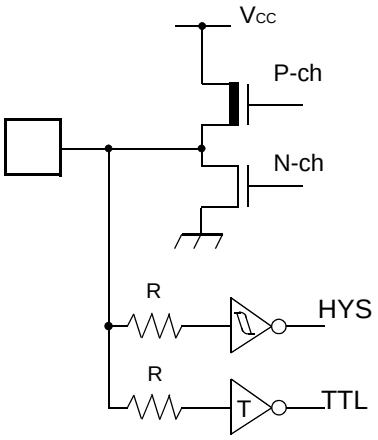
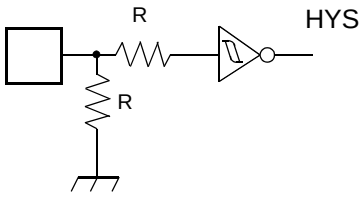
3. Pin Description

Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{\text{RST}}$	B	Reset input
52	$\overline{\text{HST}}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

Pin no.	Pin name	Circuit type	Function
76	P92	D	General purpose IO
	INT0		External interrupt input for INT0
78 to 80	P93 to P95	D	General purpose IO
	INT1 to INT3		External interrupt input for INT1 to INT3
58, 68	DV_{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV_{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV_{CC}	Power supply	Dedicated power supply pin for the A/D Converter
37	AV_{SS}	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter
49, 50	MD0 MD1	C	Operating mode selection input pins. These pins should be connected to V_{CC} or V_{SS}.
51	MD2	H	Operating mode selection input pin. This pin should be connected to V_{CC} or V_{SS}.
27	C	—	External capacitor pin. A capacitor of 0.1μF should be connected to this pin and V_{SS}.
23, 84	V_{CC}	Power supply	Power supply pins (5.0 V).
11, 42, 81	V_{SS}	Power supply	Ground pins (0.0 V).

4. I/O Circuit Type

Circuit Type	Circuit	Remarks
A		■ Oscillation feedback resistor: 1 MΩ approx.
B		■ Hysteresis input with pull-up Resistor: 50 kΩ approx.
C		■ Hysteresis input

Circuit Type	Circuit	Remarks
F		■ CMOS high current output ■ CMOS Hysteresis input
G		■ CMOS output ■ CMOS Hysteresis input ■ TTL input (MB90F598G, only in Flash mode)
H		■ Hysteresis input Pull-down Resistor: 50 kΩ approx. (except MB90F598G)

8. I/O Map

Address	Register	Abbreviation	Access	Peripheral	Initial value
00_H	Port 0 Data Register	PDR0	R/W	Port 0	$XXXXXXXX_B$
01_H	Port 1 Data Register	PDR1	R/W	Port 1	$XXXXXXXX_B$
02_H	Port 2 Data Register	PDR2	R/W	Port 2	$XXXXXXXX_B$
03_H	Port 3 Data Register	PDR3	R/W	Port 3	$XXXXXXXX_B$
04_H	Port 4 Data Register	PDR4	R/W	Port 4	$XXXXXXXX_B$
05_H	Port 5 Data Register	PDR5	R/W	Port 5	$XXXXXXXX_B$
06_H	Port 6 Data Register	PDR6	R/W	Port 6	$XXXXXXXX_B$
07_H	Port 7 Data Register	PDR7	R/W	Port 7	$XXXXXXXX_B$
08_H	Port 8 Data Register	PDR8	R/W	Port 8	$XXXXXXXX_B$
09_H	Port 9 Data Register	PDR9	R/W	Port 9	$\_\_XXXXXX_B$
$0A_H$ to $0F_H$	Reserved				
10_H	Port 0 Direction Register	DDR0	R/W	Port 0	00000000_B
11_H	Port 1 Direction Register	DDR1	R/W	Port 1	00000000_B
12_H	Port 2 Direction Register	DDR2	R/W	Port 2	00000000_B
13_H	Port 3 Direction Register	DDR3	R/W	Port 3	00000000_B
14_H	Port 4 Direction Register	DDR4	R/W	Port 4	00000000_B
15_H	Port 5 Direction Register	DDR5	R/W	Port 5	00000000_B
16_H	Port 6 Direction Register	DDR6	R/W	Port 6	00000000_B
17_H	Port 7 Direction Register	DDR7	R/W	Port 7	00000000_B
18_H	Port 8 Direction Register	DDR8	R/W	Port 8	00000000_B
19_H	Port 9 Direction Register	DDR9	R/W	Port 9	$\_\_000000_B$
$1A_H$	Reserved				
$1B_H$	Analog Input Enable Register	ADER	R/W	Port 6, A/D	11111111_B
$1C_H$ to $1F_H$	Reserved				
20_H	Serial Mode Control Register 0	UMC0	R/W	UART0	00000100_B
21_H	Serial status Register 0	USR0	R/W		00010000_B
22_H	Serial Input/Output Data Register 0	UIDR0/UODR0	R/W		$XXXXXXXX_B$
23_H	Rate and Data Register 0	URD0	R/W		$0000000X_B$
24_H	Serial Mode Register 1	SMR1	R/W	UART1	00000000_B
25_H	Serial Control Register 1	SCR1	R/W		00000100_B
26_H	Serial Input/Output Data Register 1	SIDR1/SODR1	R/W		$XXXXXXXX_B$
27_H	Serial Status Register 1	SSR1	R/W		0001_00_B
28_H	UART1 Prescaler Control Register	U1CDCR	R/W		$0\_\_\_1111_B$

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
29H to 2AH	Reserved				
2BH	Serial IO Prescaler	SCDCR	R/W	Serial IO	0 _ _ _ 1 1 1 1B
2CH	Serial Mode Control Register (low-order)	SMCS	R/W		_ _ _ _ 0 0 0 0B
2DH	Serial Mode Control Register (high-order)	SMCS	R/W		0 0 0 0 0 0 1 0B
2EH	Serial Data Register	SDR	R/W		XXXXXXXXB
2FH	Edge Selector	SES	R/W		_ _ _ _ _ _ _ 0B
30H	External Interrupt Enable Register	ENIR	R/W	External Interrupt	0 0 0 0 0 0 0 0B
31H	External Interrupt Request Register	EIRR	R/W		XXXXXXXXB
32H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
33H	External Interrupt Level Register	ELVR	R/W		0 0 0 0 0 0 0 0B
34H	A/D Control Status Register 0	ADCS0	R/W	A/D Converter	0 0 0 0 0 0 0 0B
35H	A/D Control Status Register 1	ADCS1	R/W		0 0 0 0 0 0 0 0B
36H	A/D Data Register 0	ADCR0	R		XXXXXXXXB
37H	A/D Data Register 1	ADCR1	R/W		0 0 0 0 1 _ XXB
38H	PPG0 Operation Mode Control Register	PPGC0	R/W	16-bit Programmable Pulse Generator 0/1	0 _ 0 0 0 _ _ 1B
39H	PPG1 Operation Mode Control Register	PPGC1	R/W		0 _ 0 0 0 0 0 1B
3AH	PPG0, 1 Output Pin Control Register	PPG01	R/W		0 0 0 0 0 0 _ _B
3BH	Reserved				
3CH	PPG2 Operation Mode Control Register	PPGC2	R/W	16-bit Programmable Pulse Generator 2/3	0 _ 0 0 0 _ _ 1B
3DH	PPG3 Operation Mode Control Register	PPGC3	R/W		0 _ 0 0 0 0 0 1B
3EH	PPG2, 3 Output Pin Control Register	PPG23	R/W		0 0 0 0 0 0 _ _B
3FH	Reserved				
40H	PPG4 Operation Mode Control Register	PPGC4	R/W	16-bit Programmable Pulse Generator 4/5	0 _ 0 0 0 _ _ 1B
41H	PPG5 Operation Mode Control Register	PPGC5	R/W		0 _ 0 0 0 0 0 1B
42H	PPG4, 5 Output Pin Control Register	PPG45	R/W		0 0 0 0 0 0 _ _B
43H	Reserved				
44H	PPG6 Operation Mode Control Register	PPGC6	R/W	16-bit Programmable Pulse Generator 6/7	0 _ 0 0 0 _ _ 1B
45H	PPG7 Operation Mode Control Register	PPGC7	R/W		0 _ 0 0 0 0 0 1B
46H	PPG6, 7 Output Pin Control Register	PPG67	R/W		0 0 0 0 0 0 _ _B
47H	Reserved				
48H	PPG8 Operation Mode Control Register	PPGC8	R/W	16-bit Programmable Pulse Generator 8/9	0 _ 0 0 0 _ _ 1B
49H	PPG9 Operation Mode Control Register	PPGC9	R/W		0 _ 0 0 0 0 0 1B
4AH	PPG8, 9 Output Pin Control Register	PPG89	R/W		0 0 0 0 0 0 _ _B
4BH	Reserved				

(Continued)

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Address	Register	Abbreviation	Access	Initial Value
001B08H	IDE register	IDER	R/W	XXXXXXXX XXXXXXXXB
001B09H				
001B0AH	Transmit RTR register	TRTRR	R/W	00000000 00000000B
001B0BH				
001B0CH	Remote frame receive waiting register	RFWTR	R/W	XXXXXXXX XXXXXXXXB
001B0DH				
001B0EH	Transmit interrupt enable register	TIER	R/W	00000000 00000000B
001B0FH				
001B10H	Acceptance mask select register	AMSR	R/W	XXXXXXXX XXXXXXXXB
001B11H				
001B12H				XXXXXXXX XXXXXXXXB
001B13H				
001B14H	Acceptance mask register 0	AMR0	R/W	XXXXXXXX XXXXXXXXB
001B15H				
001B16H				XXXXX--- XXXXXXXXB
001B17H				
001B18H	Acceptance mask register 1	AMR1	R/W	XXXXXXXX XXXXXXXXB
001B19H				
001B1AH				XXXXX--- XXXXXXXXB
001B1BH				

9.2 List of Message Buffers (ID Registers)

Address	Register	Abbreviation	Access	Initial Value
001A00H to 001A1FH	General-purpose RAM	--	R/W	XXXXXXXXB to XXXXXXXXB
001A20H	ID register 0	IDR0	R/W	XXXXXXXX XXXXXXXXB
001A21H				
001A22H				XXXXX--- XXXXXXXXB
001A23H				
001A24H	ID register 1	IDR1	R/W	XXXXXXXX XXXXXXXXB
001A25H				
001A26H				XXXXX--- XXXXXXXXB
001A27H				
001A28H	ID register 2	IDR2	R/W	XXXXXXXX XXXXXXXXB
001A29H				
001A2AH				XXXXX--- XXXXXXXXB
001A2BH				

(Continued)

Address	Register	Abbreviation	Access	Initial Value
001A40H	ID register 8	IDR8	R/W	XXXXXXXX XXXXXXXXB
001A41H				
001A42H				XXXXX--- XXXXXXXXB
001A43H				
001A44H	ID register 9	IDR9	R/W	XXXXXXXX XXXXXXXXB
001A45H				
001A46H				XXXXX--- XXXXXXXXB
001A47H				
001A48H	ID register 10	IDR10	R/W	XXXXXXXX XXXXXXXXB
001A49H				
001A4AH				XXXXX--- XXXXXXXXB
001A4BH				
001A4CH	ID register 11	IDR11	R/W	XXXXXXXX XXXXXXXXB
001A4DH				
001A4EH				XXXXX--- XXXXXXXXB
001A4FH				
001A50H	ID register 12	IDR12	R/W	XXXXXXXX XXXXXXXXB
001A51H				
001A52H				XXXXX--- XXXXXXXXB
001A53H				
001A54H	ID register 13	IDR13	R/W	XXXXXXXX XXXXXXXXB
001A55H				
001A56H				XXXXX--- XXXXXXXXB
001A57H				
001A58H	ID register 14	IDR14	R/W	XXXXXXXX XXXXXXXXB
001A59H				
001A5AH				XXXXX--- XXXXXXXXB
001A5BH				
001A5CH	ID register 15	IDR15	R/W	XXXXXXXX XXXXXXXXB
001A5DH				
001A5EH				XXXXX--- XXXXXXXXB
001A5FH				

(Continued)

Address	Register	Abbreviation	Access	Initial Value
001A88H to 001A8FH	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXXB to XXXXXXXXB
001A90H to 001A97H	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXXB to XXXXXXXXB
001A98H to 001A9FH	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXXB to XXXXXXXXB
001AA0H to 001AA7H	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXXB to XXXXXXXXB
001AA8H to 001AAFH	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXXB to XXXXXXXXB
001AB0H to 001AB7H	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXXB to XXXXXXXXB
001AB8H to 001ABFH	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXXB to XXXXXXXXB
001AC0H to 001AC7H	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXXB to XXXXXXXXB
001AC8H to 001ACFH	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXXB to XXXXXXXXB
001AD0H to 001AD7H	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXXB to XXXXXXXXB
001AD8H to 001ADFH	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXXB to XXXXXXXXB
001AE0H to 001AE7H	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXXB to XXXXXXXXB
001AE8H to 001AEFH	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXXB to XXXXXXXXB
001AF0H to 001AF7H	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXXB to XXXXXXXXB
001AF8H to 001AFFH	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXXB to XXXXXXXXB

10. Interrupt Source, Interrupt Vector, and Interrupt Control Register

Interrupt source	EI²OS clear	Interrupt vector		Interrupt control register	
		Number	Address	Number	Address
Reset	N/A	# 08	FFFFDC$_H$	——	——
INT9 instruction	N/A	# 09	FFFFD8$_H$	——	——
Exception	N/A	# 10	FFFFD4$_H$	——	——
CAN RX	N/A	# 11	FFFFD0$_H$	ICR00	0000B0$_H$
CAN TX/NS	N/A	# 12	FFFFCC$_H$		
External Interrupt (INT0/INT1)	*1	# 13	FFFFC8$_H$	ICR01	0000B1$_H$
Time Base Timer	N/A	# 14	FFFFC4$_H$		
16-bit Reload Timer 0	*1	# 15	FFFFC0$_H$	ICR02	0000B2$_H$
8/10-bit A/D Converter	*1	# 16	FFFFBC$_H$		
16-bit Free-run Timer	N/A	# 17	FFFFB8$_H$	ICR03	0000B3$_H$
External Interrupt (INT2/INT3)	*1	# 18	FFFFB4$_H$		
Serial I/O	*1	# 19	FFFFB0$_H$	ICR04	0000B4$_H$
External Interrupt (INT4/INT5)	*1	# 20	FFFFAC$_H$		
Input Capture 0	*1	# 21	FFFFA8$_H$	ICR05	0000B5$_H$
8/16-bit PPG 0/1	N/A	# 22	FFFFA4$_H$		
Output Compare 0	*1	# 23	FFFFA0$_H$	ICR06	0000B6$_H$
8/16-bit PPG 2/3	N/A	# 24	FFFF9C$_H$		
External Interrupt (INT6/INT7)	*1	# 25	FFFF98$_H$	ICR07	0000B7$_H$
Input Capture 1	*1	# 26	FFFF94$_H$		
8/16-bit PPG 4/5	N/A	# 27	FFFF90$_H$	ICR08	0000B8$_H$
Output Compare 1	*1	# 28	FFFF8C$_H$		
8/16-bit PPG 6/7	N/A	# 29	FFFF88$_H$	ICR09	0000B9$_H$
Input Capture 2	*1	# 30	FFFF84$_H$		
8/16-bit PPG 8/9	N/A	# 31	FFFF80$_H$	ICR10	0000BA$_H$
Output Compare 2	*1	# 32	FFFF7C$_H$		
Input Capture 3	*1	# 33	FFFF78$_H$	ICR11	0000BB$_H$
8/16-bit PPG A/B	N/A	# 34	FFFF74$_H$		
Output Compare 3	*1	# 35	FFFF70$_H$	ICR12	0000BC$_H$
16-bit Reload Timer 1	*1	# 36	FFFF6C$_H$		
UART 0 RX	*2	# 37	FFFF68$_H$	ICR13	0000BD$_H$
UART 0 TX	*1	# 38	FFFF64$_H$		
UART 1 RX	*2	# 39	FFFF60$_H$	ICR14	0000BE$_H$
UART 1 TX	*1	# 40	FFFF5C$_H$		
Flash Memory	N/A	# 41	FFFF58$_H$	ICR15	0000BF$_H$
Delayed interrupt	N/A	# 42	FFFF54$_H$		

*1: The interrupt request flag is cleared by the EI²OS interrupt clear signal.

*2: The interrupt request flag is cleared by the EI²OS interrupt clear signal. A stop request is available.

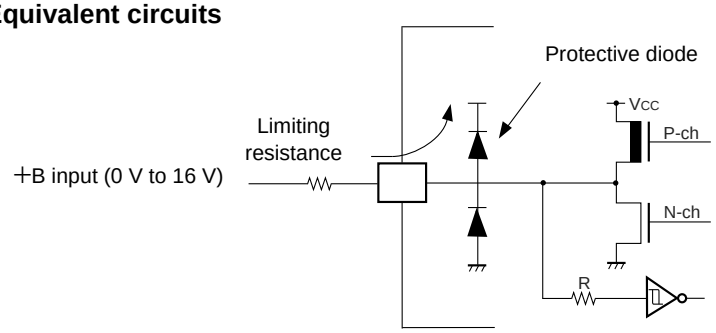
N/A:The interrupt request flag is not cleared by the EI²OS interrupt clear signal.

Notes:

- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller current is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on result.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits :

• Input/Output Equivalent circuits



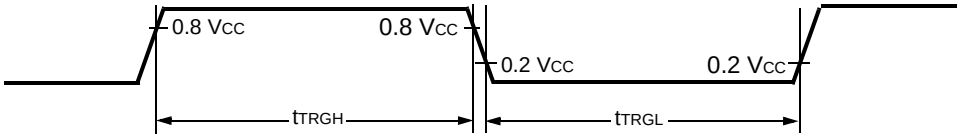
Note: : Average output current = operating current × operating efficiency

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}		V_{CC} = 5.5 V, $V_{SS} < V_I < V_{CC}$	–5	—	5	µA	
Power supply current *	I_{CC}	V_{CC}	V_{CC} = 5.0 V±10%, Internal frequency: 16 MHz, At normal operating	—	35	60	mA	MB90598G
				—	40	60	mA	MB90F598G
	I_{CCS}		V_{CC} = 5.0 V±10%, Internal frequency: 16 MHz, At sleep	—	11	18	mA	
	I_{CTS}		V_{CC} = 5.0 V±1%, Internal frequency: 2 MHz, At timer mode	—	0.3	0.6	mA	
	I_{CCH}		V_{CC} = 5.0 V±10%, At stop, T_A = 25°C	—	—	20	µA	
	I_{CCH2}		V_{CC} = 5.0 V±10%, At Hardware stand-by mode, T_A = 25°C	—	—	20	µA	MB90598G
				—	50	100	µA	MB90F598G

(Continued)

- **Trigger Input Timing**



11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)

(V_{CC} = 5.0 V±10 %, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Output Rise/Fall time	t_{R2} t_{F2}	Port P70 to P77, Port P80 to P87	—	15	40	150	ns	

- Slew Rate Output Timing

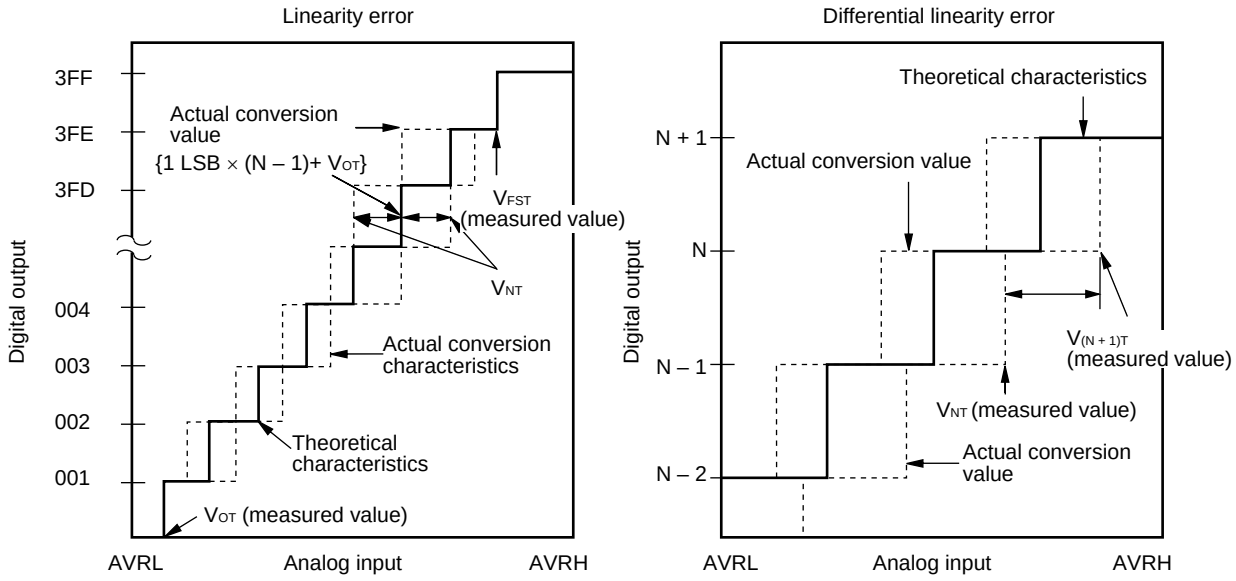
$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

11.5 A/D Converter

(V_{CC} = AV_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V,3.0 V ≤ AVRH − AVRL, T_A = −40 °C to +85 °C)

Parameter	Sym-bol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—		10	bit	
Conversion error	—	—	—	—	±5.0	LSB	
Nonlinearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AVRL − 3.5 LSB	AVRL + 0.5 LSB	AVRL + 4.5 LSB	V	
Full scale transition voltage	V_{FST}	AN0 to AN7	AVRH − 6.5 LSB	AVRH − 1.5 LSB	AVRH + 1.5 LSB	V	
Conversion time	—	—	—	352t_{CP}	—	ns	
Sampling time	—	—	—	64t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	−10	—	10	µA	
Analog input voltage range	V_{AIN}	AN0 to AN7	AVRL	—	AVRH	V	

(Continued)



$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

V_{OT}: Voltage at transition of digital output from "000_H" to "001_H"
V_{FST}: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

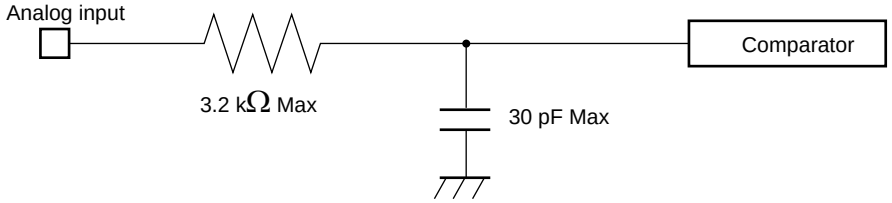
11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions,:

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

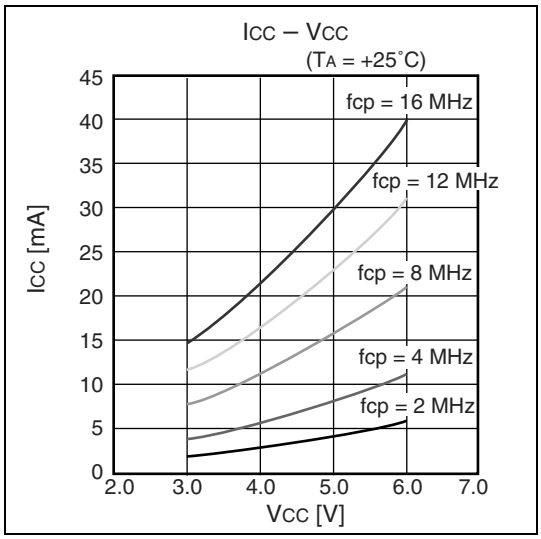
- **Equipment of analog input circuit model**

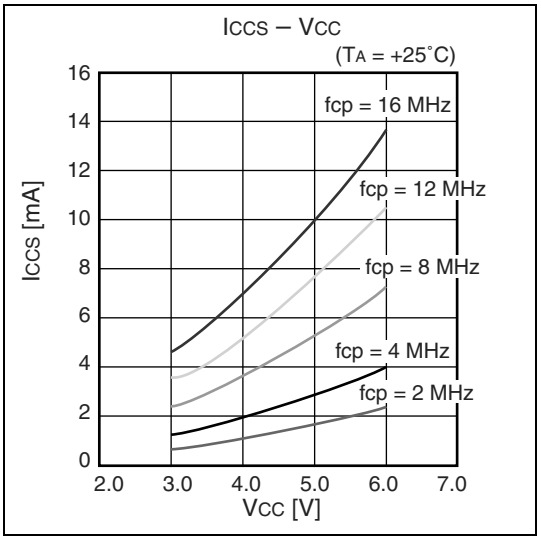


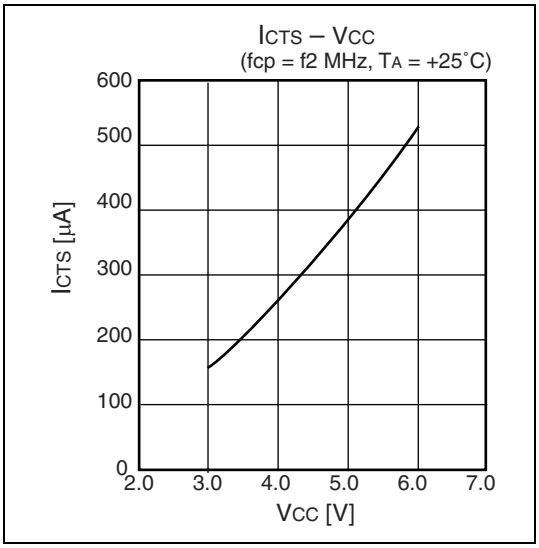
■ Error

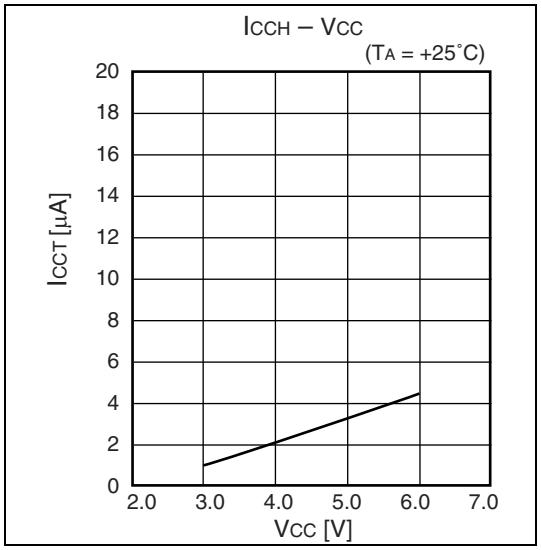
The smaller the | AVRH − AVRL |, the greater the error would become relatively.

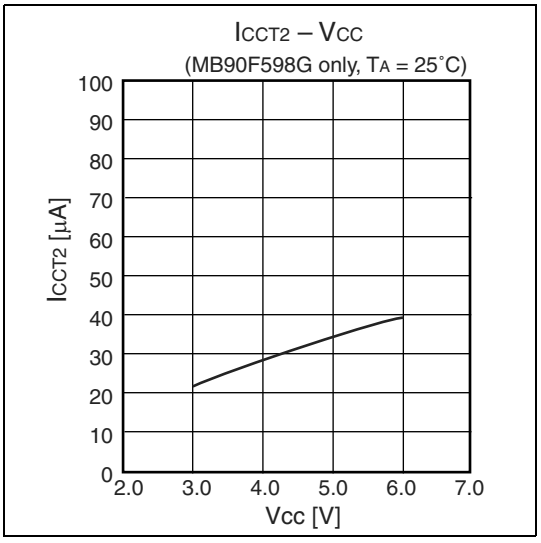
Supply Current







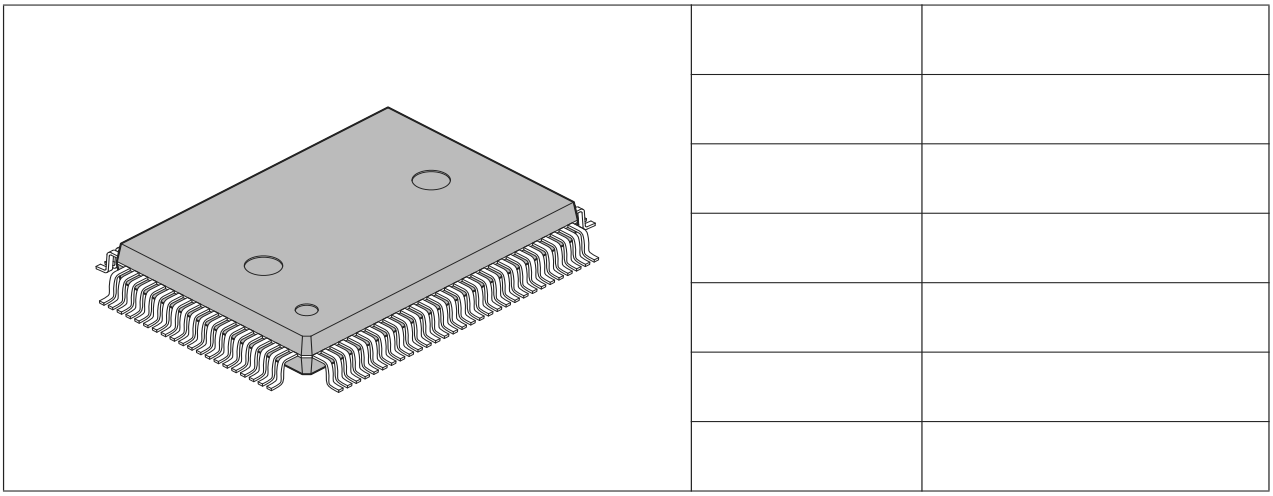


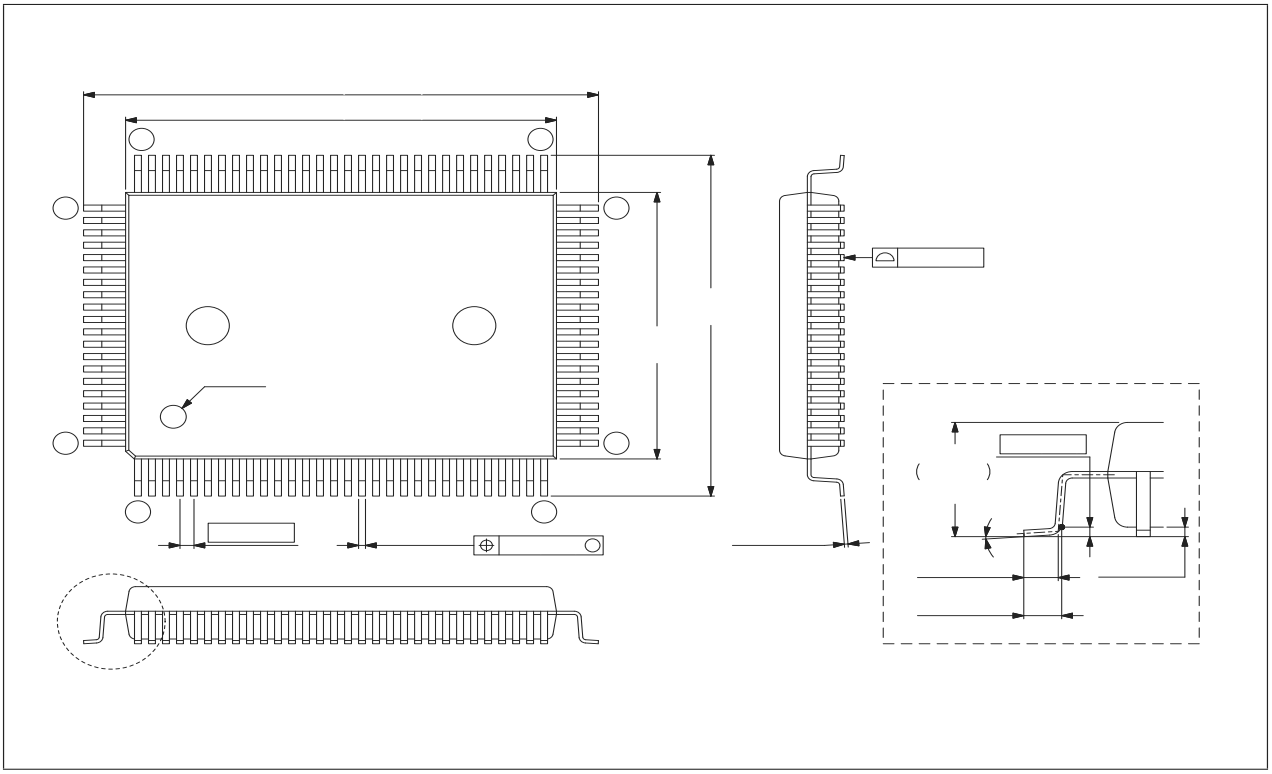


13. Ordering Information

Part number	Package	Remarks
MB90598GPF MB90F598GPF	100-pin Plastic QFP (FPT-100P-M06)	
MB90V595GCR	256-pin Ceramic PGA (PGA-256C-A01)	For evaluation

14. Package Dimensions





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