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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | F²MC-16LX |
| Core Size | 16-Bit |
| Speed | 16MHz |
| Connectivity | CANbus, EBI/EMI, SCI, Serial I/O, UART/USART |
| Peripherals | POR, PWM, WDT |
| Number of I/O | 78 |
| Program Memory Size | 128KB (128K x 8) |
| Program Memory Type | Mask ROM |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 5.5V |
| Data Converters | A/D 8x8/10b |
| Oscillator Type | External |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-BQFP |
| Supplier Device Package | 100-QFP (14x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-g-194e1 |

## 3. Pin Description

| Pin no. | Pin name | Circuit type | Function |
|---|---|---|---|
| 82 | X0 | A | Oscillator pin |
| 83 | X1 | | |
| 77 | $\overline{\text{RST}}$ | B | Reset input |
| 52 | $\overline{\text{HST}}$ | C | Hardware standby input |
| 85 to 88 | P00 to P03 | G | General purpose IO |
| | IN0 to IN3 | | Inputs for the Input Captures |
| 89 to 92 | P04 to P07 | G | General purpose IO |
| | OUT0 to OUT3 | | Outputs for the Output Compares. |
| 93 to 98 | P10 to P15 | D | General purpose IO |
| | PPG0 to PPG5 | | Outputs for the Programmable Pulse Generators |
| 99 | P16 | D | General purpose IO |
| | TIN1 | | TIN input for the 16-bit Reload Timer 1 |
| 100 | P17 | D | General purpose IO |
| | TOT1 | | TOT output for the 16-bit Reload Timer 1 |
| 1 to 8 | P20 to P27 | G | General purpose IO |
| 9 to 10 | P30 to P31 | G | General purpose IO |
| 12 to 16 | P32 to P36 | G | General purpose IO |
| 17 | P37 | D | General purpose IO |
| 18 | P40 | G | General purpose IO |
| | SOT0 | | SOT output for UART 0 |
| 19 | P41 | G | General purpose IO |
| | SCK0 | | SCK input/output for UART 0 |
| 20 | P42 | G | General purpose IO |
| | SIN0 | | SIN input for UART 0 |
| 21 | P43 | G | General purpose IO |
| | SIN1 | | SIN input for UART 1 |
| 22 | P44 | G | General purpose IO |
| | SCK1 | | SCK input/output for UART 1 |
| 24 | P45 | G | General purpose IO |
| | SOT1 | | SOT output for UART 1 |
| 25 | P46 | G | General purpose IO |
| | SOT2 | | SOT output for the Serial IO |
| 26 | P47 | G | General purpose IO |
| | SCK2 | | SCK input/output for the Serial IO |

| Pin no. | Pin name | Circuit type | Function |
|---|---|---|---|
| 28 | P50 | D | General purpose IO |
| | SIN2 | | SIN Input for the Serial IO |
| 29 to 32 | P51 to P54 | D | General purpose IO |
| | INT4 to INT7 | | External interrupt input for INT4 to INT7 |
| 33 | P55 | D | General purpose IO |
| | ADTG | | Input for the external trigger of the A/D Converter |
| 38 to 41 | P60 to P63 | E | General purpose IO |
| | AN0 to AN3 | | Inputs for the A/D Converter |
| 43 to 46 | P64 to P67 | E | General purpose IO |
| | AN4 to AN7 | | Inputs for the A/D Converter |
| 47 | P56 | D | General purpose IO |
| | TIN0 | | TIN input for the 16-bit Reload Timer 0 |
| 48 | P57 | D | General purpose IO |
| | TOT0 | | TOT output for the 16-bit Reload Timer 0 |
| 54 to 57 | P70 to P73 | F | General purpose IO |
| | PWM1P0<br>PWM1M0<br>PWM2P0<br>PWM2M0 | | Output for Stepper Motor Controller channel 0 |
| 59 to 62 | P74 to P77 | F | General purpose IO |
| | PWM1P1<br>PWM1M1<br>PWM2P1<br>PWM2M1 | | Output for Stepper Motor Controller channel 1 |
| 64 to 67 | P80 to P83 | F | General purpose IO |
| | PWM1P2<br>PWM1M2<br>PWM2P2<br>PWM2M2 | | Output for Stepper Motor Controller channel 2 |
| 69 to 72 | P84 to P87 | F | General purpose IO |
| | PWM1P3<br>PWM1M3<br>PWM2P3<br>PWM2M3 | | Output for Stepper Motor Controller channel 3 |
| 74 | P90 | D | General purpose IO |
| | TX | | TX output for CAN Interface |
| 75 | P91 | D | General purpose IO |
| | RX | | RX input for CAN Interface |

**(5) Pull-up/down resistors**
The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

**(6) Crystal Oscillator Circuit**
Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.
A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

**(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs**
Make sure to turn on the A/D converter power supply ($AV_{CC}$, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply ($V_{CC}$).
Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or $AV_{CC}$ (turning on/off the analog and digital power supplies simultaneously is acceptable).

**(8) Connection of Unused Pins of A/D Converter**
Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, $AV_{SS} = AVRH = DV_{CC} = V_{SS}$.

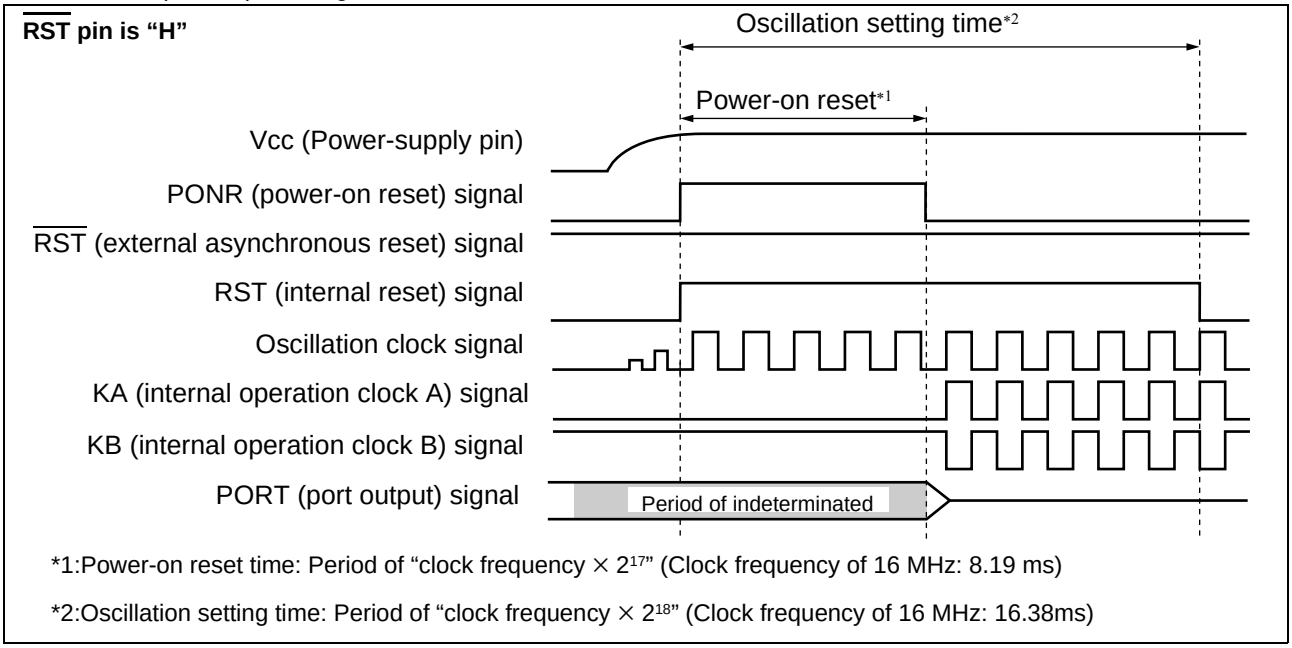
**(9) N.C. Pin**
The N.C. (internally connected) pin must be opened for use.

**(10) Notes on Energization**
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

**(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)**
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

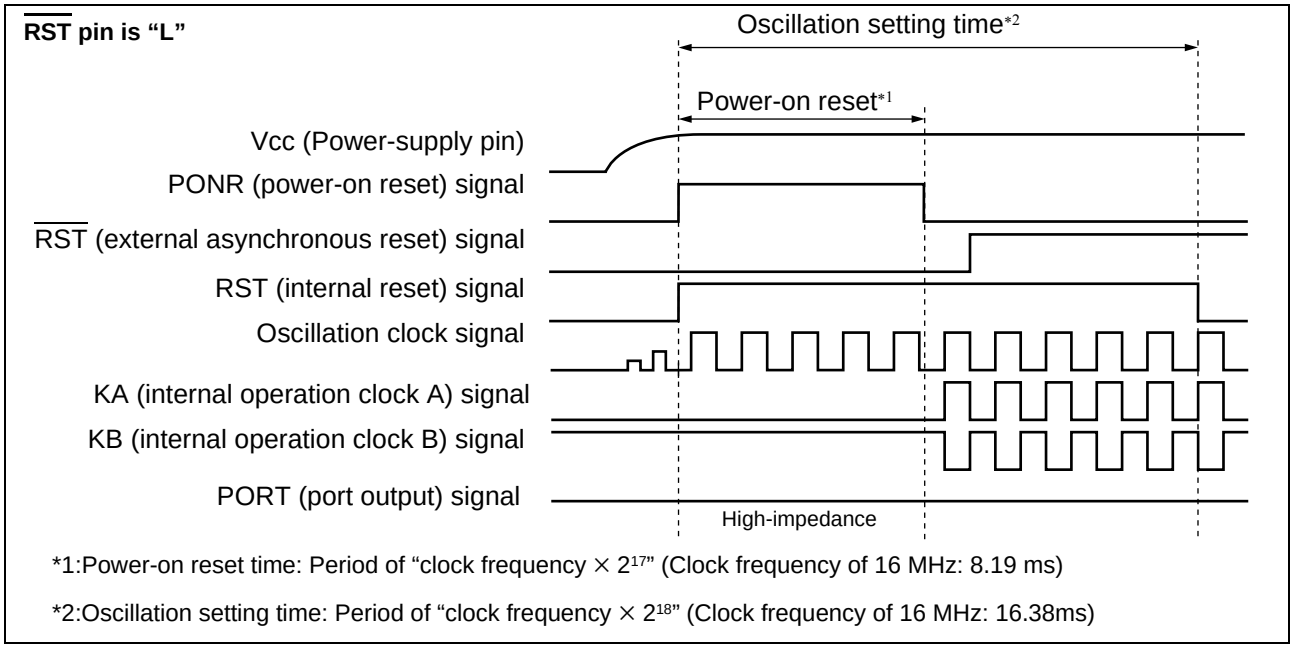
■ If $\overline{RST}$ pin is “H”, the outputs become indeterminate.

■ If $\overline{RST}$ pin is “L”, the outputs become high-impedance.
Pay attention to the port output timing shown as follows.




*1:Power-on reset time: Period of “clock frequency × $2^{17}$” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × $2^{18}$” (Clock frequency of 16 MHz: 16.38ms)




*1:Power-on reset time: Period of “clock frequency × $2^{17}$” (Clock frequency of 16 MHz: 8.19 ms)

*2:Oscillation setting time: Period of “clock frequency × $2^{18}$” (Clock frequency of 16 MHz: 16.38ms)

**(12) Initialization**

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

**(13) Directions of “DIV A, Ri” and “DIVW A, RWi” instructions**

In the signed multiplication and division instructions (“DIV A, Ri” and “DIVW A, RWi”), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in “$00_H$”.

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than “$00_H$”, the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

**(14) Using REALOS**

The use of $EI^2OS$ is not possible with the REALOS real time operating system.

**(15) Caution on Operations during PLL Clock Mode**

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

## 8. I/O Map

| Address | Register | Abbreviation | Access | Peripheral | Initial value |
|---|---|---|---|---|---|
| $00_H$ | Port 0 Data Register | PDR0 | R/W | Port 0 | $XXXXXXXX_B$ |
| $01_H$ | Port 1 Data Register | PDR1 | R/W | Port 1 | $XXXXXXXX_B$ |
| $02_H$ | Port 2 Data Register | PDR2 | R/W | Port 2 | $XXXXXXXX_B$ |
| $03_H$ | Port 3 Data Register | PDR3 | R/W | Port 3 | $XXXXXXXX_B$ |
| $04_H$ | Port 4 Data Register | PDR4 | R/W | Port 4 | $XXXXXXXX_B$ |
| $05_H$ | Port 5 Data Register | PDR5 | R/W | Port 5 | $XXXXXXXX_B$ |
| $06_H$ | Port 6 Data Register | PDR6 | R/W | Port 6 | $XXXXXXXX_B$ |
| $07_H$ | Port 7 Data Register | PDR7 | R/W | Port 7 | $XXXXXXXX_B$ |
| $08_H$ | Port 8 Data Register | PDR8 | R/W | Port 8 | $XXXXXXXX_B$ |
| $09_H$ | Port 9 Data Register | PDR9 | R/W | Port 9 | $\_\_XXXXXX_B$ |
| $0A_H$ to $0F_H$ | Reserved | | | | |
| $10_H$ | Port 0 Direction Register | DDR0 | R/W | Port 0 | $00000000_B$ |
| $11_H$ | Port 1 Direction Register | DDR1 | R/W | Port 1 | $00000000_B$ |
| $12_H$ | Port 2 Direction Register | DDR2 | R/W | Port 2 | $00000000_B$ |
| $13_H$ | Port 3 Direction Register | DDR3 | R/W | Port 3 | $00000000_B$ |
| $14_H$ | Port 4 Direction Register | DDR4 | R/W | Port 4 | $00000000_B$ |
| $15_H$ | Port 5 Direction Register | DDR5 | R/W | Port 5 | $00000000_B$ |
| $16_H$ | Port 6 Direction Register | DDR6 | R/W | Port 6 | $00000000_B$ |
| $17_H$ | Port 7 Direction Register | DDR7 | R/W | Port 7 | $00000000_B$ |
| $18_H$ | Port 8 Direction Register | DDR8 | R/W | Port 8 | $00000000_B$ |
| $19_H$ | Port 9 Direction Register | DDR9 | R/W | Port 9 | $\_\_000000_B$ |
| $1A_H$ | Reserved | | | | |
| $1B_H$ | Analog Input Enable Register | ADER | R/W | Port 6, A/D | $11111111_B$ |
| $1C_H$ to $1F_H$ | Reserved | | | | |
| $20_H$ | Serial Mode Control Register 0 | UMC0 | R/W | UART0 | $00000100_B$ |
| $21_H$ | Serial status Register 0 | USR0 | R/W | | $00010000_B$ |
| $22_H$ | Serial Input/Output Data Register 0 | UIDR0/UODR0 | R/W | | $XXXXXXXX_B$ |
| $23_H$ | Rate and Data Register 0 | URD0 | R/W | | $0000000X_B$ |
| $24_H$ | Serial Mode Register 1 | SMR1 | R/W | UART1 | $00000000_B$ |
| $25_H$ | Serial Control Register 1 | SCR1 | R/W | | $00000100_B$ |
| $26_H$ | Serial Input/Output Data Register 1 | SIDR1/SODR1 | R/W | | $XXXXXXXX_B$ |
| $27_H$ | Serial Status Register 1 | SSR1 | R/W | | $0001\_00_B$ |
| $28_H$ | UART1 Prescaler Control Register | U1CDCR | R/W | | $0\_\_\_1111_B$ |

*(Continued)*

| Address | Register | Abbreviation | Access | Peripheral | Initial value |
|---|---|---|---|---|---|
| 4C$_H$ | PPGA Operation Mode Control Register | PPGCA | R/W | 16-bit Programmable Pulse Generator A/B | 0 _ 0 0 0 _ _ 1$_B$ |
| 4D$_H$ | PPGB Operation Mode Control Register | PPGCB | R/W | | 0 _ 0 0 0 0 0 1$_B$ |
| 4E$_H$ | PPGA, B Output Pin Control Register | PPGAB | R/W | | 0 0 0 0 0 0 _ _$_B$ |
| 4F$_H$ | Reserved | | | | |
| 50$_H$ | Timer Control Status Register 0 | TMCSR0 | R/W | 16-bit Reload Timer 0 | 0 0 0 0 0 0 0 0$_B$ |
| 51$_H$ | Timer Control Status Register 0 | TMCSR0 | R/W | | _ _ _ _ 0 0 0 0$_B$ |
| 52$_H$ | Timer 0/Reload Register 0 | TMR0/TMRLR0 | R/W | | XXXXXXXX$_B$ |
| 53$_H$ | Timer 0/Reload Register 0 | TMR0/TMRLR0 | R/W | | XXXXXXXX$_B$ |
| 54$_H$ | Timer Control Status Register 1 | TMCSR1 | R/W | 16-bit Reload Timer 1 | 0 0 0 0 0 0 0 0$_B$ |
| 55$_H$ | Timer Control Status Register 1 | TMCSR1 | R/W | | _ _ _ _ 0 0 0 0$_B$ |
| 56$_H$ | Timer Register 1/Reload Register 1 | TMR1/TMRLR1 | R/W | | XXXXXXXX$_B$ |
| 57$_H$ | Timer Register 1/Reload Register 1 | TMR1/TMRLR1 | R/W | | XXXXXXXX$_B$ |
| 58$_H$ | Output Compare Control Status Register 0 | OCS0 | R/W | Output Compare 0/1 | 0 0 0 0 _ _ 0 0$_B$ |
| 59$_H$ | Output Compare Control Status Register 1 | OCS1 | R/W | | _ _ _ 0 0 0 0 0$_B$ |
| 5A$_H$ | Output Compare Control Status Register 2 | OCS2 | R/W | Output Compare 2/3 | 0 0 0 0 _ _ 0 0$_B$ |
| 5B$_H$ | Output Compare Control Status Register 3 | OCS3 | R/W | | _ _ _ 0 0 0 0 0$_B$ |
| 5C$_H$ | Input Capture Control Status Register 0/1 | ICS01 | R/W | Input Capture 0/1 | 0 0 0 0 0 0 0 0$_B$ |
| 5D$_H$ | Input Capture Control Status Register 2/3 | ICS23 | R/W | Input Capture 2/3 | 0 0 0 0 0 0 0 0$_B$ |
| 5E$_H$ | PWM Control Register 0 | PWC0 | R/W | Stepping Motor Controller 0 | 0 0 0 0 0 _ _ 0$_B$ |
| 5F$_H$ | Reserved | | | | |
| 60$_H$ | PWM Control Register 1 | PWC1 | R/W | Stepping Motor Controller 1 | 0 0 0 0 0 _ _ 0$_B$ |
| 61$_H$ | Reserved | | | | |
| 62$_H$ | PWM Control Register 2 | PWC2 | R/W | Stepping Motor Controller 2 | 0 0 0 0 0 _ _ 0$_B$ |
| 63$_H$ | Reserved | | | | |
| 64$_H$ | PWM Control Register 3 | PWC3 | R/W | Stepping Motor Controller 3 | 0 0 0 0 0 _ _ 0$_B$ |
| 65$_H$ | Reserved | | | | |
| 66$_H$ | Timer Data Register (low-order) | TCDT | R/W | 16-bit Free-run Timer | 0 0 0 0 0 0 0 0$_B$ |
| 67$_H$ | Timer Data Register (high-order) | TCDT | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 68$_H$ | Timer Control Status Register | TCCS | R/W | | 0 0 0 0 0 0 0 0$_B$ |
| 69$_H$ to 6E$_H$ | Reserved | | | | |

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| Address | Register | Abbreviation | Access | Peripheral | Initial value |
|---|---|---|---|---|---|
| 192C$_H$ | Output Compare Register 2 (low-order) | OCCP2 | R/W | Output Compare 2/3 | XXXXXXXX$_B$ |
| 192D$_H$ | Output Compare Register 2 (high-order) | OCCP2 | R/W | | XXXXXXXX$_B$ |
| 192E$_H$ | Output Compare Register 3 (low-order) | OCCP3 | R/W | | XXXXXXXX$_B$ |
| 192F$_H$ | Output Compare Register 3 (high-order) | OCCP3 | R/W | | XXXXXXXX$_B$ |
| 1930$_H$ to 19FF$_H$ | Reserved | | | | |
| 1A00$_H$ to 1AFF$_H$ | CAN Controller. Refer to section about CAN Controller | | | | |
| 1B00$_H$ to 1BFF$_H$ | CAN Controller. Refer to section about CAN Controller | | | | |
| 1C00$_H$ to 1EFF$_H$ | Reserved | | | | |
| 1FF0$_H$ | Program Address Detection Register 0 (low-order) | PADR0 | R/W | Address Match Detection Function | XXXXXXXX$_B$ |
| 1FF1$_H$ | Program Address Detection Register 0 (middle-order) | | | | XXXXXXXX$_B$ |
| 1FF2$_H$ | Program Address Detection Register 0 (high-order) | | | | XXXXXXXX$_B$ |
| 1FF3$_H$ | Program Address Detection Register 1 (low-order) | PADR1 | R/W | | XXXXXXXX$_B$ |
| 1FF4$_H$ | Program Address Detection Register 1 (middle-order) | | | | XXXXXXXX$_B$ |
| 1FF5$_H$ | Program Address Detection Register 1 (high-order) | | | | XXXXXXXX$_B$ |
| 1FF6$_H$ to 1FFF$_H$ | Reserved | | | | |

■ Description for Read/Write
R/W : Readable/writable
R : Read only
W : Write only

■ Description of initial value
0 : the initial value of this bit is "0".
1 : the initial value of this bit is "1".
X : the initial value of this bit is undefined.
_ : this bit is unused. the initial value is undefined.

Note: : Addresses in the range of 0000$_H$ to 00FF$_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 001A2C$_H$ | ID register 3 | IDR3 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 001A2D$_H$ | | | | |
| 001A2E$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 001A2F$_H$ | | | | |
| 001A30$_H$ | ID register 4 | IDR4 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 001A31$_H$ | | | | |
| 001A32$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 001A33$_H$ | | | | |
| 001A34$_H$ | ID register 5 | IDR5 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 001A35$_H$ | | | | |
| 001A36$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 001A37$_H$ | | | | |
| 001A38$_H$ | ID register 6 | IDR6 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 001A39$_H$ | | | | |
| 001A3A$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 001A3B$_H$ | | | | |
| 001A3C$_H$ | ID register 7 | IDR7 | R/W | XXXXXXXX XXXXXXXX$_B$ |
| 001A3D$_H$ | | | | |
| 001A3E$_H$ | | | | XXXXX--- XXXXXXXX$_B$ |
| 001A3F$_H$ | | | | |

*(Continued)*

*(Continued)*

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 001A40H | ID register 8 | IDR8 | R/W | XXXXXXXX XXXXXXXXB |
| 001A41H | | | | |
| 001A42H | | | | XXXXX--- XXXXXXXXB |
| 001A43H | | | | |
| 001A44H | ID register 9 | IDR9 | R/W | XXXXXXXX XXXXXXXXB |
| 001A45H | | | | |
| 001A46H | | | | XXXXX--- XXXXXXXXB |
| 001A47H | | | | |
| 001A48H | ID register 10 | IDR10 | R/W | XXXXXXXX XXXXXXXXB |
| 001A49H | | | | |
| 001A4AH | | | | XXXXX--- XXXXXXXXB |
| 001A4BH | | | | |
| 001A4CH | ID register 11 | IDR11 | R/W | XXXXXXXX XXXXXXXXB |
| 001A4DH | | | | |
| 001A4EH | | | | XXXXX--- XXXXXXXXB |
| 001A4FH | | | | |
| 001A50H | ID register 12 | IDR12 | R/W | XXXXXXXX XXXXXXXXB |
| 001A51H | | | | |
| 001A52H | | | | XXXXX--- XXXXXXXXB |
| 001A53H | | | | |
| 001A54H | ID register 13 | IDR13 | R/W | XXXXXXXX XXXXXXXXB |
| 001A55H | | | | |
| 001A56H | | | | XXXXX--- XXXXXXXXB |
| 001A57H | | | | |
| 001A58H | ID register 14 | IDR14 | R/W | XXXXXXXX XXXXXXXXB |
| 001A59H | | | | |
| 001A5AH | | | | XXXXX--- XXXXXXXXB |
| 001A5BH | | | | |
| 001A5CH | ID register 15 | IDR15 | R/W | XXXXXXXX XXXXXXXXB |
| 001A5DH | | | | |
| 001A5EH | | | | XXXXX--- XXXXXXXXB |
| 001A5FH | | | | |

### 9.3 List of Message Buffers (DLC Registers and Data Registers)

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 001A60H | DLC register 0 | DLCR0 | R/W | ----XXXXB |
| 001A61H | | | | |
| 001A62H | DLC register 1 | DLCR1 | R/W | ----XXXXB |
| 001A63H | | | | |
| 001A64H | DLC register 2 | DLCR2 | R/W | ----XXXXB |
| 001A65H | | | | |
| 001A66H | DLC register 3 | DLCR3 | R/W | ----XXXXB |
| 001A67H | | | | |
| 001A68H | DLC register 4 | DLCR4 | R/W | ----XXXXB |
| 001A69H | | | | |
| 001A6AH | DLC register 5 | DLCR5 | R/W | ----XXXXB |
| 001A6BH | | | | |
| 001A6CH | DLC register 6 | DLCR6 | R/W | ----XXXXB |
| 001A6DH | | | | |
| 001A6EH | DLC register 7 | DLCR7 | R/W | ----XXXXB |
| 001A6FH | | | | |
| 001A70H | DLC register 8 | DLCR8 | R/W | ----XXXX |
| 001A71H | | | | |
| 001A72H | DLC register 9 | DLCR9 | R/W | ----XXXXB |
| 001A73H | | | | |
| 001A74H | DLC register 10 | DLCR10 | R/W | ----XXXXB |
| 001A75H | | | | |
| 001A76H | DLC register 11 | DLCR11 | R/W | ----XXXXB |
| 001A77H | | | | |
| 001A78H | DLC register 12 | DLCR12 | R/W | ----XXXXB |
| 001A79H | | | | |
| 001A7AH | DLC register 13 | DLCR13 | R/W | ----XXXXB |
| 001A7BH | | | | |
| 001A7CH | DLC register 14 | DLCR14 | R/W | ----XXXXB |
| 001A7DH | | | | |
| 001A7EH | DLC register 15 | DLCR15 | R/W | ----XXXXB |
| 001A7FH | | | | |
| 001A80H to 001A87H | Data register 0 (8 bytes) | DTR0 | R/W | XXXXXXXXB to XXXXXXXXB |

*(Continued)*

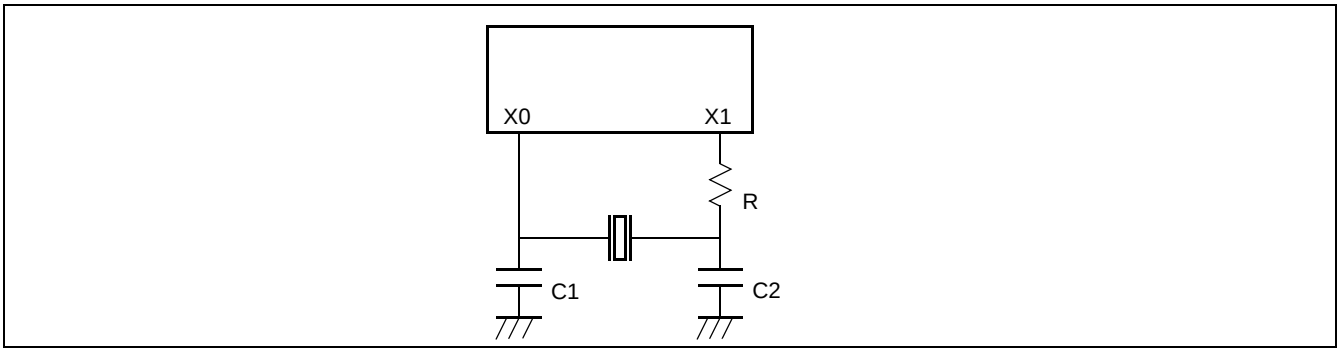
*(Continued)*

| Address | Register | Abbreviation | Access | Initial Value |
|---|---|---|---|---|
| 001A88H to 001A8FH | Data register 1 (8 bytes) | DTR1 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001A90H to 001A97H | Data register 2 (8 bytes) | DTR2 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001A98H to 001A9FH | Data register 3 (8 bytes) | DTR3 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AA0H to 001AA7H | Data register 4 (8 bytes) | DTR4 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AA8H to 001AAFH | Data register 5 (8 bytes) | DTR5 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AB0H to 001AB7H | Data register 6 (8 bytes) | DTR6 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AB8H to 001ABFH | Data register 7 (8 bytes) | DTR7 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AC0H to 001AC7H | Data register 8 (8 bytes) | DTR8 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AC8H to 001ACFH | Data register 9 (8 bytes) | DTR9 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AD0H to 001AD7H | Data register 10 (8 bytes) | DTR10 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AD8H to 001ADFH | Data register 11 (8 bytes) | DTR11 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AE0H to 001AE7H | Data register 12 (8 bytes) | DTR12 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AE8H to 001AEFH | Data register 13 (8 bytes) | DTR13 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AF0H to 001AF7H | Data register 14 (8 bytes) | DTR14 | R/W | XXXXXXXXB to XXXXXXXXB |
| 001AF8H to 001AFFH | Data register 15 (8 bytes) | DTR15 | R/W | XXXXXXXXB to XXXXXXXXB |

Notes:

- For a peripheral module with two interrupt for a single interrupt number, both interrupt request flags are cleared by the EI²OS interrupt clear signal.
- At the end of EI²OS, the EI²OS clear signal will be asserted for all the interrupt flags assigned to the same interrupt number. If one interrupt flag starts the EI²OS and in the meantime another interrupt flag is set by hardware event, the later event is lost because the flag is cleared by the EI²OS clear signal caused by the first event. So it is recommended not to use the EI²OS for this interrupt number.
- If EI²OS is enabled, EI²OS is initiated when one of the two interrupt signals in the same interrupt control register (ICR) is asserted. This means that different interrupt sources share the same EI²OS Descriptor which should be unique for each interrupt source. For this reason, when one interrupt source uses the EI²OS, the other interrupt should be disabled.

■ Example of Oscillation circuit



*11.4.3 Power On Reset*

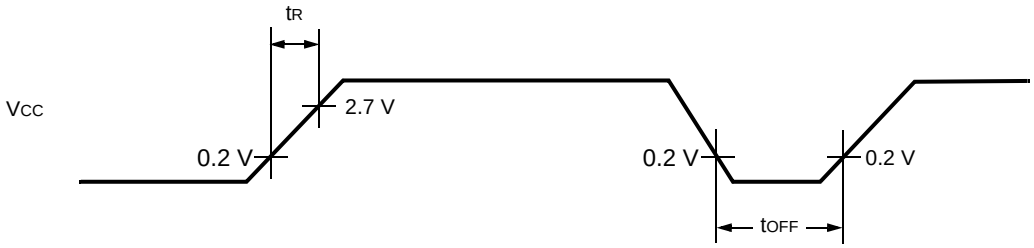
($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Power on rise time | $t_R$ | $V_{CC}$ | — | 0.05 | 30 | ms | * |
| Power off time | $t_{OFF}$ | $V_{CC}$ | | 50 | — | ms | Due to repetitive operation |

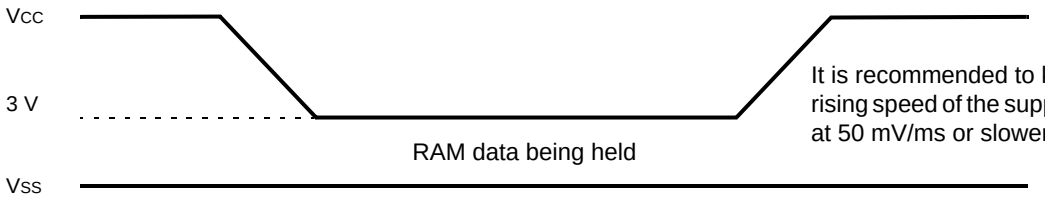
*: $V_{CC}$ must be kept lower than 0.2 V before power-on.

Notes:

- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn on the power supply using the above values.




Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or less per second, however, you can use the PLL clock.



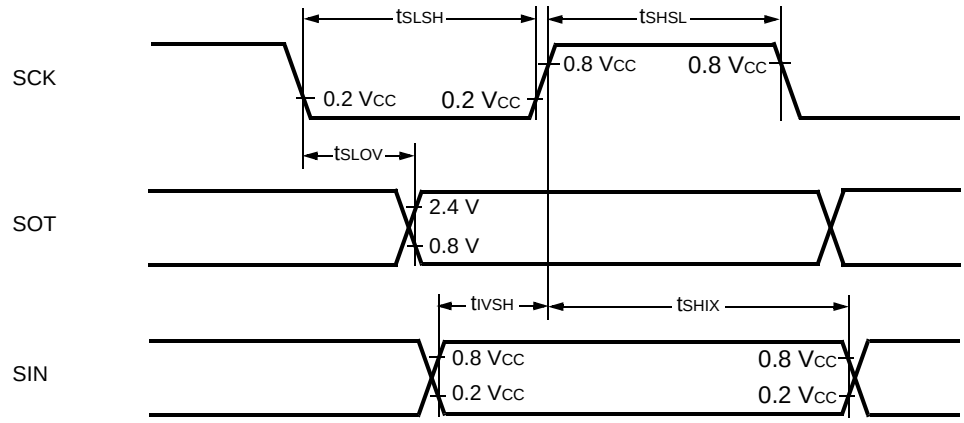

It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

*11.4.4 UART0/1, Serial I/O Timing*

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Serial clock cycle time | $t_{SCYC}$ | SCK0 to SCK2 | Internal clock operation output pins are $C_L$ = 80 pF + 1 TTL. | 8 $t_{CP}$ | — | ns | |
| SCK ↓ ⇒ SOT delay time | $t_{SLOV}$ | SCK0 to SCK2, SOT0 to SOT2 | | –80 | 80 | ns | |
| Valid SIN ⇒ SCK ↑ | $t_{IVSH}$ | SCK0 to SCK2, SIN0 to SIN2 | | 100 | — | ns | |
| SCK ↑ ⇒ Valid SIN hold time | $t_{SHIX}$ | SCK0 to SCK2, SIN0 to SIN2 | | 60 | — | ns | |

• **External Shift Clock Mode**

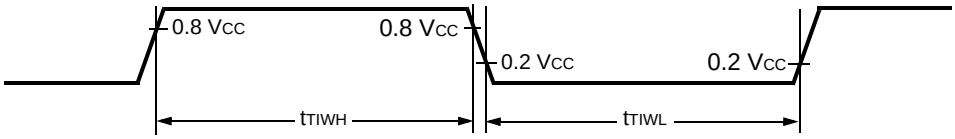



**(5) Timer Input Timing**

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TIWH}$ | TIN0, TIN1 | — | 4 $t_{CP}$ | — | ns | |
| | $t_{TIWL}$ | IN0 to IN3 | | | | | |

• **Timer Input Timing**

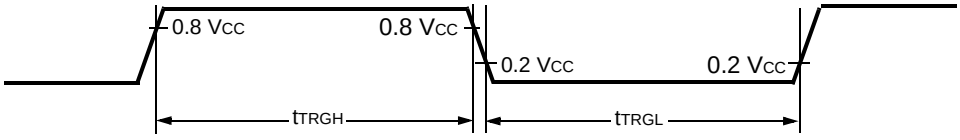



*11.4.5 Trigger Input Timing*

($V_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | | Min | Max | | |
| Input pulse width | $t_{TRGH}$ $t_{TRGL}$ | INT0 to INT7, ADTG | — | 5 $t_{CP}$ | — | ns | Under normal operation |
| | | | | 1 | — | µs | In stop mode |

- **Trigger Input Timing**




*11.4.6 Slew Rate High Current Outputs (MB90598G, MB90F598G only)*

($V_{CC}$ = 5.0 V±10 %, $V_{SS}$ = $AV_{SS}$ = 0.0 V, $T_A$ = −40 °C to +85 °C)

| Parameter | Symbol | Pin name | Condition | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | | |
| Output Rise/Fall time | $t_{R2}$<br>$t_{F2}$ | Port P70 to P77,<br>Port P80 to P87 | — | 15 | 40 | 150 | ns | |

- Slew Rate Output Timing


$V_H = V_{OL2} + 0.1 \times (V_{OH2} - V_{OL2})$
$V_L = V_{OL2} + 0.9 \times (V_{OH2} - V_{OL2})$

## 11.5 A/D Converter

($V_{CC}$ = $AV_{CC}$ = 5.0 V±10%, $V_{SS}$ = $AV_{SS}$ = 0.0 V,3.0 V ≤ AVRH − AVRL, $T_A$ = −40 °C to +85 °C)

| Parameter | Sym-bol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Resolution | — | — | — | | 10 | bit | |
| Conversion error | — | — | — | — | ±5.0 | LSB | |
| Nonlinearity error | — | — | — | — | ±2.5 | LSB | |
| Differential linearity error | — | — | — | — | ±1.9 | LSB | |
| Zero transition voltage | $V_{OT}$ | AN0 to AN7 | AVRL − 3.5 LSB | AVRL + 0.5 LSB | AVRL + 4.5 LSB | V | |
| Full scale transition voltage | $V_{FST}$ | AN0 to AN7 | AVRH − 6.5 LSB | AVRH − 1.5 LSB | AVRH + 1.5 LSB | V | |
| Conversion time | — | — | — | 352$t_{CP}$ | — | ns | |
| Sampling time | — | — | — | 64$t_{CP}$ | — | ns | |
| Analog port input current | $I_{AIN}$ | AN0 to AN7 | −10 | — | 10 | µA | |
| Analog input voltage range | $V_{AIN}$ | AN0 to AN7 | AVRL | — | AVRH | V | |

| Parameter | Symbol | Pin name | Value | | | Unit | Remarks |
|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | | |
| Reference voltage range | — | AVRH | AVRL + 3.0 | — | $AV_{CC}$ | V | |
| | — | AVRL | 0 | — | AVRH − 3.0 | V | |
| Power supply current | $I_A$ | $AV_{CC}$ | — | 5 | — | mA | |
| | $I_{AH}$ | $AV_{CC}$ | — | — | 5 | µA | * |
| Reference voltage current | $I_R$ | AVRH | — | 400 | 600 | µA | MB90V595G, MB90F598G |
| | | | — | 140 | 600 | µA | MB90598G |
| | $I_{RH}$ | AVRH | — | — | 5 | µA | * |
| Offset between input channels | — | AN0 to AN7 | — | — | 4 | LSB | |

* : When not operating A/D converter, this is the current ($V_{CC}$ = $AV_{CC}$ = AVRH = 5.0 V) when the CPU is stopped.

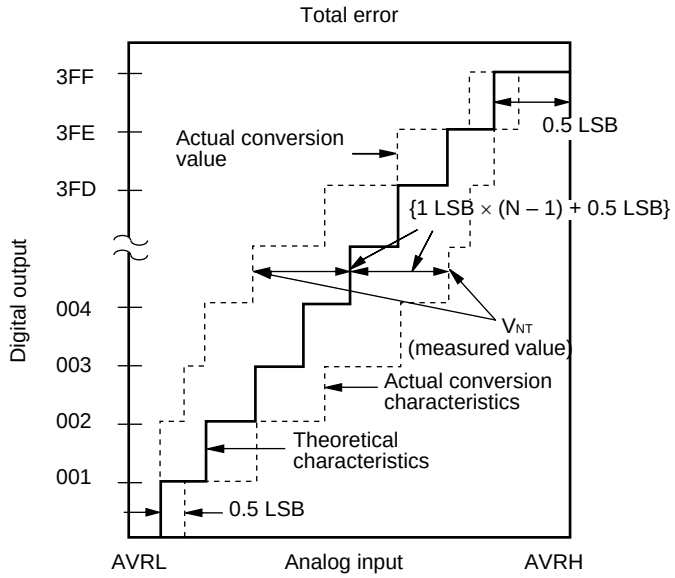
### 11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error: The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error: The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error: The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.




1 LSB = (Theoretical value) $\frac{AVRH - AVRL}{1024}$ [V]

Total error for digital output N = $\frac{V_{NT} - \{1\ LSB \times (N - 1) + 0.5\ LSB\}}{1\ LSB}$ [LSB]

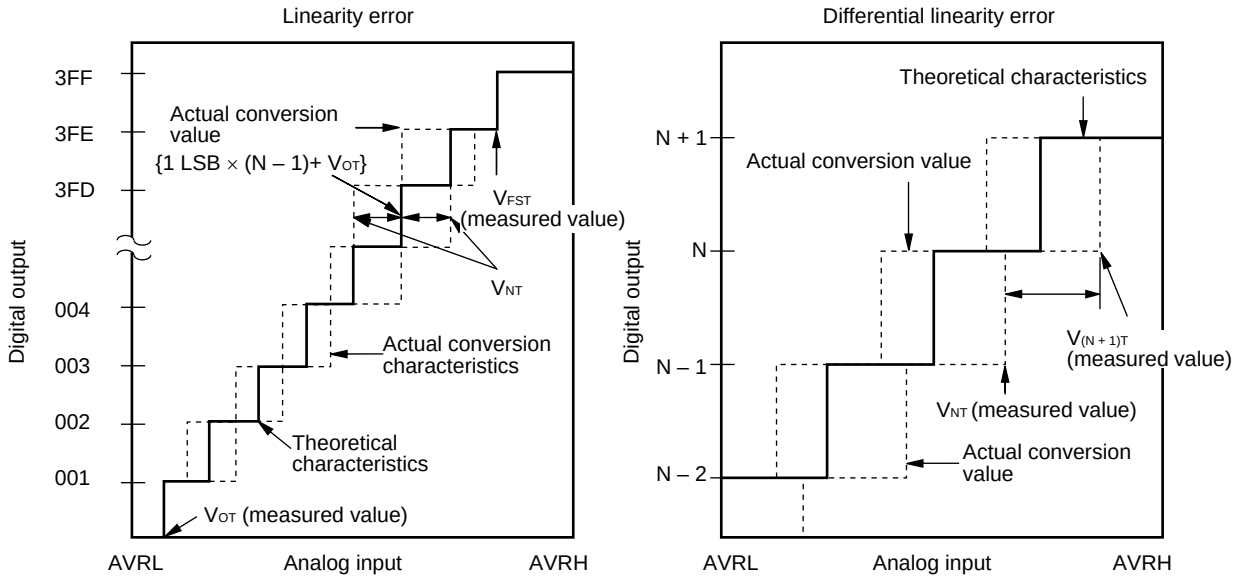
$V_{OT}$ (Theoretical value) = AVRL + 0.5 LSB[V]

$V_{NT}$: Voltage at a transition of digital output from (N – 1) to N

$V_{FST}$ (Theoretical value) = AVRH – 1.5 LSB[V]

*(Continued)*

*(Continued)*




$$\text{Linearity error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linearity error of digital N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\ \text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

$V_{OT}$: Voltage at transition of digital output from "$000_H$" to "$001_H$"
$V_{FST}$: Voltage at transition of digital output from "$3FE_H$" to "$3FF_H$"

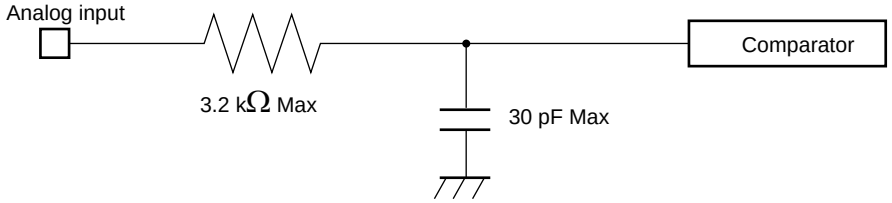
### 11.7 Notes on Using A/D Converter

Select the output impedance value for the external circuit of analog input according to the following conditions,:

- Output impedance values of the external circuit of 15 kΩ or lower are recommended.
- When capacitors are connected to external pins, the capacitance of several thousand times the internal capacitor value is recommended to minimized the effect of voltage distribution between the external capacitor and internal capacitor.

When the output impedance of the external circuit is too high, the sampling period for analog voltages may not be sufficient (sampling period = 4.00 μs @machine clock of 16 MHz).

- **Equipment of analog input circuit model**




**■ Error**

The smaller the | AVRH − AVRL |, the greater the error would become relatively.

### 11.8 Flash memory

■ Erase and programming performance

| Parameter | Condition | Value | | | Unit | Remarks | |
|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | | | |
| Sector erase time | $T_A = +25\ ^{\circ}C$, $V_{CC} = 5.0$ V | — | 1 | 15 | s | MB90F598G | Excludes 00H programming prior erasure |
| Chip erase time | | — | 5 | — | s | MB90F598G | Excludes 00H programming prior |
| Word (16-bit) programming time | | — | 16 | 3600 | µs | MB90F598G | Excludes system-level overhead |
| Erase/Program cycle | — | 10000 | — | — | cycle | | |