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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	CANbus, EBI/EMI, SCI, Serial I/O, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	78
Program Memory Size	128KB (128K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-BQFP
Supplier Device Package	100-QFP (14x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90598gpf-gs-198e1

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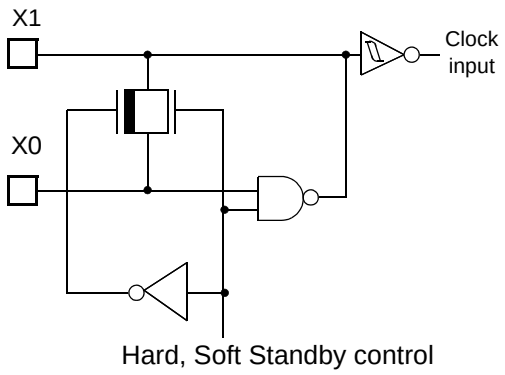
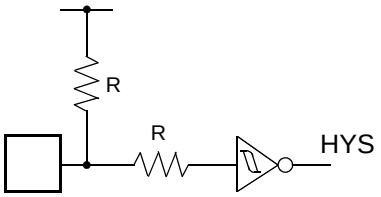
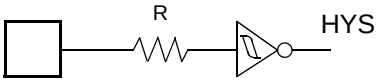
3. Pin Description

Pin no.	Pin name	Circuit type	Function
82	X0	A	Oscillator pin
83	X1		
77	$\overline{RST}$	B	Reset input
52	$\overline{HST}$	C	Hardware standby input
85 to 88	P00 to P03	G	General purpose IO
	IN0 to IN3		Inputs for the Input Captures
89 to 92	P04 to P07	G	General purpose IO
	OUT0 to OUT3		Outputs for the Output Compares.
93 to 98	P10 to P15	D	General purpose IO
	PPG0 to PPG5		Outputs for the Programmable Pulse Generators
99	P16	D	General purpose IO
	TIN1		TIN input for the 16-bit Reload Timer 1
100	P17	D	General purpose IO
	TOT1		TOT output for the 16-bit Reload Timer 1
1 to 8	P20 to P27	G	General purpose IO
9 to 10	P30 to P31	G	General purpose IO
12 to 16	P32 to P36	G	General purpose IO
17	P37	D	General purpose IO
18	P40	G	General purpose IO
	SOT0		SOT output for UART 0
19	P41	G	General purpose IO
	SCK0		SCK input/output for UART 0
20	P42	G	General purpose IO
	SIN0		SIN input for UART 0
21	P43	G	General purpose IO
	SIN1		SIN input for UART 1
22	P44	G	General purpose IO
	SCK1		SCK input/output for UART 1
24	P45	G	General purpose IO
	SOT1		SOT output for UART 1
25	P46	G	General purpose IO
	SOT2		SOT output for the Serial IO
26	P47	G	General purpose IO
	SCK2		SCK input/output for the Serial IO

Pin no.	Pin name	Circuit type	Function
76	P92	D	General purpose IO
	INT0		External interrupt input for INT0
78 to 80	P93 to P95	D	General purpose IO
	INT1 to INT3		External interrupt input for INT1 to INT3
58, 68	DV_{CC}	—	Dedicated power supply pins for the high current output buffers (Pin No. 54 to 72)
53, 63, 73	DV_{SS}	—	Dedicated ground pins for the high current output buffers (Pin No. 54 to 72)
34	AV_{CC}	Power supply	Dedicated power supply pin for the A/D Converter
37	AV_{SS}	Power supply	Dedicated ground pin for the A/D Converter
35	AVRH	Power supply	Upper reference voltage input for the A/D Converter
36	AVRL	Power supply	Lower reference voltage input for the A/D Converter
49, 50	MD0 MD1	C	Operating mode selection input pins. These pins should be connected to V_{CC} or V_{SS}.
51	MD2	H	Operating mode selection input pin. This pin should be connected to V_{CC} or V_{SS}.
27	C	—	External capacitor pin. A capacitor of 0.1μF should be connected to this pin and V_{SS}.
23, 84	V_{CC}	Power supply	Power supply pins (5.0 V).
11, 42, 81	V_{SS}	Power supply	Ground pins (0.0 V).

4. I/O Circuit Type

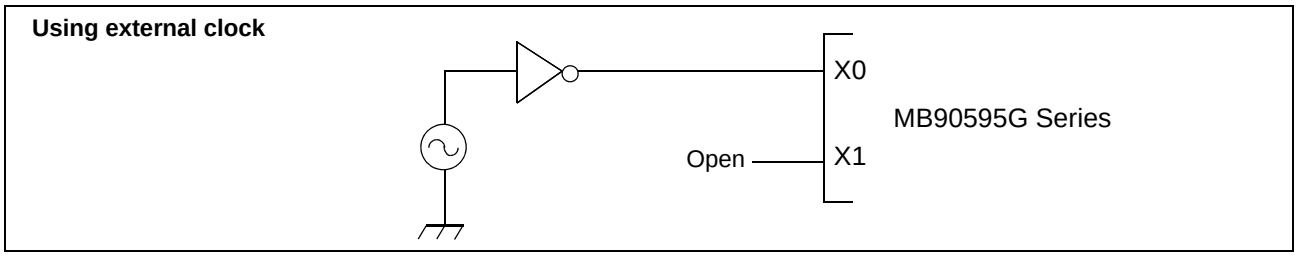
Circuit Type	Circuit	Remarks
A		■ Oscillation feedback resistor: 1 MΩ approx.
B		■ Hysteresis input with pull-up Resistor: 50 kΩ approx.
C		■ Hysteresis input

5. Handling Devices

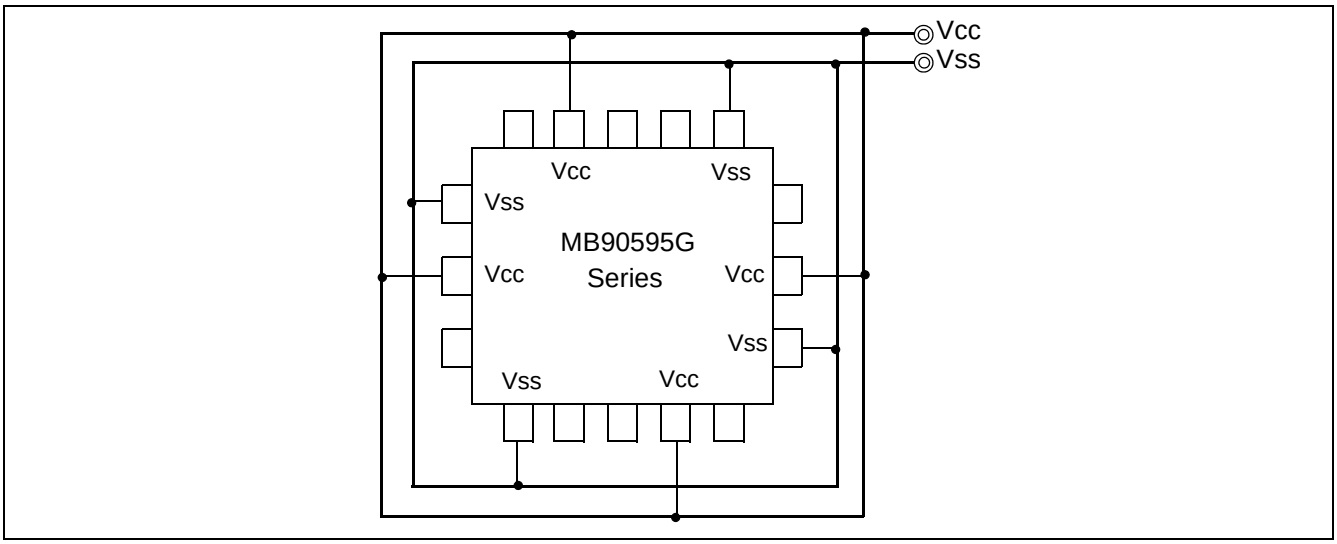
(1) Make Sure that the Voltage not Exceed the Maximum Rating (to Avoid a Latch-up).
In CMOS ICs, a latch-up phenomenon is caused when an voltage exceeding V_{CC} or an voltage below V_{SS} is applied to input or output pins or a voltage exceeding the rating is applied across V_{CC} and V_{SS}.
When a latch-up is caused, the power supply current may be dramatically increased causing resultant thermal break-down of devices. To avoid the latch-up, make sure that the voltage not exceed the maximum rating.
In turning on/turning off the analog power supply, make sure the analog power voltage (AV_{CC}, AVRH, DV_{CC}) and analog input voltages not exceed the digital voltage (V_{CC}).

(2) Treatment of Unused Pins
Unused input pins left open may cause abnormal operation, or latch-up leading to permanent damage. Unused input pins should be pulled up or pulled down through at least 2 kΩ resistance.
Unused input/output pins may be left open in output state, but if such pins are in input state they should be handled in the same way as input pins.

(3) Using external clock
In using the external clock, drive X0 pin only and leave X1 pin unconnected.



(4) Power supply pins (Vcc/Vss)
In products with multiple V_{cc} or V_{ss} pins, pins with the same potential are internally connected in the device to avoid abnormal operations including latch-up. However, you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating (See the figure below.)
Make sure to connect V_{cc} and V_{ss} pins via lowest impedance to power lines.
It is recommended to provide a bypass capacitor of around 0.1 μF between V_{cc} and V_{ss} pins near the device.



(5) Pull-up/down resistors
The MB90595G Series does not support internal pull-up/down resistors. Use external components where needed.

(6) Crystal Oscillator Circuit
Noises around X0 or X1 pins may cause abnormal operations. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator (or ceramic resonator) and ground lines, and make sure that lines of oscillation circuit not cross the lines of other circuits.
A printed circuit board artwork surrounding the X0 and X1 pins with ground area for stabilizing the operation is highly recommended.

(7) Turning-on Sequence of Power Supply to A/D Converter and Analog Inputs
Make sure to turn on the A/D converter power supply (AV_{CC}, AVRH, AVRL) and analog inputs (AN0 to AN7) after turning-on the digital power supply (V_{CC}).
Turn-off the digital power after turning off the A/D converter supply and analog inputs. In this case, make sure that the voltage does not exceed AVRH or AV_{CC} (turning on/off the analog and digital power supplies simultaneously is acceptable).

(8) Connection of Unused Pins of A/D Converter
Connect unused pins of A/D converter to $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = $DV_{CC} = V_{SS}$.

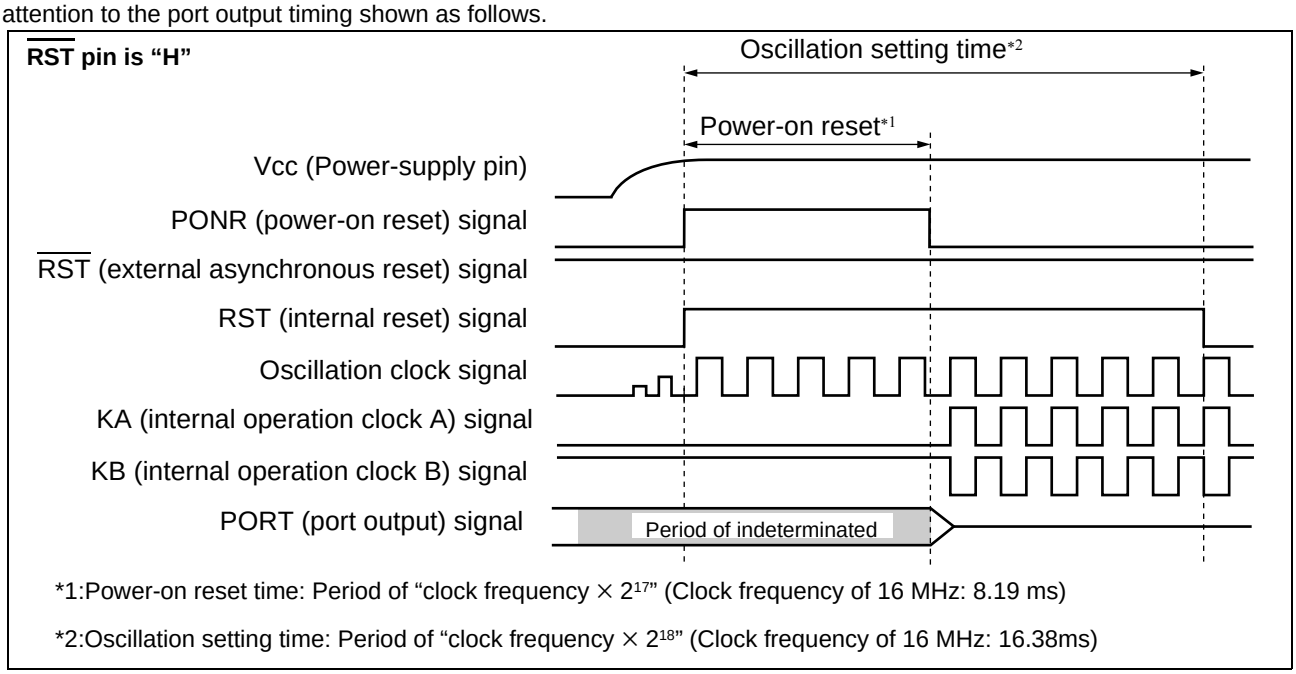
(9) N.C. Pin
The N.C. (internally connected) pin must be opened for use.

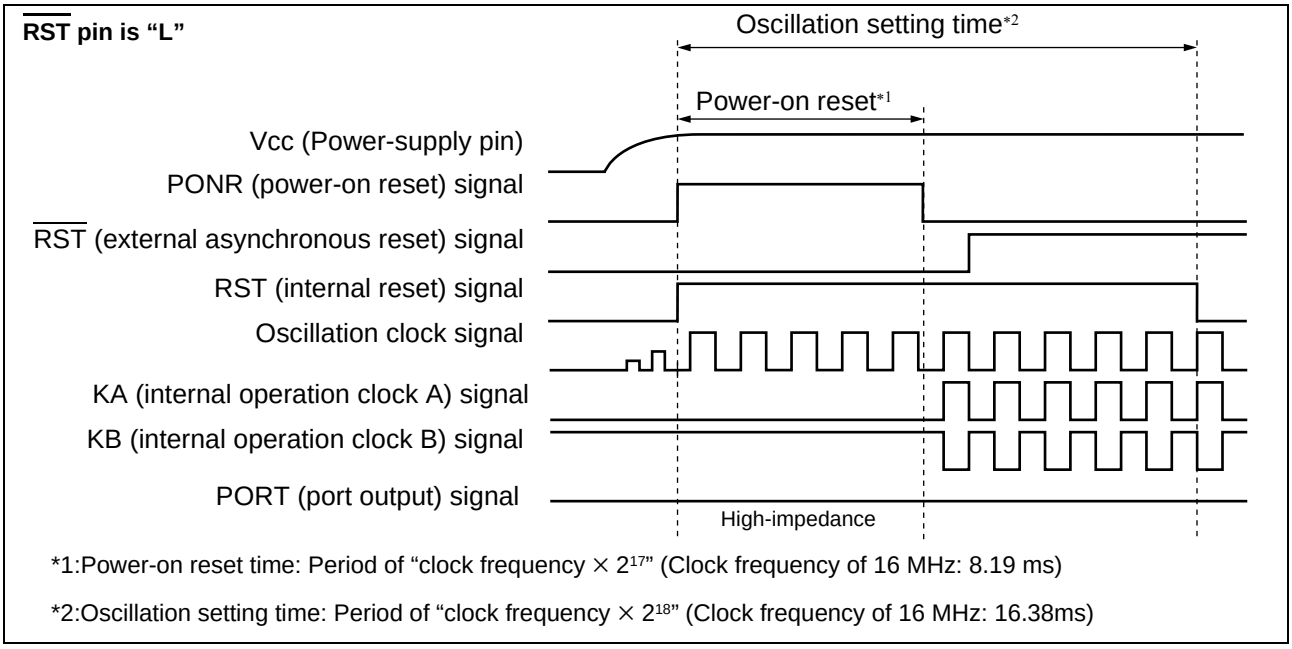
(10) Notes on Energization
To prevent the internal regulator circuit from malfunctioning, set the voltage rise time during energization at 50 µs or more (0.2 V to 2.7 V).

(11) Indeterminate outputs from ports 0 and 1 (MB90V595G only)
During oscillation setting time of step-down circuit (during a power-on reset) after the power is turned on, the outputs from ports 0 and 1 become following state.

- If $\overline{RST}$ pin is “H”, the outputs become indeterminate.
- If $\overline{RST}$ pin is “L”, the outputs become high-impedance.

Pay attention to the port output timing shown as follows.





(12) Initialization

The device contains internal registers which are initialized only by a power-on reset. To initialize these registers, please turn on the power again.

(13) Directions of "DIV A, Ri" and "DIVW A, RWi" instructions

In the signed multiplication and division instructions ("DIV A, Ri" and "DIVW A, RWi"), the value of the corresponding bank register (DTB, ADB, USB, SSB) is set in "00_H".

If the values of the corresponding bank register (DTB,ADB,USB,SSB) are set to other than "00_H", the remainder by the execution result of the instruction is not stored in the register of the instruction operand.

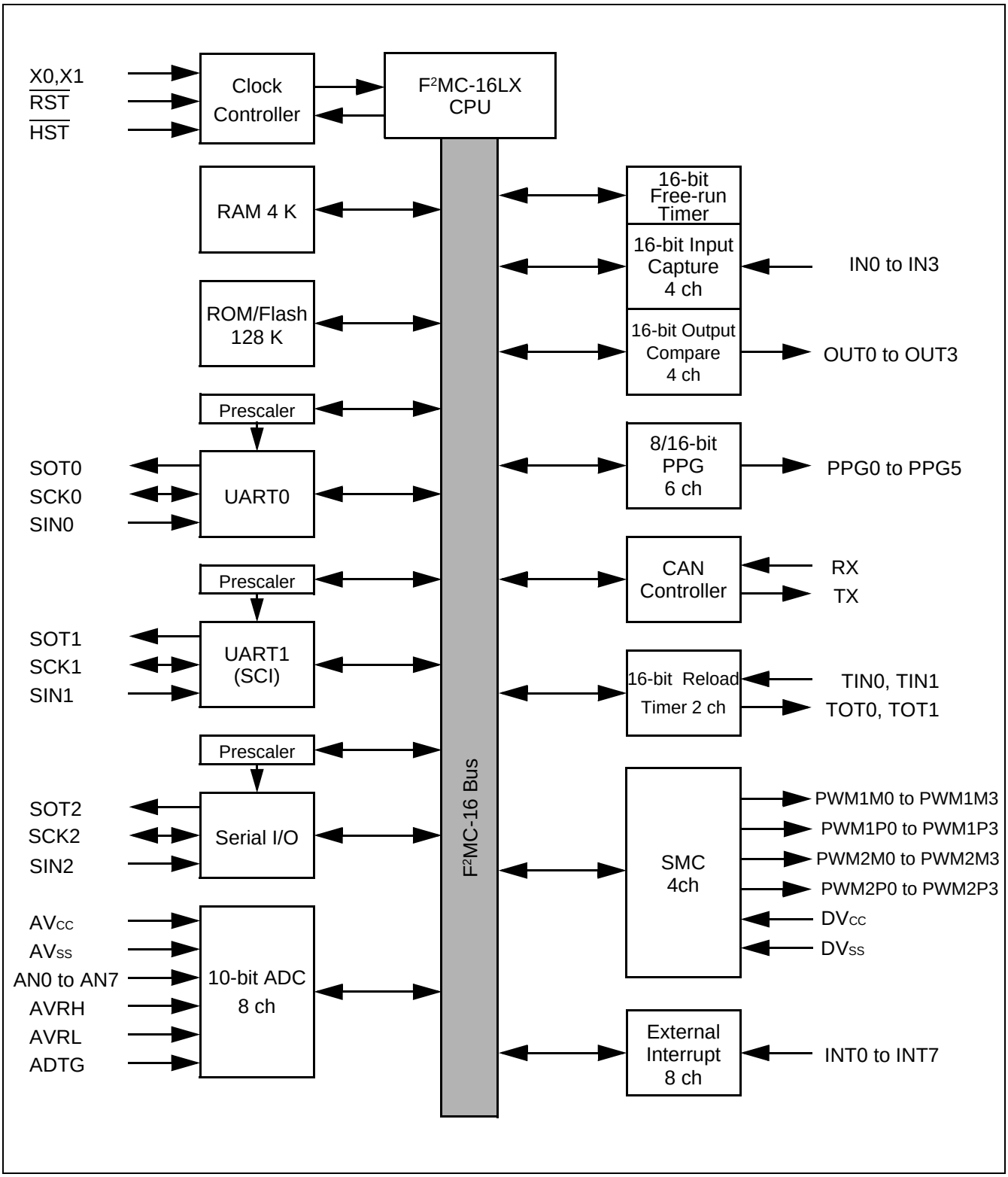
(14) Using REALOS

The use of EI^2OS is not possible with the REALOS real time operating system.

(15) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the automatic oscillating circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

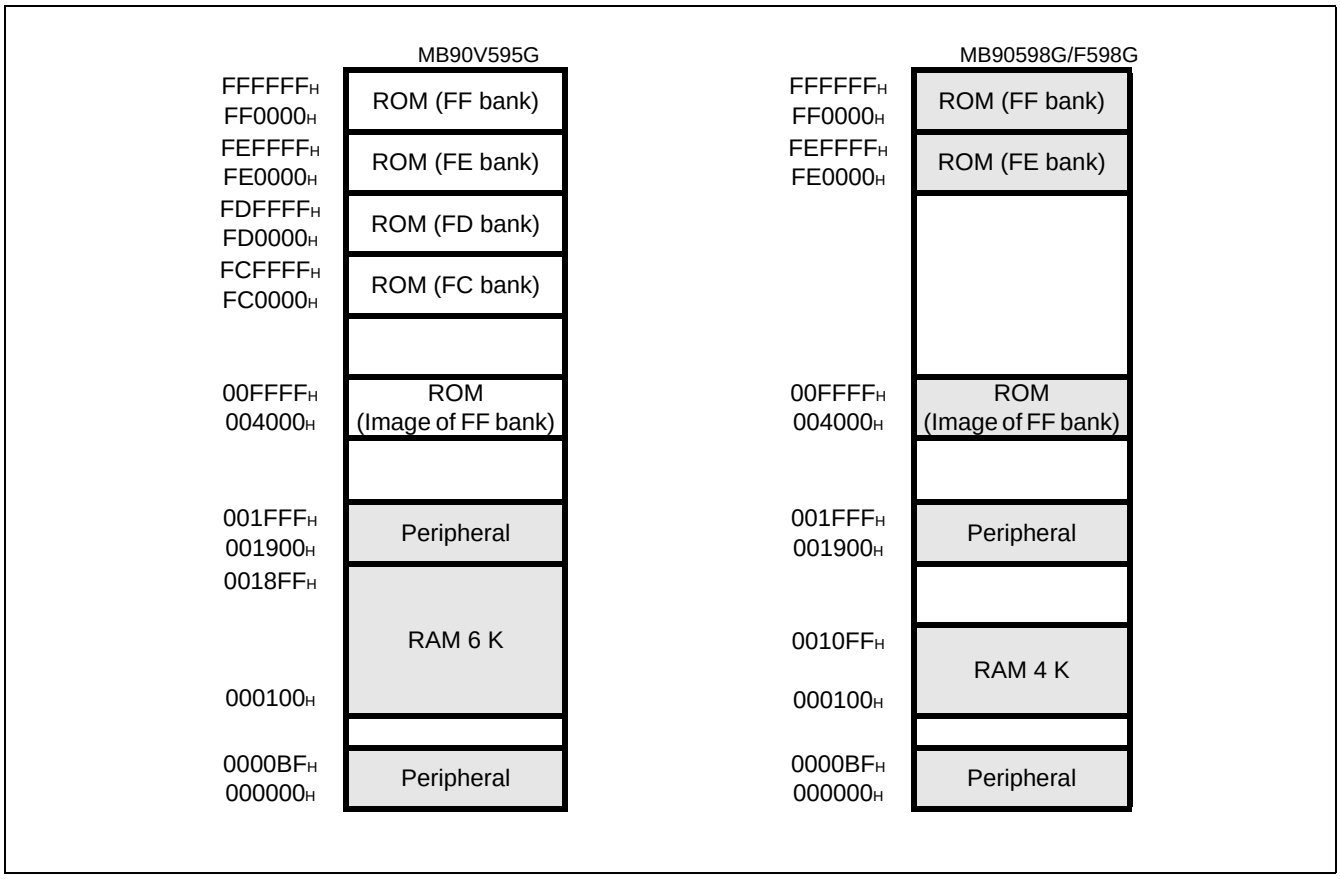
6. Block Diagram



7. Memory Space

The memory space of the MB90595G Series is shown below

Figure 1. Memory space map



Note: : The ROM data of bank FF is reflected in the upper address of bank 00, realizing effective use of the C compiler small model. The lower 16-bit of bank FF and the lower 16-bit of bank 00 are assigned to the same address, enabling reference of the table on the ROM without stating “far”.
For example, if an attempt has been made to access 00C000H , the contents of the ROM at FFC000H are accessed. Since the ROM area of the FF bank exceeds 48 Kbytes, the whole area cannot be reflected in the image for the 00 bank. The ROM data at FF4000H to FFFFFFH looks, therefore, as if it were the image for 004000H to 00FFFFH. Thus, it is recommended that the ROM data table be stored in the area of FF4000H to FFFFFFH.

(Continued)

Address	Register	Abbreviation	Access	Peripheral	Initial value
$192C_H$	Output Compare Register 2 (low-order)	OCCP2	R/W	Output Compare 2/3	XXXXXXXX_B
$192D_H$	Output Compare Register 2 (high-order)	OCCP2	R/W		XXXXXXXX_B
$192E_H$	Output Compare Register 3 (low-order)	OCCP3	R/W		XXXXXXXX_B
$192F_H$	Output Compare Register 3 (high-order)	OCCP3	R/W		XXXXXXXX_B
1930_H to $19FF_H$	Reserved				
$1A00_H$ to $1AFF_H$	CAN Controller. Refer to section about CAN Controller				
$1B00_H$ to $1BFF_H$	CAN Controller. Refer to section about CAN Controller				
$1C00_H$ to $1EFF_H$	Reserved				
$1FF0_H$	Program Address Detection Register 0 (low-order)	PADR0	R/W	Address Match Detection Function	XXXXXXXX_B
$1FF1_H$	Program Address Detection Register 0 (middle-order)				XXXXXXXX_B
$1FF2_H$	Program Address Detection Register 0 (high-order)				XXXXXXXX_B
$1FF3_H$	Program Address Detection Register 1 (low-order)	PADR1	R/W		XXXXXXXX_B
$1FF4_H$	Program Address Detection Register 1 (middle-order)				XXXXXXXX_B
$1FF5_H$	Program Address Detection Register 1 (high-order)				XXXXXXXX_B
$1FF6_H$ to $1FFF_H$	Reserved				

■ Description for Read/Write
R/W : Readable/writable
R : Read only
W : Write only

■ Description of initial value
0 : the initial value of this bit is "0".
1 : the initial value of this bit is "1".
X : the initial value of this bit is undefined.
_ : this bit is unused. the initial value is undefined.

Note: : Addresses in the range of 0000_H to $00FF_H$, which are not listed in the table, are reserved for the primary functions of the MCU. A read access to these reserved addresses results in reading “X”, and any write access should not be performed.

9.3 List of Message Buffers (DLC Registers and Data Registers)

Address	Register	Abbreviation	Access	Initial Value
001A60H 001A61H	DLC register 0	DLCR0	R/W	----XXXXB
001A62H 001A63H	DLC register 1	DLCR1	R/W	----XXXXB
001A64H 001A65H	DLC register 2	DLCR2	R/W	----XXXXB
001A66H 001A67H	DLC register 3	DLCR3	R/W	----XXXXB
001A68H 001A69H	DLC register 4	DLCR4	R/W	----XXXXB
001A6AH 001A6BH	DLC register 5	DLCR5	R/W	----XXXXB
001A6CH 001A6DH	DLC register 6	DLCR6	R/W	----XXXXB
001A6EH 001A6FH	DLC register 7	DLCR7	R/W	----XXXXB
001A70H 001A71H	DLC register 8	DLCR8	R/W	----XXXX
001A72H 001A73H	DLC register 9	DLCR9	R/W	----XXXXB
001A74H 001A75H	DLC register 10	DLCR10	R/W	----XXXXB
001A76H 001A77H	DLC register 11	DLCR11	R/W	----XXXXB
001A78H 001A79H	DLC register 12	DLCR12	R/W	----XXXXB
001A7AH 001A7BH	DLC register 13	DLCR13	R/W	----XXXXB
001A7CH 001A7DH	DLC register 14	DLCR14	R/W	----XXXXB
001A7EH 001A7FH	DLC register 15	DLCR15	R/W	----XXXXB
001A80H to 001A87H	Data register 0 (8 bytes)	DTR0	R/W	XXXXXXXXB to XXXXXXXXB

(Continued)

(Continued)

Address	Register	Abbreviation	Access	Initial Value
$001A88_H$ to $001A8F_H$	Data register 1 (8 bytes)	DTR1	R/W	XXXXXXXX_B to XXXXXXXX_B
$001A90_H$ to $001A97_H$	Data register 2 (8 bytes)	DTR2	R/W	XXXXXXXX_B to XXXXXXXX_B
$001A98_H$ to $001A9F_H$	Data register 3 (8 bytes)	DTR3	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AA0_H$ to $001AA7_H$	Data register 4 (8 bytes)	DTR4	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AA8_H$ to $001AAF_H$	Data register 5 (8 bytes)	DTR5	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AB0_H$ to $001AB7_H$	Data register 6 (8 bytes)	DTR6	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AB8_H$ to $001ABF_H$	Data register 7 (8 bytes)	DTR7	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AC0_H$ to $001AC7_H$	Data register 8 (8 bytes)	DTR8	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AC8_H$ to $001ACF_H$	Data register 9 (8 bytes)	DTR9	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AD0_H$ to $001AD7_H$	Data register 10 (8 bytes)	DTR10	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AD8_H$ to $001ADF_H$	Data register 11 (8 bytes)	DTR11	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AE0_H$ to $001AE7_H$	Data register 12 (8 bytes)	DTR12	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AE8_H$ to $001AEF_H$	Data register 13 (8 bytes)	DTR13	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AF0_H$ to $001AF7_H$	Data register 14 (8 bytes)	DTR14	R/W	XXXXXXXX_B to XXXXXXXX_B
$001AF8_H$ to $001AFF_H$	Data register 15 (8 bytes)	DTR15	R/W	XXXXXXXX_B to XXXXXXXX_B

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage	V_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} = AV_{CC} *1
	AVRH, AVRL	V_{SS} − 0.3	V_{SS} + 6.0	V	AV_{CC} ≥ AVRH/L, AVRH ≥ AVRL *1
	DV_{CC}	V_{SS} − 0.3	V_{SS} + 6.0	V	V_{CC} ≥ DV_{CC}
Input voltage	V_I	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} − 0.3	V_{SS} + 6.0	V	*2
Maximum Clamp Current	I_{CLAMP}	−2.0	2.0	mA	*6
Maximum Total Clamp Current	$\sum\lvert I_{CLAMP}\rvert$	−	20	mA	*6
“L” level Max. output current	I_{OL1}	—	15	mA	Normal output *3
“L” level Avg. output current	I_{OLAV1}	—	4	mA	Normal output, average value *4
“L” level Max. output current	I_{OL2}	—	40	mA	High current output *3
“L” level Avg. output current	I_{OLAV2}	—	30	mA	High current output, average value *4
“L” level Max. overall output current	$\sum I_{OL1}$	—	100	mA	Total normal output
“L” level Max. overall output current	$\sum I_{OL2}$	—	330	mA	Total high current output
“L” level Avg. overall output current	$\sum I_{OLAV1}$	—	50	mA	Total normal output, average value *5
“L” level Avg. overall output current	$\sum I_{OLAV2}$	—	250	mA	Total high current output, average value *5
“H” level Max. output current	I_{OH1}	—	−15	mA	Normal output *3
“H” level Avg. output current	I_{OHAV1}	—	−4	mA	Normal output, average value *4
“H” level Max. output current	I_{OH2}	—	−40	mA	High current output *3
“H” level Avg. output current	I_{OHAV2}	—	−30	mA	High current output, average value *4
“H” level Max. overall output current	$\sum I_{OH1}$	—	−100	mA	Total normal output
“H” level Max. overall output current	$\sum I_{OH2}$	—	−330	mA	Total high current output
“H” level Avg. overall output current	$\sum I_{OHAV1}$	—	−50	mA	Total normal output, average value *5
“H” level Avg. overall output current	$\sum I_{OHAV2}$	—	−250	mA	Total high current output, average value *5
Power consumption	P_D	—	500	mW	MB90F598G
		—	400	mW	MB90598G
Operating temperature	T_A	−40	+85	°C	
Storage temperature	T_{STG}	−55	+150	°C	

*1: AV_{CC}, AVRH, AVRL and DV_{CC} shall not exceed V_{CC}. AVRH and AVRL shall not exceed AV_{CC}. Also, AVRL shall never exceed AVRH.

*2: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

*3: The maximum output current is a peak value for a corresponding pin.

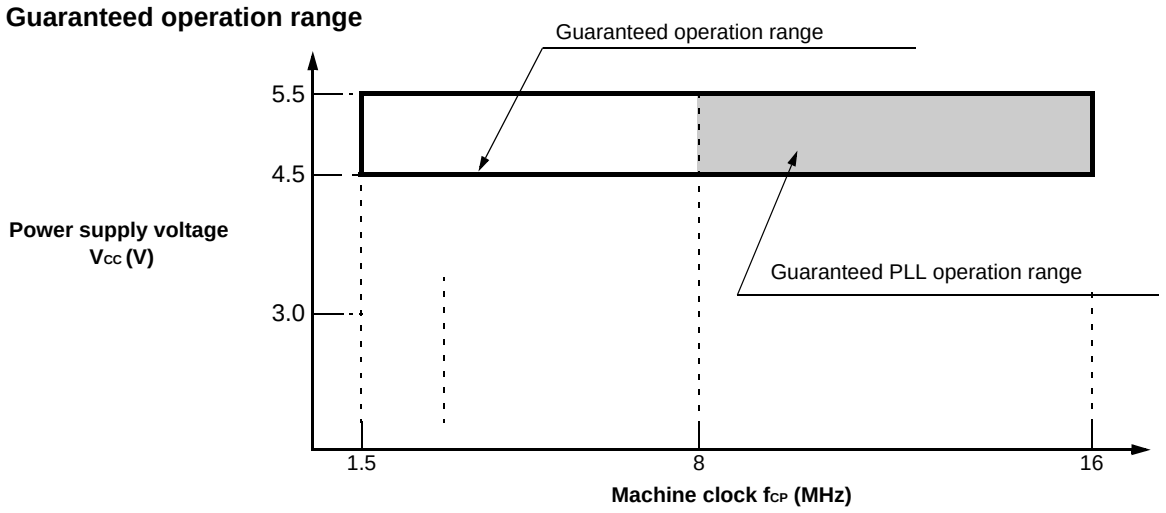
*4: Average output current is an average current value observed for a 100 ms period for a corresponding pin.

*5: Total average current is an average current value observed for a 100 ms period for all corresponding pins.

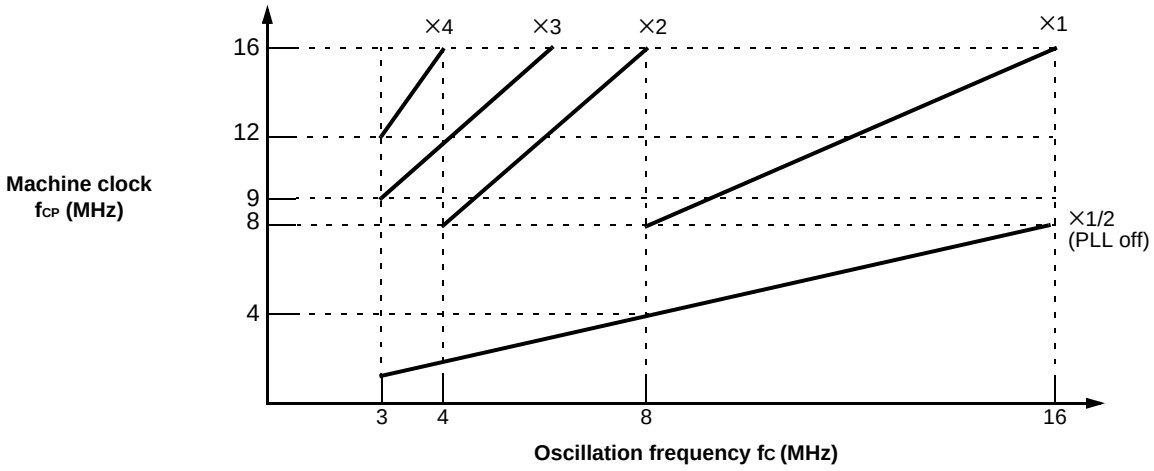
*6:

- Applicable to pins : P00 to P07, P10 to P17, P20 to P27, P30 to P37, P40 to P47, P50 to P57, P70 to P77, P80 to P87, P90 to P95
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied with a limiting resistance placed between the +B signal and the microcontroller.

- **Guaranteed operation range**



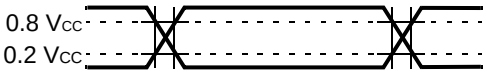
- **Oscillation frequency and machine clock frequency**



AC characteristics are set to the measured reference voltage values below.

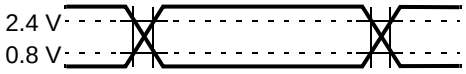
- **Input signal waveform**

Hysteresis Input Pin



- **Output signal waveform**

Output Pin



11.4.3 Power On Reset

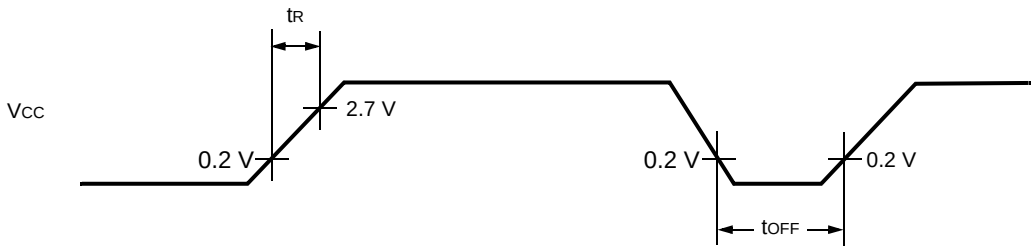
(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Power on rise time	t_R	V_{CC}	—	0.05	30	ms	*
Power off time	t_{OFF}	V_{CC}		50	—	ms	Due to repetitive operation

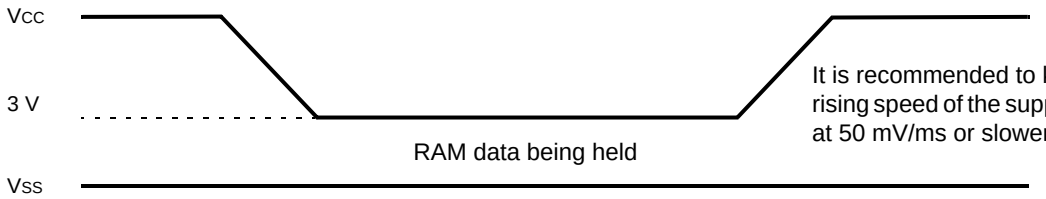
*: V_{CC} must be kept lower than 0.2 V before power-on.

Notes:

- The above values are used for creating a power-on reset.
- Some registers in the device are initialized only upon a power-on reset. To initialize these registers, turn on the power supply using the above values.



Sudden changes in the power supply voltage may cause a power-on reset.
To change the power supply voltage while the device is in operation, it is recommended to raise the voltage smoothly to suppress fluctuations as shown below.
In this case, change the supply voltage with the PLL clock not used. If the voltage drop is 1 V or less per second, however, you can use the PLL clock.



It is recommended to keep the rising speed of the supply voltage at 50 mV/ms or slower.

11.4.4 UART0/1, Serial I/O Timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = −40 °C to +85 °C)

Parameter	Symbol	Pin name	Condition	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0 to SCK2	Internal clock operation output pins are C_L = 80 pF + 1 TTL.	8 t_{CP}	—	ns	
SCK ↓ ⇒ SOT delay time	t_{SLOV}	SCK0 to SCK2, SOT0 to SOT2		–80	80	ns	
Valid SIN ⇒ SCK ↑	t_{IVSH}	SCK0 to SCK2, SIN0 to SIN2		100	—	ns	
SCK ↑ ⇒ Valid SIN hold time	t_{SHIX}	SCK0 to SCK2, SIN0 to SIN2		60	—	ns	

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	—	AVRH	AVRL + 3.0	—	AV_{CC}	V	
	—	AVRL	0	—	AVRH − 3.0	V	
Power supply current	I_A	AV_{CC}	—	5	—	mA	
	I_{AH}	AV_{CC}	—	—	5	μA	*
Reference voltage current	I_R	AVRH	—	400	600	μA	MB90V595G, MB90F598G
			—	140	600	μA	MB90598G
	I_{RH}	AVRH	—	—	5	μA	*
Offset between input channels	—	AN0 to AN7	—	—	4	LSB	

* : When not operating A/D converter, this is the current (V_{CC} = AV_{CC} = AVRH = 5.0 V) when the CPU is stopped.

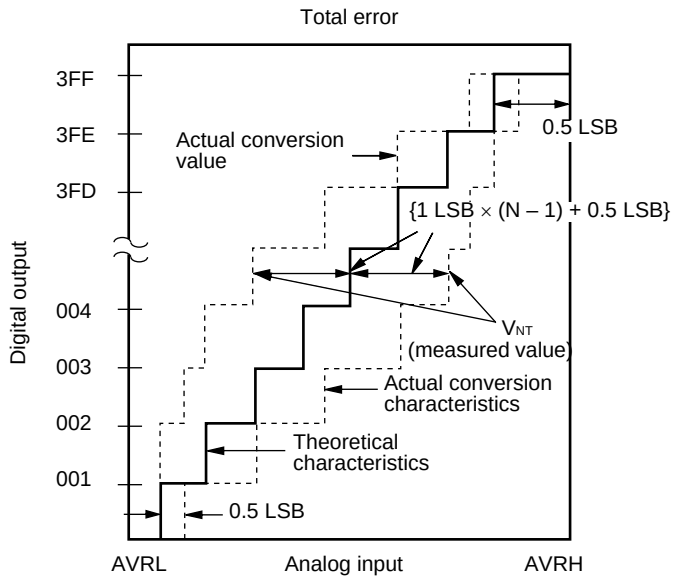
11.6 A/D Converter Glossary

Resolution: Analog changes that are identifiable with the A/D converter

Linearity error:The deviation of the straight line connecting the zero transition point (“00 0000 0000” ↔ “00 0000 0001”) with the full-scale transition point (“11 1111 1110” ↔ “11 1111 1111”) from actual conversion characteristics

Differential linearity error:The deviation of input voltage needed to change the output code by 1 LSB from the theoretical value

Total error:The total error is defined as a difference between the actual value and the theoretical value, which includes zero-transition error/full-scale transition error and linearity error.



$$1\ \text{LSB} = (\text{Theoretical value})\ \frac{\text{AVRH} - \text{AVRL}}{1024}\ [\text{V}]$$

$$\text{Total error for digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (\text{N} - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

V_{OT} (Theoretical value) = AVRL + 0.5 LSB[V]

V_{NT}: Voltage at a transition of digital output from (N – 1) to N

V_{FST} (Theoretical value) = AVRH – 1.5 LSB[V]

(Continued)