Renesas Electronics America Inc - R7FS3A37A3A01CFP#AA0 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	CANbus, EBI/EMI, I²C, MMC/SD, QSPI, SCI, SPI, SSI, UART/USART, USB
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	84
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	8K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.6V ~ 5.5V
Data Converters	A/D 25x14b; D/A 3x8b, 3x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LFQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r7fs3a37a3a01cfp-aa0

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 31, Controller Area Network (CAN) Module in User's Manual.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (only for the host controller) transfer as defined in the Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on the user system. The MCU supports revision 1.2 of the Battery Charging Specification. Because the MCU can be powered at 5 V, the USB LDO regulator provides the internal USB transceiver power supply at 3.3 V. See section 28, USB 2.0 Full-Speed Module (USBFS) in User's Manual.
SD/MMC Host Interface (SDHI)	The Secure Digital Host Interface (SDHI) and MultiMediaCard (MMC) interface provide the functionality needed to connect a variety of external memory cards to the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting different memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and support for high-speed SDR transfer modes. See section 36, SD/MMC Host Interface (SDHI) in User's Manual.

Table 1.9 Analog

Feature	Functional description
14-bit A/D Converter (ADC14)	A 14-bit successive approximation A/D converter is provided. Up to 28 analog input channels are selectable. Temperature sensor output and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit and 14-bit conversion making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 38, 14-Bit A/D Converter (ADC14) in User's Manual.
12-bit D/A Converter (DAC12)	The 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 39, 12-Bit D/A Converter (DAC12) in User's Manual.
8-bit D/A Converter (DAC8) for ACMPLP	The 8-bit D/A Converter (DAC8) converts data and does not include an output amplifier. The DAC8 is used only as the reference voltage for ACMPLP. See section 43, 8-Bit D/A Converter (DAC8) in User's Manual.
Temperature Sensor (TSN)	The on-chip temperature sensor determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC14 for conversion and can be further used by the end application. See section 40, Temperature Sensor (TSN) in User's Manual.
Low-Power Analog Comparator (ACMPLP)	The Low-Power Analog Comparator (ACMPLP) compares a reference input voltage and analog input voltage. The comparison result can be read by software and also be output externally. The reference voltage can be selected from an input to the CMPREFi(i = 0,1) pin, an internal 8-bit D/A converter output, or the internal reference voltage (Vref) generated internally in the MCU. The ACMPLP response speed can be set before starting an operation. Setting the high-speed mode decreases the response delay time, but increases current consumption. Setting the low-speed mode increases the response delay time, but decreases current consumption. See section 42, Low Power Analog Comparator (ACMPLP) in User's Manual.
Operational Amplifier (OPAMP)	The Operational Amplifier (OPAMP) can be used to amplify small analog input voltages and output the amplified voltages. A total of four differential operational amplifier units with two input pins and one output pin are provided. See section 41, Operational Amplifier (OPAMP) in User's Manual.

1.4 Function Comparison

Table 1.14 Function comparison

Part numbers		R7FS3A37A2A01CLK	R7FS3A37A3A01CFB	R7FS3A37A2A01CBJ	R7FS3A37A3A01CFP	R7FS3A37A2A01CLJ	R7FS3A37A3A01CFM R7FS3A37A3A01CNB
Pin count		145	144	121	100	100	64
Package		LGA	LQFP	BGA	LQFP	LGA	LQFP/QFN
Code flash memory		512 KB					
Data flash memory		8 KB					
SRAM		96 KB					
	Parity	80 KB					
	ECC	16 KB					
System	CPU clock	48 MHz					
	Backup registers	512 bytes					
	ICU	Yes					
	KINT	8					
Event control	ELC	Yes					
DMA	DTC	Yes					
	DMAC	4					
BUS	External bus	16-bit bus		8-bit bus			No
Timers	GPT32	4					
	GPT16	6					
	AGT	2					
	RTC	Yes					
	WDT/IWDT	Yes					
Communication	SCI	6					
	IIC	3			2		
	SPI	2					
	SSIE	1					No
	QSPI	1					No
	SDHI	1					No
	CAN	1					
	USBFS	Yes					
Analog	ADC14	28		26	25		18
	DAC12	1					
	DAC8	2					
	ACMPLP	2					
	OPAMP	4	4	4	4	4	3
	TSN	Yes					
HMI	SLCDC	4 com × 54 seg or 8 com x 50 seg		4 com × 46 seg or 8 com x 42 seg	4 com x 38 seg or 8 com x 34 seg		4 com × 21 seg or 8 com x 17 seg
	CTSU	27					24
Data processing	CRC	Yes					
	DOC	Yes					
Security		SCE5					

1.7 Pin Lists

Pin number											Timers				Communication interfaces						Analogs			HMI	
LGA145	LQFP144	BGA121	LQFP100	LGA100	LQFP64	QFN64	Power, System, Clock, Debug, CAC, VBATT	Interrupt	I/O ports	External bus	AGT	GPT_OPS, POEG	GPT	RTC	USBFS,CAN	SCI	IIC	SPI/QSPI	SSIE	SDHI	ADC14	DAC12, OPAMP	ACMPLP	SLCDC	CTSU
N13	1	L11	1	J10	1	1	CACREF	IRQ0	P400		AGTIO1		GTIOC6A			SCK1 SCK4	SCL0		AUDIO_CLK					SEG4	TS20
L11	2	K11	2	J9	2	2		IRQ5	P401			GTETRGA	GTIOC6B		CTX0	TXD1/MOSI1/SDA1 CTS4_RTS4/SS4	SDA0							SEG5	TS19
M13	3	J10	3	F6	3	3	VBATWIO0	IRQ4	P402		AGTIO0/AGTIO1			RTCIC0	CRX0	RXD1/MISO1/SCL1								SEG6	TS18
K11	4	J11	4	H10			VBATWIO1		P403		AGTIO0/AGTIO1		GTIOC3A	RTCIC1		CTS1_RTS1/SS1			SSIBCK0						TS17
L12	5	H9	5	G8			VBATWIO2		P404				GTIOC3B	RTCIC2					SSILRCK0/SSIFS0						
L13	6	H10	6	H9					P405				GTIOC1A						SSITXD0						
J10	7	H11	7	F7					P406				GTIOC1B					SSLA3	SSIRXD0						
H10	8	G6							P700				GTIOC5A					MISOA							
K12	9	G7							P701				GTIOC5B					MOSIA							
K13	10	G8							P702				GTIOC6A					RSPCKA							
J11	11								P703				GTIOC6B					SSLA0					VCOUT		
H11	12								P704		AGTO0							SSLA1							
G11	13								P705		AGTIO0							SSLA2							
J12	14	G10	8	G9	4	4	VBATT																		
J13	15	G11	9	G10	5	5	VCL																		
H13	16	F11	10	F10	6	6	XCIN		P215																
H12	17	F10	11	F9	7	7	XCOUT		P214																
F12	18	G9	12	D9	8	8	VSS																		
G12	19	E10	13	E9	9	9	XTAL	IRQ2	P213			GTETRGA	GTIOC0A			TXD1/MOSI1/SDA1									
G13	20	E11	14	E10	10	10	EXTAL	IRQ3	P212		AGTEE1	GTETRGB	GTIOC0B			RXD1/MISO1/SCL1									
F13	21	F9	15	D10	11	11	VCC																		
G10	22								P713		AGTOA0		GTIOC2A												
F11	23								P712		AGTOB0		GTIOC2B												
E13	24								P711		AGTEE0					CTS1_RTS1/SS1									
E12	25	F8							P710	A17						SCK1									
F10	26	F7						IRQ10	P709							TXD1/MOSI1/SDA1									
D13	27	E9	16	F8				IRQ11	P708							RXD1/MISO1/SCL1		SSLA3							
E11	28	D10	17	E8				IRQ8	P415				GTIOC0A					SSLA2		SD0CD						
D12	29	D11	18	E7				IRQ9	P414				GTIOC0B					SSLA1		SD0WP						
E10	30	E8	19	C9					P413			GTOUP				CTS0_RTS0/SS0		SSLA0		SD0CLK					
C13	31	D9	20	C10					P412			GTOULO				SCK0		RSPCKA		SD0CMD					

2.2.7 P408, P409 I/O Pin Output Characteristics of Middle Drive Capacity

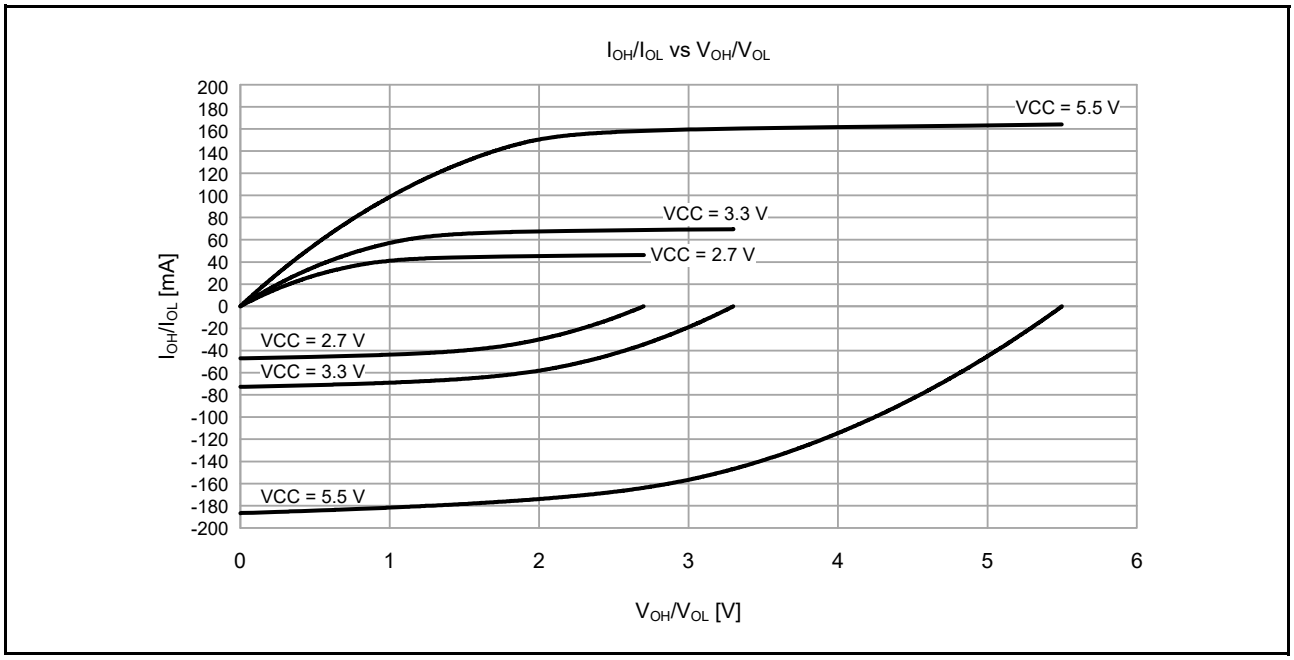


Figure 2.12 **V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C when middle drive output is selected (reference data)**

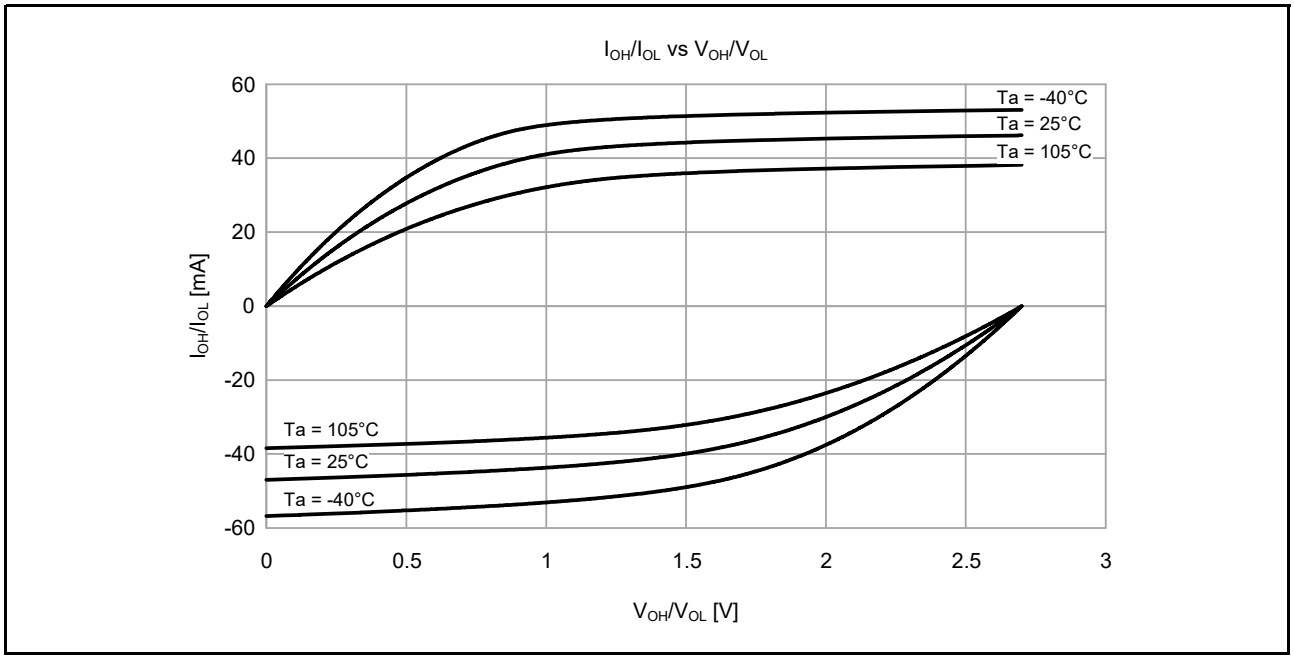


Figure 2.13 **V_{OH}/V_{OL} and I_{OH}/I_{OL} temperature characteristics at VCC = 2.7 V when middle drive output is selected (reference data)**

2.2.8 IIC I/O Pin Output Characteristics

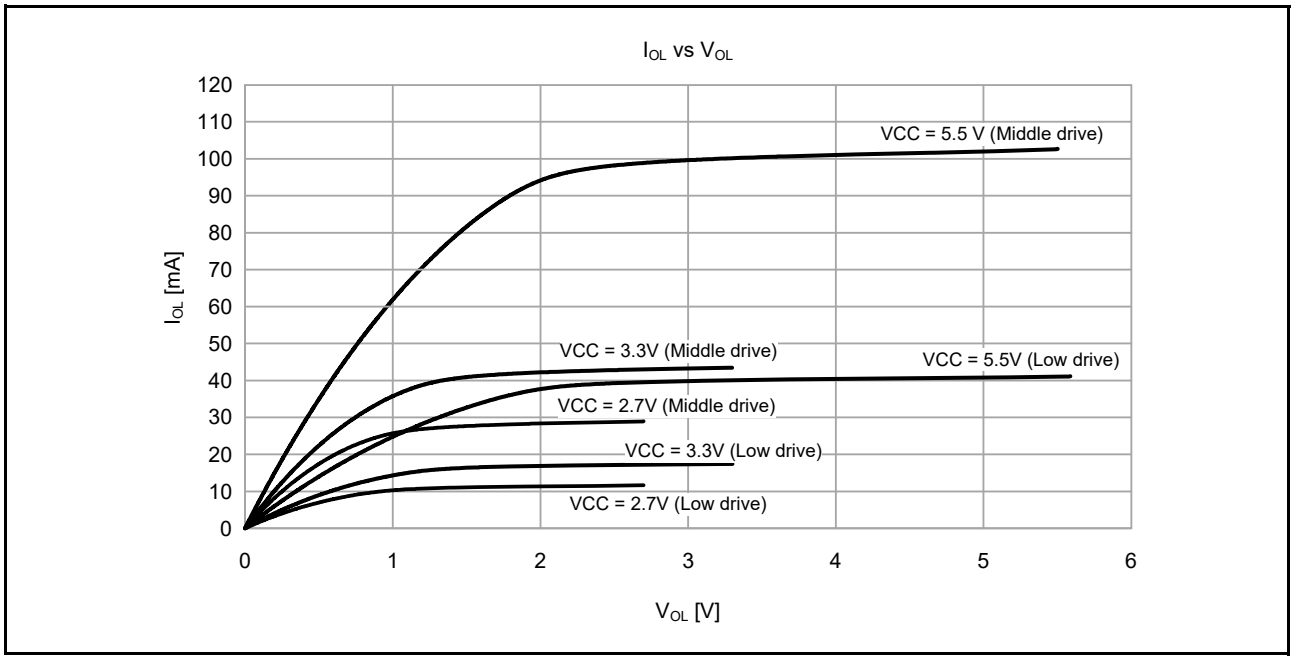


Figure 2.16 V_{OH}/V_{OL} and I_{OH}/I_{OL} voltage characteristics at Ta = 25°C

2.3 AC Characteristics

2.3.1 Frequency

Table 2.17 Operation frequency value in high-speed operating mode

Conditions: VCC = AVCC0 = 2.4 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	2.7 to 5.5 V	f	0.032768	-	48	MHz
		2.4 to 2.7 V		0.032768	-	16	
	FlashIF clock (FCLK)*1, *2, *4	2.7 to 5.5 V		0.032768	-	32	
		2.4 to 2.7 V		0.032768	-	16	
	Peripheral module clock (PCLKA)*4	2.7 to 5.5 V		-	-	48	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKB)*4	2.7 to 5.5 V		-	-	32	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKC)*3, *4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	Peripheral module clock (PCLKD)*4	2.7 to 5.5 V		-	-	64	
		2.4 to 2.7 V		-	-	16	
	External bus clock (BCLK)*4	2.7 to 5.5 V		-	-	24	
		2.4 to 2.7 V		-	-	16	
	EBCLK pin output	2.7 to 5.5 V		-	-	12	
		2.4 to 2.7 V		-	-	8	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.

Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.

Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.

Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

Note 5. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see Table 2.22, Clock timing.

Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.
Note 4. The maximum value of operation frequency does not include the internal oscillator errors. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see Table 2.22, Clock timing.

Table 2.20 Operation frequency value in low-voltage mode
Conditions: VCC = AVCC0 = 1.6 to 5.5 V

Parameter			Symbol	Min	Typ	Max*5	Unit
Operation frequency	System clock (ICLK)*4	1.6 to 5.5 V	f	0.032768	-	4	MHz
	FlashIF clock (FCLK)*1, *2, *4	1.6 to 5.5 V		0.032768	-	4	
	Peripheral module clock (PCLKA)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKB)*4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKC)*3, *4	1.6 to 5.5 V		-	-	4	
	Peripheral module clock (PCLKD)*4	1.6 to 5.5 V		-	-	4	
	External bus clock (BCLK)*4	1.6 to 5.5 V		-	-	4	
	EBCLK pin output	1.8 to 5.5 V		-	-	4	
		1.6 to 1.8 V		-	-	2	

Note 1. The lower-limit frequency of FCLK is 1 MHz while programming or erasing the flash memory. When using FCLK for programming or erasing the flash memory at below 4 MHz, the frequency can be set to 1 MHz, 2 MHz, or 3 MHz. A non-integer frequency such as 1.5 MHz cannot be set.
Note 2. The frequency accuracy of FCLK must be ±3.5% while programming or erasing the flash memory. Confirm the frequency accuracy of the clock source.
Note 3. The lower-limit frequency of PCLKC is 4 MHz at 2.4 V or above and 1 MHz at below 2.4 V when the 14-bit A/D converter is in use.
Note 4. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.
Note 5. The maximum value of operation frequency does not include errors of the internal oscillator. The operation can be guaranteed with the errors of the internal oscillator. For details on the range for guaranteed operation, see Table 2.22, Clock timing.

Table 2.21 Operation frequency value in Subosc-speed mode
Conditions: VCC = AVCC0 = 1.8 to 5.5 V

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*3	1.8 to 5.5 V	f	27.8528	32.768	37.6832	kHz
	FlashIF clock (FCLK)*1, *3	1.8 to 5.5 V		27.8528	32.768	37.6832	
	Peripheral module clock (PCLKA)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKB)*3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKC)*2, *3	1.8 to 5.5 V		-	-	37.6832	
	Peripheral module clock (PCLKD)*3	1.8 to 5.5 V		-	-	37.6832	
	External bus clock (BCLK)*3	1.8 to 5.5 V		-	-	37.6832	
	EBCLK pin output	1.8 to 5.5 V		-	-	37.6832	

Note 1. Programming and erasing the flash memory is not possible.
Note 2. The 14-bit A/D converter cannot be used.
Note 3. See section 9, Clock Generation Circuit in User's Manual for the relationship of frequencies between ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK.

2.3.2 Clock Timing

Table 2.22 Clock timing (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	VCC = 2.7 V or above	t_{Bcyc}	83.3	-	-	ns	Figure 2.26
	VCC = 1.8 V or above		125	-	-		
	VCC = 1.6 V or above		500	-	-		
EBCLK pin output high pulse width	VCC = 2.7 V or above	t_{CH}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output low pulse width	VCC = 2.7 V or above	t_{CL}	20	-	-	ns	
	VCC = 1.8 V or above		30	-	-		
	VCC = 1.6 V or above		150	-	-		
EBCLK pin output rise time	VCC = 2.7 V or above	t_{Cr}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EBCLK pin output fall time	VCC = 2.7 V or above	t_{Cf}	-	-	15	ns	
	VCC = 2.4 V or above		-	-	25		
	VCC = 1.8 V or above		-	-	30		
	VCC = 1.6 V or above		-	-	50		
EXTAL external clock input cycle time		t_{Xcyc}	50	-	-	ns	Figure 2.27
EXTAL external clock input high pulse width		t_{XH}	20	-	-	ns	
EXTAL external clock input low pulse width		t_{XL}	20	-	-	ns	
EXTAL external clock rising time		t_{Xr}	-	-	5	ns	
EXTAL external clock falling time		t_{Xf}	-	-	5	ns	
EXTAL external clock input wait time*1		t_{EXWT}	0.3	-	-	μs	-
EXTAL external clock input frequency		f_{EXTAL}	-	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			-	-	8		1.8 ≤ VCC < 2.4
			-	-	1		1.6 ≤ VCC < 1.8
Main clock oscillator oscillation frequency		f_{MAIN}	1	-	20	MHz	2.4 ≤ VCC ≤ 5.5
			1	-	8		1.8 ≤ VCC < 2.4
			1	-	4		1.6 ≤ VCC < 1.8
Main clock oscillation stabilization wait time (crystal)*9		$t_{MAINOSCWT}$	-	-	-*9	ms	
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization time		t_{LOCO}	-	-	100	μs	Figure 2.28
IWDT-dedicated clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		f_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization time		t_{MOCO}	-	-	1	μs	-

2.3.3 Reset Timing

Table 2.23 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	At power-on	t_{RESWP}	3	-	-	ms	Figure 2.34
	Other than above	t_{RESW}	30	-	-	μs	Figure 2.35
Wait time after RES cancellation (at power-on)	LVD0: enable*1	t_{RESWT}	-	0.7	-	ms	Figure 2.34
	LVD0: disable*2		-	0.3	-		
Wait time after RES cancellation (during powered-on state)	LVD0: enable*1	t_{RESWT2}	-	0.5	-	ms	Figure 2.35
	LVD0: disable*2		-	0.05	-		
Internal reset cancellation time (Watchdog timer reset, SRAM parity error reset, SRAM ECC error reset, Bus master MPU error reset, Bus slave MPU error reset, Stack pointer error reset, Software reset)	LVD0: enable*1	t_{RESWT3}	-	0.6	-	ms	
	LVD0: disable*2		-	0.15	-		

Note 1. When OFS1.LVDAS = 0.
Note 2. When OFS1.LVDAS = 1.

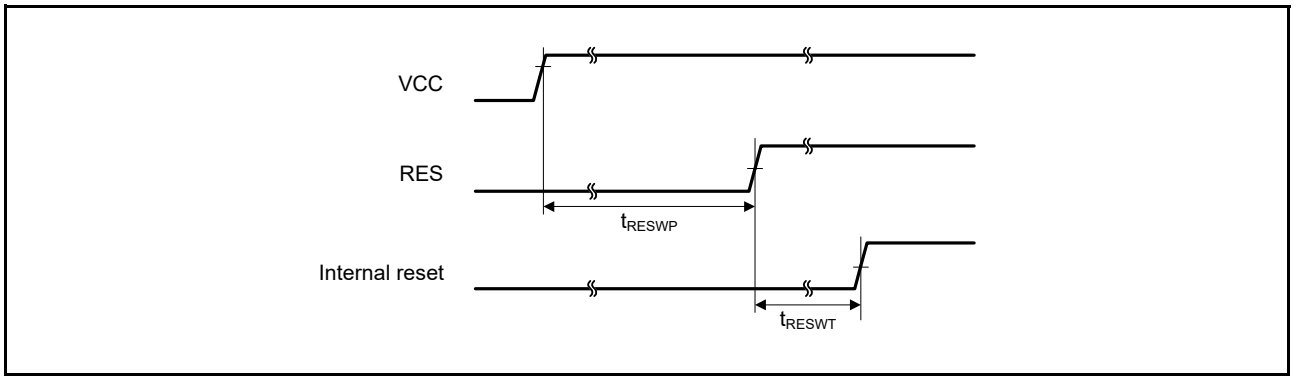


Figure 2.34 Reset input timing at power-on

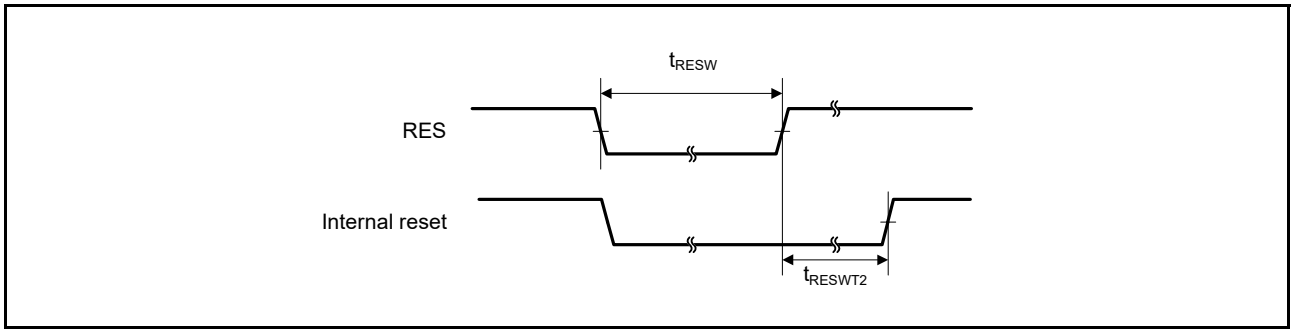


Figure 2.35 Reset input timing (1)

2.3.5 NMI and IRQ Noise Filter

Table 2.30 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note 1. t_{Pcyc} indicates the cycle of PCLKB.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock (i = 0 to 15).

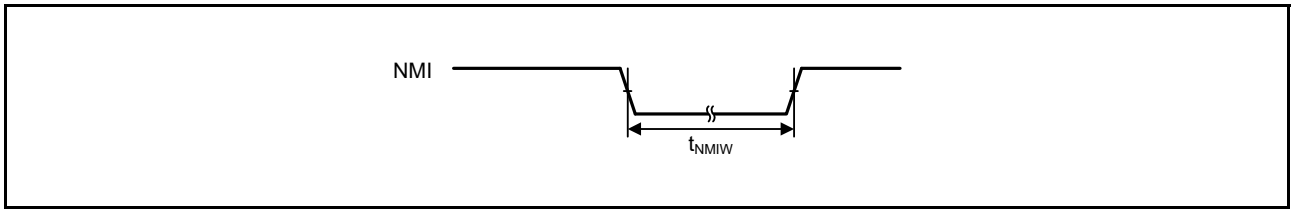


Figure 2.38 NMI interrupt input timing

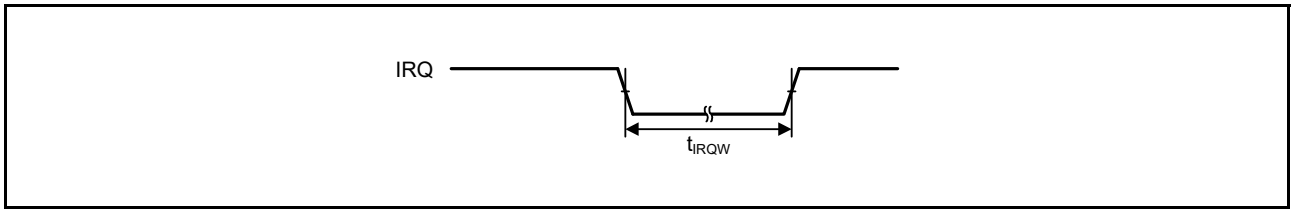


Figure 2.39 IRQ interrupt input timing

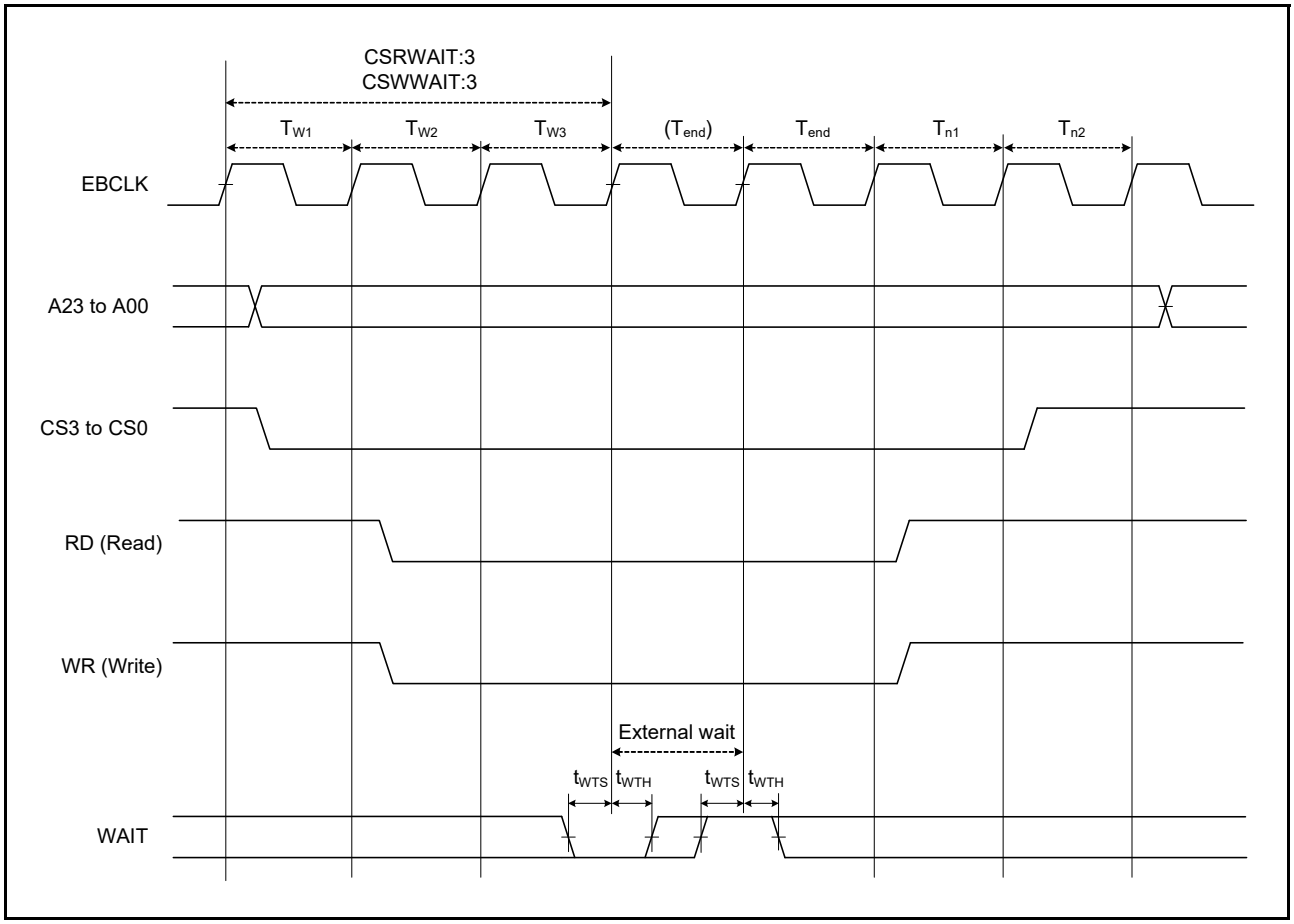


Figure 2.46 External bus timing/external wait control

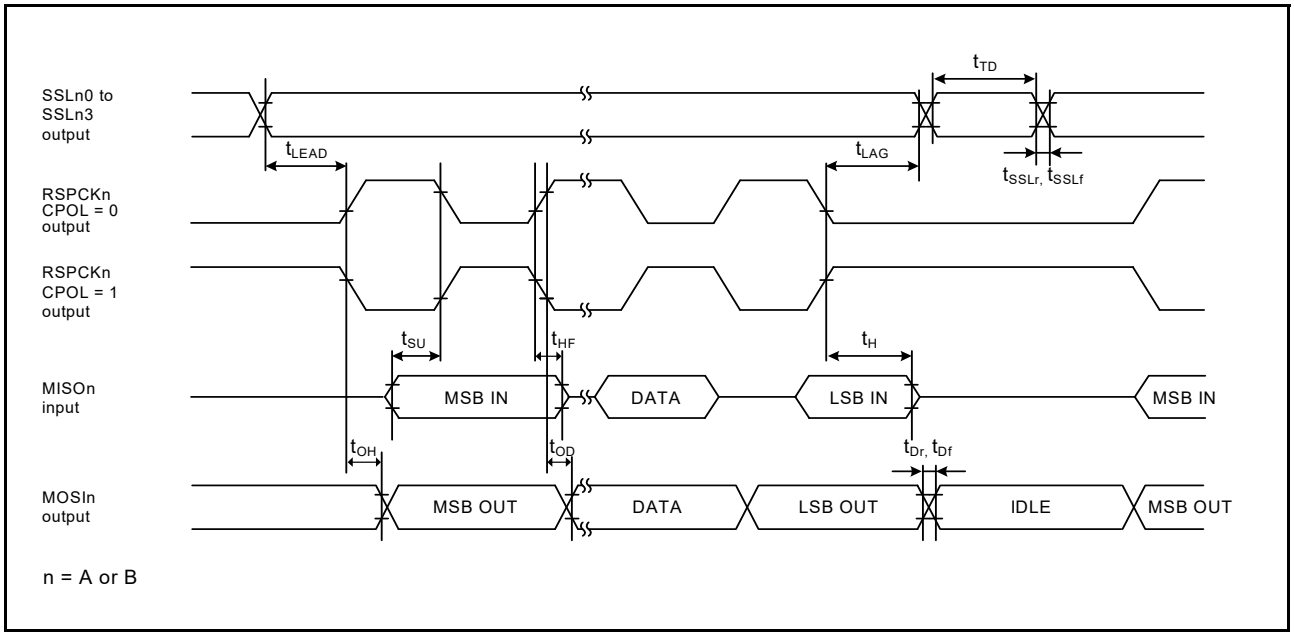


Figure 2.65 SPI timing (master, CPHA = 1) (bit rate: PCLKA division ratio is set to 1/2)

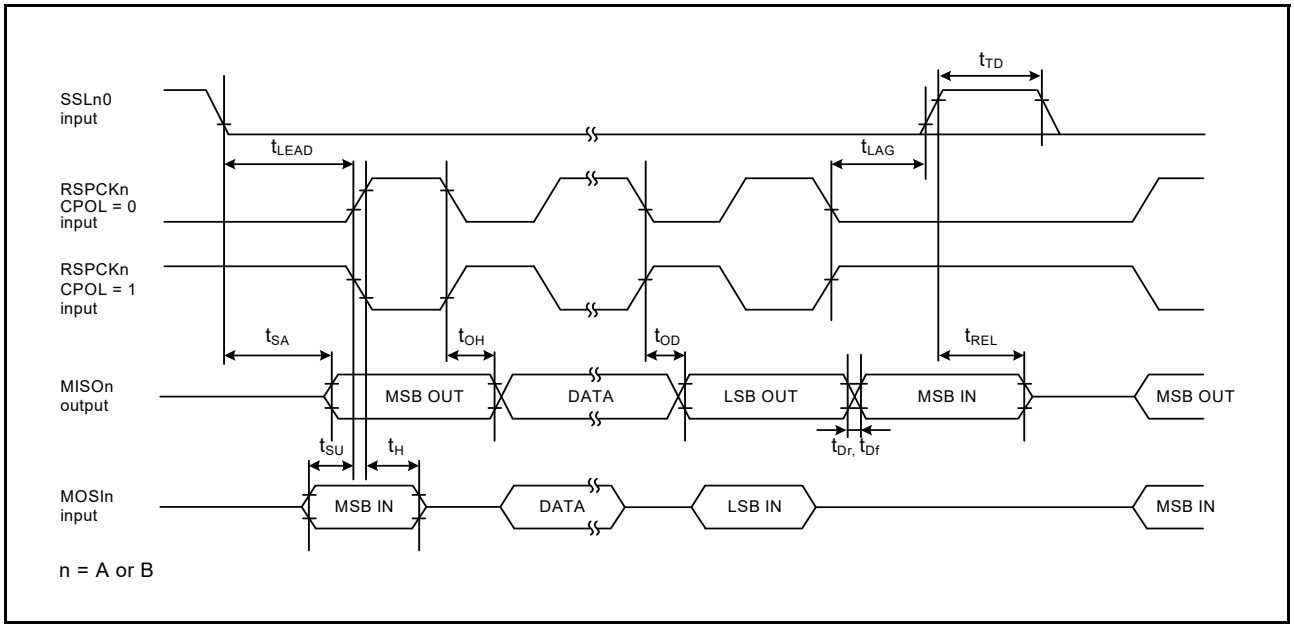


Figure 2.66 SPI timing (slave, CPHA = 0)

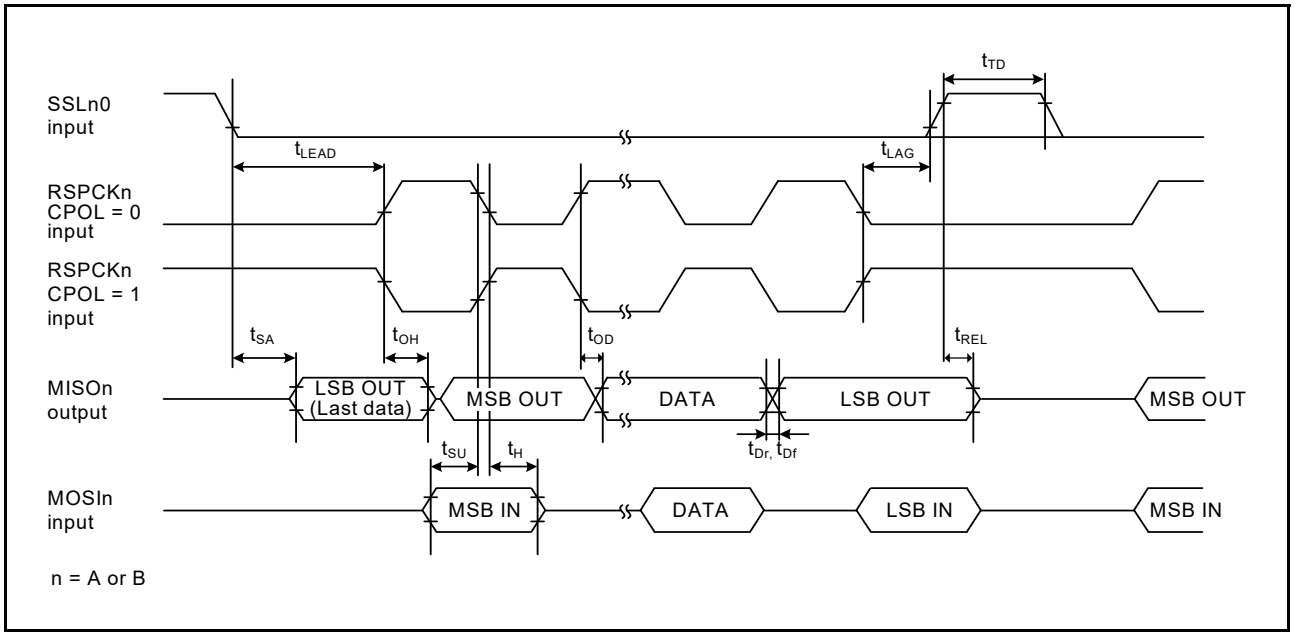


Figure 2.67 SPI timing (slave, CPHA = 1)

2.3.11 QSPI Timing

Table 2.41 QSPI timing

Conditions: VCC = 1.8 to 5.5 V

Conditions: Middle drive output is selected in the Port Drive Capability bit in PmnPFS register

Parameter			Symbol	Min	Max	Unit*1	Test conditions
QSPI	QSPCLK clock cycle		t_{QScyc}	2*4	48	t_{Pcyc}	Figure 2.68
	QSPCLK clock high-level pulse width		t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCLK clock low-level pulse width		t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	Data input setup time		t_{SU}	25	-	ns	Figure 2.69
	Data input hold time		t_{IH}	2	-	ns	
	SSL setup time		t_{LEAD}	(N + 0.5) × t_{Qscyc} - 15*2	(N + 0.5) × t_{Qscyc} + 100*2	ns	
	SSL hold time		t_{LAG}	(N + 0.5) × t_{Qscyc} - 15*3	(N + 0.5) × t_{Qscyc} + 100*3	ns	
	Data output delay	2.7 V or above	t_{OD}	-	14	ns	
		2.4 V or above		-	20		
		1.8 V or above		-	30		
	Data output hold time	2.7 V or above	t_{OH}	–3.3	-	ns	
		1.8 V or above		–10	-		
	Successive transmission delay		t_{TD}	1	16	t_{Qscyc}	

Note 1. t_{Pcyc}: PCLKA cycle.

Note 2. N is set to 0 or 1 in SFMSLD.

Note 3. N is set to 0 or 1 in SFMSHD.

Note 4. The upper limit of QSPCLK is 16MHz.

2.3.13 SSIE Timing

Table 2.43 SSIE timing
Conditions: VCC = 1.6 to 5.5 V

Parameter			Symbol	Min	Max	Unit	Test conditions
SSIE	AUDIO_CLK input frequency	2.7 V or above	t_{AUDIO}	-	25	MHz	-
		1.6 V or above		-	4		
	Output clock period		t_O	250	-	ns	Figure 2.71
	Input clock period		t_I	250	-	ns	
	Clock high pulse width	1.8 V or above	t_{HC}	100	-	ns	
		1.6 V or above		200	-		
	Clock low pulse width	1.8 V or above	t_{LC}	100	-	ns	
		1.6 V or above		200	-		
	Clock rise time		t_{RC}	-	25	ns	
	Data delay	2.7 V or above	t_{DTR}	-	65	ns	Figure 2.72, Figure 2.73
		1.8 V or above		-	105		
		1.6 V or above		-	140		
	Set-up time	2.7 V or above	t_{SR}	65	-	ns	
		1.8 V or above		90	-		
		1.6 V or above		140	-		
	Hold time		t_{HTR}	40	-	ns	
	SSITXD0 output delay from SSILRCK/SSIFS change time	1.8 V or above	T_{DTRW}	-	105	ns	Figure 2.74
		1.6 V or above		-	140		

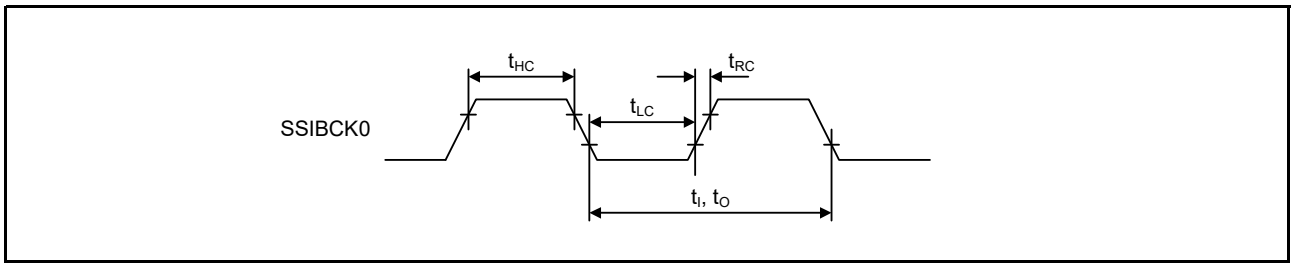


Figure 2.71 SSIE clock input/output timing

2.5 ADC14 Characteristics

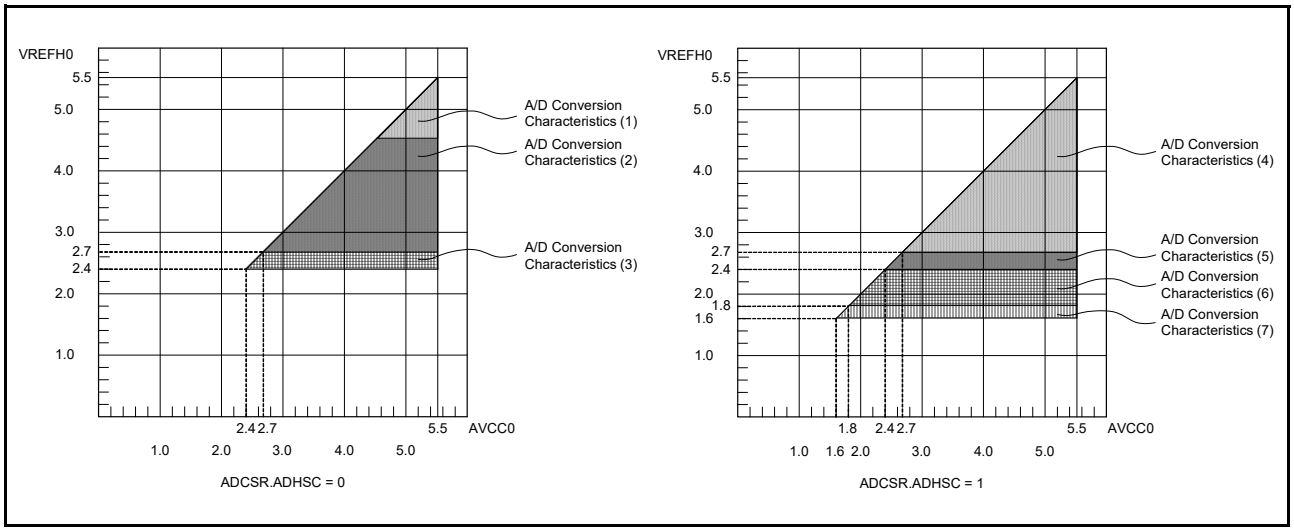


Figure 2.80 AVCC0 to VREFH0 voltage range

Table 2.48 A/D conversion characteristics (1) in high-speed A/D conversion mode (1 of 2)
Conditions: VCC = AVCC0 = 4.5 to 5.5 V, VREFH0 = 4.5 to 5.5 V
Reference voltage range applied to the VREFH0 and VREFL0.

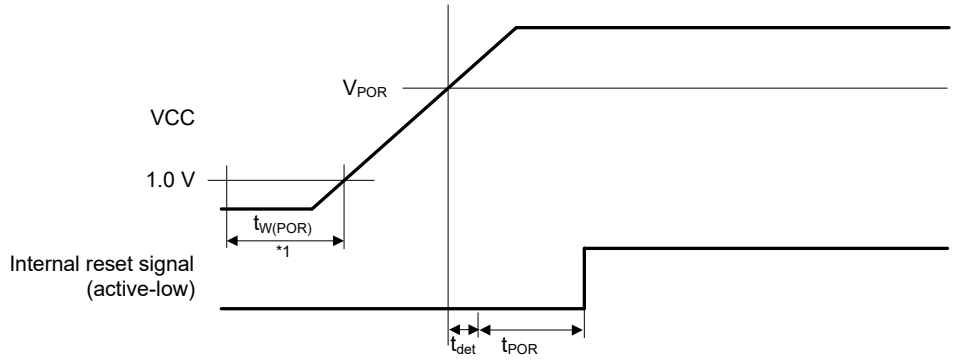
Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	64	MHz	-
Analog input capacitance*2		Cs	-	-	8 (reference data)	pF	High-precision channel
			-	-	9 (reference data)	pF	Normal-precision channel
Analog input resistance		Rs	-	-	2.5 (reference data)	kΩ	High-precision channel
			-	-	6.7 (reference data)	kΩ	Normal-precision channel
Analog input voltage range		Ain	0	-	VREFH0	V	-
12-bit mode							
Resolution			-	-	12	Bit	-
Conversion time*1 (Operation at PCLKC = 64 MHz)	Permissible signal source impedance Max. = 0.3 kΩ		0.70	-	-	µs	High-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 0Dh
			1.13	-	-	µs	Normal-precision channel ADCSR.ADHSC = 0 ADSSTRn.SST[7:0] = 28h
Offset error			-	±0.5	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above
Full-scale error			-	±0.75	±4.5	LSB	High-precision channel
					±6.0	LSB	Other than above
Quantization error			-	±0.5	-	LSB	-
Absolute accuracy			-	±1.25	±5.0	LSB	High-precision channel
					±8.0	LSB	Other than above
DNL differential nonlinearity error			-	±1.0	-	LSB	-
INL integral nonlinearity error			-	±1.0	±3.0	LSB	-
14-bit mode							
Resolution			-	-	14	Bit	-

2.9 POR and LVD Characteristics

Table 2.62 Power-on reset circuit and voltage detection circuit characteristics (1)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level*1	Power-on reset (POR)	V_{POR}	1.27	1.42	1.57	V	Figure 2.85, Figure 2.86
	Voltage detection circuit (LVD0)*2	V_{det0_0}	3.68	3.85	4.00	V	Figure 2.87 At falling edge VCC
		V_{det0_1}	2.68	2.85	2.96		
		V_{det0_2}	2.38	2.53	2.64		
		V_{det0_3}	1.78	1.90	2.02		
		V_{det0_4}	1.60	1.69	1.82		
	Voltage detection circuit (LVD1)*3	V_{det1_0}	4.13	4.29	4.45	V	Figure 2.88 At falling edge VCC
		V_{det1_1}	3.98	4.16	4.30		
		V_{det1_2}	3.86	4.03	4.18		
		V_{det1_3}	3.68	3.86	4.00		
		V_{det1_4}	2.98	3.10	3.22		
		V_{det1_5}	2.89	3.00	3.11		
		V_{det1_6}	2.79	2.90	3.01		
		V_{det1_7}	2.68	2.79	2.90		
		V_{det1_8}	2.58	2.68	2.78		
		V_{det1_9}	2.48	2.58	2.68		
		V_{det1_A}	2.38	2.48	2.58		
		V_{det1_B}	2.10	2.20	2.30		
		V_{det1_C}	1.84	1.96	2.05		
		V_{det1_D}	1.74	1.86	1.95		
		V_{det1_E}	1.63	1.75	1.84		
		V_{det1_F}	1.60	1.65	1.73		
	Voltage detection circuit (LVD2)*4	V_{det2_0}	4.11	4.31	4.48	V	Figure 2.89 At falling edge VCC
		V_{det2_1}	3.97	4.17	4.34		
		V_{det2_2}	3.83	4.03	4.20		
		V_{det2_3}	3.64	3.84	4.01		

Note 1. These characteristics apply when noise is not superimposed on the power supply. When a setting causes this voltage detection level to overlap with that of the voltage detection circuit, it cannot be specified whether LVD1 or LVD2 is used for voltage detection.
Note 2. # in the symbol Vdet0_# denotes the value of the OFS1.VDSEL1[2:0] bits.
Note 3. # in the symbol Vdet1_# denotes the value of the LVDLVLR.LVD1LVL[4:0] bits.
Note 4. # in the symbol Vdet2_# denotes the value of the LVDLVLR.LVD2LVL[2:0] bits.



Note: $t_{W(POR)}$ is the time required for a power-on reset to be enabled while the external power VCC is being held below the valid voltage (1.0 V).
When VCC turns on, maintain $t_{W(POR)}$ for 1.0 ms or more.

Figure 2.86 Power-on reset timing

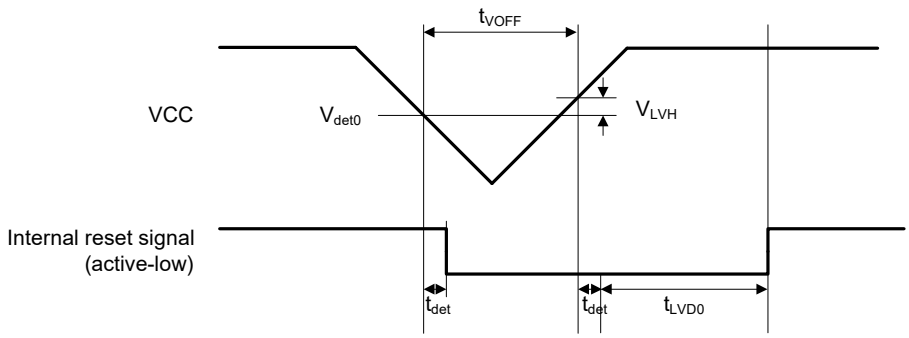


Figure 2.87 Voltage detection circuit timing (V_{det0})

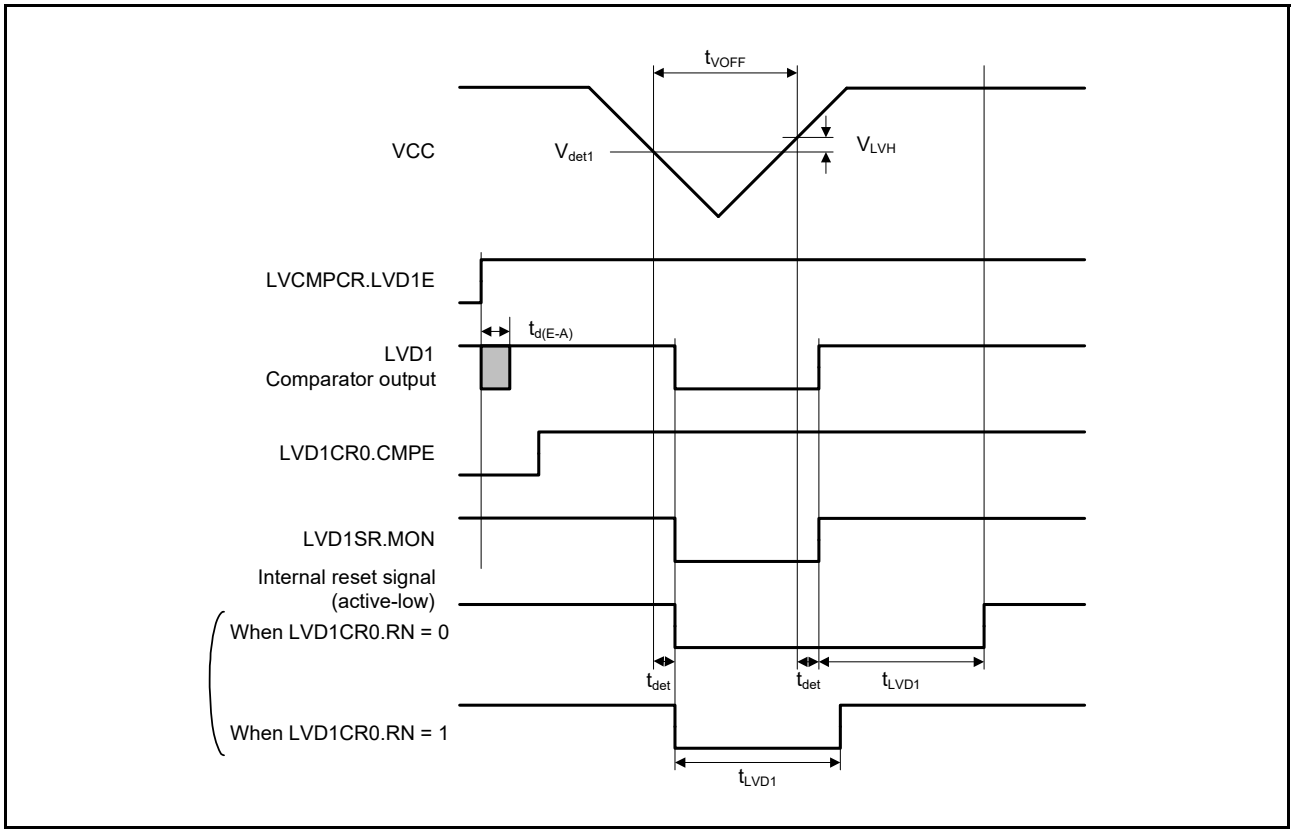


Figure 2.88 Voltage detection circuit timing (V_{det1})

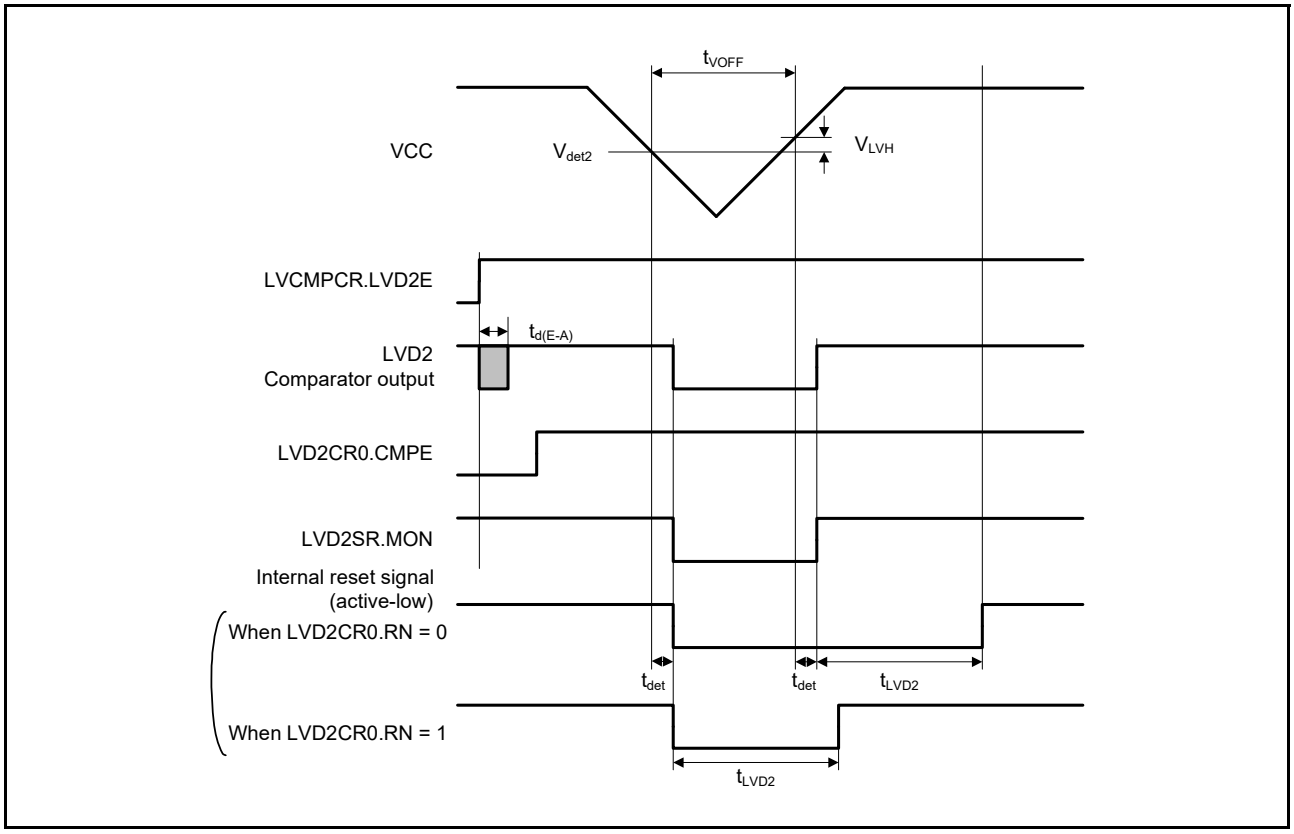


Figure 2.89 Voltage detection circuit timing (V_{det2})

2.12.3 Capacitor Split Method

[1/3 Bias Method]

Table 2.72 Internal voltage boosting method LCD characteristics
Conditions: VCC = 2.2 V to 5.5 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	Test conditions
VL4 voltage*1	V_{L4}	C1 to C4 = 0.47 µF*2	-	VCC	-	V	-
VL2 voltage*1	V_{L2}	C1 to C4 = 0.47 µF*2	2/3 × V_{L4} - 0.07	2/3 × V_{L4}	2/3 × V_{L4} + 0.07	V	-
VL1 voltage*1	V_{L1}	C1 to C4 = 0.47 µF*2	1/3 × V_{L4} - 0.08	1/3 × V_{L4}	1/3 × V_{L4} + 0.08	V	-
Capacitor split wait time*1	t_{WAIT}		100	-	-	ms	Figure 2.93

Note 1. This is the wait time from when voltage bucking is started (VLCON = 1) until display is enabled (LCDON = 1).
Note 2. This is a capacitor that is connected between voltage pins used to drive the LCD.
C1: A capacitor connected between CAPH and CAPL
C2: A capacitor connected between VL1 and GND
C3: A capacitor connected between VL2 and GND
C4: A capacitor connected between VL4 and GND
C1 = C2 = C3 = C4 = 0.47 µF ± 30%.

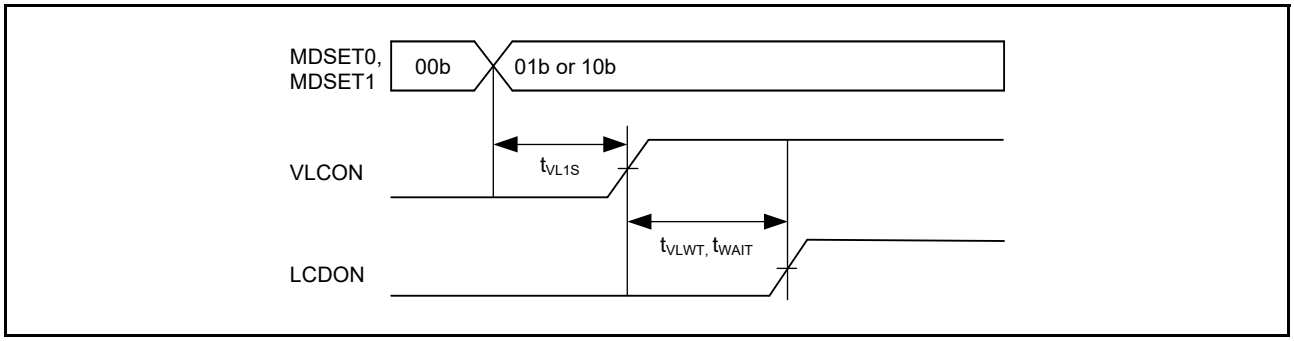


Figure 2.93 LCD reference voltage setup time, voltage boosting wait time, and capacitor split wait time

2.13 Comparator Characteristics

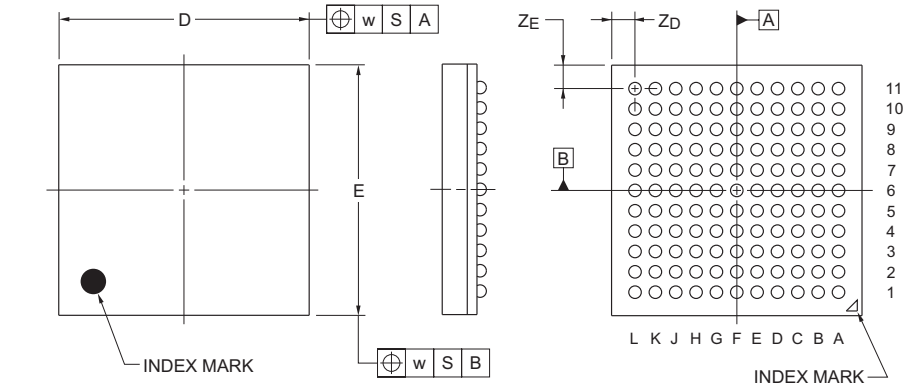
Table 2.73 ACMPLP characteristics
Conditions: VCC = 1.8 to 5.5 V

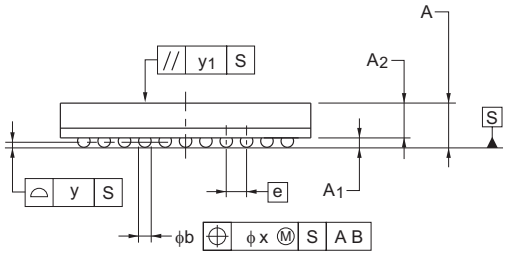
Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	Standard mode	IVREFn (n=0,1)	VREF	0	-	VCC–1.4	V	-
	Window mode*2	IVREF1	VREFH	1.4	-	VCC	V	-
		IVREF0	VREFL	0	-	VCC–1.4	V	-
Input voltage range			VI	0	-	VCC	V	-
Internal reference voltage			-	1.36	1.44	1.50	V	-
Output delay	High-speed mode		Td	-	-	1.2	µs	VCC = 3.0 Slew rate of input signal > 50 mV/µs
	Low-speed mode			-	-	5	µs	
	Window mode			-	-	2	µs	
Offset voltage*1	High-speed mode		-	-	-	50	mV	-
	Low-speed mode		-	-	-	40	mV	-
	Window mode		-	-	-	60	mV	-
Operation stabilization wait time			T_{cmp}	100	-	-	µs	-

Note 1. When 8-bit DAC output is used as the reference voltage, the offset voltage increases up to 2.5 x VCC/256.
Note 2. In window mode, be sure to satisfy the following condition: IVREF1 - IVREF0 ≥ 0.2 V.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFBGA121-8x8-0.65	PLBG0121JA-A	—	0.15

Unit: mm





Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	7.90	8.00	8.10
E	7.90	8.00	8.10
w	—	0.20	—
A	1.11	1.21	1.31
A_1	0.25	0.30	0.35
A_2	—	0.91	—
e	—	0.65	—
b	0.35	0.40	0.45
x	—	0.08	—
y	—	0.10	—
y_1	—	0.20	—
Z_D	—	0.75	—
Z_E	—	0.75	—

Figure 1.3 BGA 121-pin