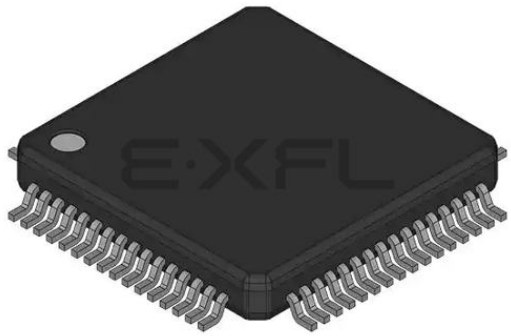

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Core Size	-
Speed	-
Connectivity	-
Peripherals	-
Number of I/O	-
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Program Memory Type	-
EEPROM Size	-
RAM Size	-
Voltage - Supply (Vcc/Vdd)	-
Data Converters	-
Oscillator Type	-
Operating Temperature	-
Mounting Type	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/onsemi/lc87fc096avuef-3h

■Minimum Bus Cycle

- 83.3ns (12MHz) V_{DD}=2.7 to 3.6V
- 125ns (8MHz) V_{DD}=2.5 to 3.6V

Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time

- 250ns (12MHz) V_{DD}=2.7V to 3.6V
- 375ns (8MHz) V_{DD}=2.5V to 3.6V

■Ports

- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1-bit units — 46 (P1n, P2n, P3n, P70 to P73, P80 to P86, PCn, PWM2, PWM3, XT2)
  Ports whose I/O direction can be designated in 4-bit units — 8 (P0n)
- Normal withstand voltage input port — 1 (XT1)
- Dedicated oscillator ports — 2 (CF1, CF2)
- Reset pins — 1 ($\overline{RES}$)
- Power pins — 6(V_{SS}1 to 3, V_{DD}1 to 3)

■Timers

- Timer 0:16-bit timer/counter with a capture register
  Mode 0:8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  Mode 1:8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  Mode 2:16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  Mode 3:16-bit counter (with a 16-bit capture register)
- Timer 1:16-bit timer/counter that supports PWM/toggle outputs
  Mode 0:8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1:8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2:16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  Mode 3:16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM)
- Timer 4:8-bit timer with a 6-bit prescaler
- Timer 5:8-bit timer with a 6-bit prescaler
- Timer 6:8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer 7:8-bit timer with a 6-bit prescaler (with toggle outputs)
- Timer A:16-bit timer
  Mode 0:8-bit timer with an 8-bit programmable prescaler × 2-channels
  Mode 1:16-bit timer with an 8-bit programmable prescaler
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts programmable in 5 different time schemes

■High-Speed Clock Counter

- Can count clocks with a maximum clock rate of 24MHz (at a main clock of 12MHz)
- Can generate output real-time

■Interrupts

- 31 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.

2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/TAL/Infrared remote control receiver
4	0001BH	H or L	INT3/INT5/base timer0/base timer1
5	00023H	H or L	T0H/INT6/TAH
6	0002BH	H or L	T1L/T1H/INT7/SMIIC0
7	00033H	H or L	SIO0/UART1 receive/ UART2 receive
8	0003BH	H or L	SIO1/UART1 transmit/ UART2 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3/RMPWM

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

■Subroutine Stack Levels: 2048 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions

- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, with internal Rf
- Crystal oscillation circuit: For low-speed system clock

■System Clock Divider Function

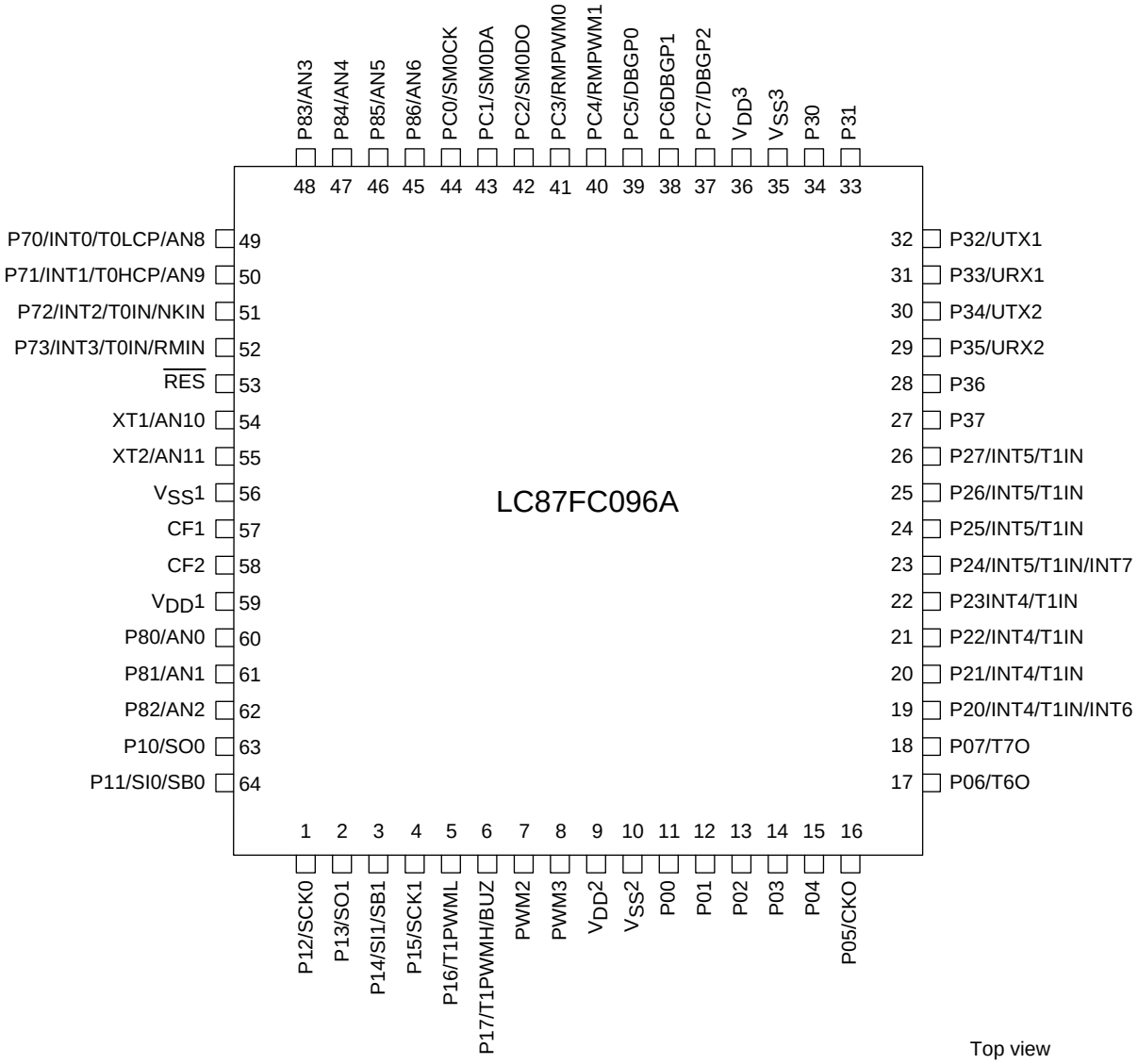
- Can run on low current.
- The minimum instruction cycle selectable from 250ns, 500ns, 1.0µs, 2.0µs, 4.0µs, 8.0µs, 16.0µs, 32.0µs, and 64.0µs (at a main clock rate of 12MHz).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) Canceled by a system reset or occurrence of an interrupt.
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, and crystal oscillators automatically stop operation.
  2) There are three ways of resetting the HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
     (3) Having an interrupt source established at port 0

Continued on next page.

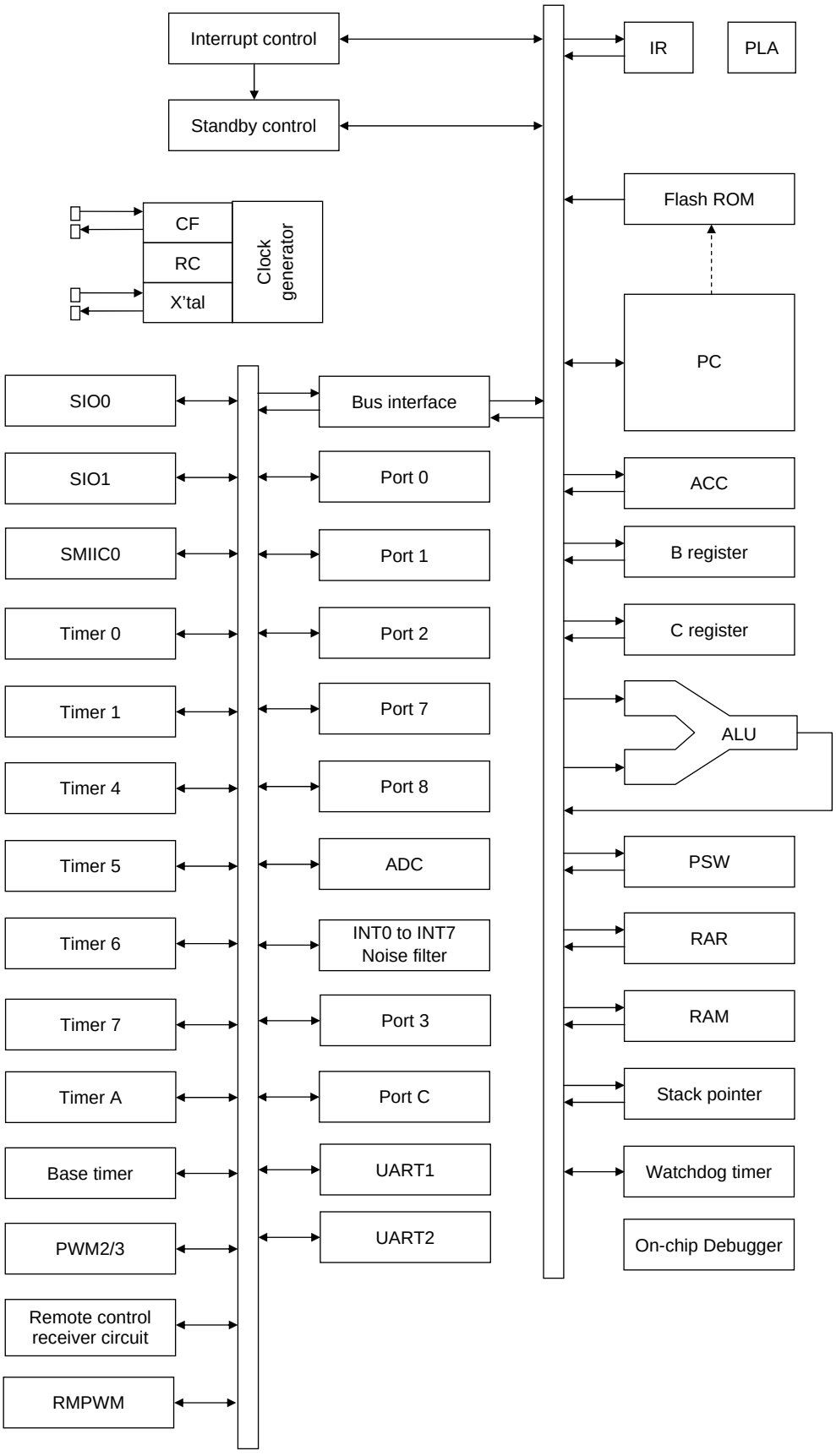
Pin Assignment



Top view

QIP64E (14×14) “Lead-free and halogen-free type”

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$, $V_{SS}2$, $V_{SS}3$</td><td>-</td><td>- Power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$, $V_{DD}2$, $V_{DD}3$</td><td>-</td><td>+ Power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 4-bit units
• Pull-up resistor can be turned on and off in 4-bit units
• HOLD release input
• Port 0 interrupt input
• Shared Pins
P05 : Clock output (system clock / can selected from sub clock)
P06 : Timer 6 toggle output
P07 : Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P10 : SIO0 data output
P11 : SIO0 data input/bus I/O
P12 : SIO0 clock I/O
P13 : SIO1 data output
P14 : SIO1 data input/bus I/O
P15 : SIO1 clock I/O
P16 : Timer 1 PWML output
P17 : Timer 1 PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Other functions
P20: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT6 input/timer 0L capture 1 input
P21 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
P24: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input/INT7 input/timer 0H capture 1 input
P25 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
</td><td>Yes</td></tr>
</table>

Continued on next page.

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Shared pins
P70 : INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71 : INT1 input/HOLD reset input/timer 0H capture input
P72 : INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/
high speed clock counter input
P73 : INT3 input (with noise filter)/timer 0 event input/timer 0H capture input/
remote control receiver input
AD converter input port: AN8 (P70), AN9 (P71)
• Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/
Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table>
</td><td>No</td></tr>
<tr><td>Port 8
P80 to P86</td><td>I/O</td><td>• 7-bit I/O port
• I/O specifiable in 1-bit units
• Shared pins
AD converter input port : AN0 (P80) to AN6 (P86)</td><td>No</td></tr>
<tr><td>PWM2
PWM3</td><td>I/O</td><td>• PWM2 and PWM3 output ports
• General-purpose I/O available</td><td>No</td></tr>
<tr><td>Port 3
P30 to P37</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
P32: UART1 transmit
P33: UART1 receive
P34: UART2 transmit
P35: UART2 receive</td><td>Yes</td></tr>
<tr><td>Port C
PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistor can be turned on and off in 1-bit units
• Pin functions
PC0: SMIIC0 clock input/output
PC1: SMIIC0 bus input/output/data input
PC2: SMIIC0 data output (used in 3-wire SIO mode)
PC3: RMPWM0 output
PC4: RMPWM1 output
PC5: DBGP0
PC6: DBGP1
PC7: DBGP2
DBGP0 to DBGP2: On-chip Debugger</td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin
• Shared pins
General-purpose input port
AD converter input port : AN10
Must be connected to VDD1 if not to be used.</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin
• Shared pins
General-purpose I/O port
AD converter input port : AN11
Must be set for oscillation and kept open if not to be used.</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>Ceramic resonator input pin</td><td>No</td></tr>
<tr><td>CF2</td><td>Output</td><td>Ceramic resonator output pin</td><td>No</td></tr>
</table>

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2 Ports 7, 8 Ports 3, C $\overline{RES}$ PWM2, PWM3	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.5 to 3.6			1	µA
	$I_{IH}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{DD}$	2.5 to 3.6			1	
	$I_{IH}(3)$	CF1	$V_{IN}=V_{DD}$	2.5 to 3.6			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2 Ports 7, 8 Ports 3, C $\overline{RES}$ PWM2, PWM3	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.5 to 3.6	-1			
	$I_{IL}(2)$	XT1, XT2	For input port specification $V_{IN}=V_{SS}$	2.5 to 3.6	-1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	2.5 to 3.6	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2 Ports 3, C	I_{OH}=-0.4mA	3.0 to 3.6	V_{DD}-0.4			V
	$V_{OH}(2)$		I_{OH}=-0.2mA	2.5 to 3.6	V_{DD}-0.4			
	$V_{OH}(3)$	P71 to P73	I_{OH}=-0.4mA	3.0 to 3.6	V_{DD}-0.4			
	$V_{OH}(4)$		I_{OH}=-0.2mA	2.5 to 3.6	V_{DD}-0.4			
	$V_{OH}(5)$	PWM2, PWM3	I_{OH}=-1.6mA	3.0 to 3.6	V_{DD}-0.4			
	$V_{OH}(6)$		I_{OH}=-1mA	2.5 to 3.6	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2 Ports 3, C PWM2, PWM3	I_{OL}=1.6mA	3.0 to 3.6			0.4	
	$V_{OL}(2)$		I_{OL}=1mA	2.5 to 3.6			0.4	
	$V_{OL}(3)$	Ports 7, 8 XT2	I_{OL}=1.6mA	3.0 to 3.6			0.4	
	$V_{OL}(4)$		I_{OL}=1mA	2.5 to 3.6			0.4	
	$V_{OL}(5)$	P00, P01	I_{OL}=5mA	3.0 to 5.5			0.4	
	$V_{OL}(6)$		I_{OL}=2.5mA	2.2 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 7 Ports 3, C	$V_{OH}=0.9V_{DD}$	3.0 to 3.6	15	35	80	kΩ
	Rpu(2)			2.5 to 3.6	15	35	100	
Hysteresis voltage	VHYS	$\overline{RES}$ Ports 1, 2, 7		2.5 to 3.6		0.1 V_{DD}		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.5 to 3.6		10		pF

Serial I/O Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/ Remarks	Conditions	V_{DD} [V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.5 to 3.6	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. • (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.5 to 3.6	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 3.6	0.03			µs
	Data hold time		thDI(1)			2.5 to 3.6	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.5 to 3.6			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.5 to 3.6			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.5 to 3.6			(1/3)tCYC +0.15	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans / rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions		Specification			
						V_{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.5 to 3.6	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.5 to 3.6	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.5 to 3.6	0.03			µs
	Data hold time		thDI(2)			2.5 to 3.6	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.5 to 3.6			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

3-1. SMIIC0 Simple SIO Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions		Specification			
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (4)	SM0CK (PC0)	See Fig. 6.	2.5 to 3.6	4/3			tCYC
		Low level pulse width	tSCKL (4)				2/3			
		High level pulse width	tSCKH (4)				2/3			
	Output clock	Period	tSCK (5)	SM0CK (PC0)	• CMOS output selected • See Fig. 6.	2.5 to 3.6	4/3			
		Low level pulse width	tSCKL (5)				1/2			tSCK
		High level pulse width	tSCKH (5)				1/2			
Serial input	Data setup time		tsDI (3)	SM0DA (PC1)	• Specified with respect to rising edge of SIOCLK • See Fig. 6.	2.5 to 3.6	0.03			µs
	Data hold time		thDI (3)				0.03			
Serial output	Output delay time		tdD0 (5)	SM0DO (PC2), SM0DA (PC1)	• Specified with respect to falling edge of SIOCLK • Specified as interval up to time when output state starts changing. • See Fig. 6.	2.5 to 3.6			1/3tCYC +0.05	

Note 4-3-1: These specifications are theoretical values. Add margin depending on its use.

3-2. SMIIC0 I2C Mode Input/Output Characteristics

Parameter			Symbol	Applicable Pin/Remarks	Conditions	V_{DD}[V]	Specification Min	typ	max	Unit
Clock	Input clock	Period	tSCL	SM0CK (PC0)	• See Fig. 8.	2.5 to 3.6	5			Tfilt
		Low level pulse width	tSCLL				2.5			
		High level pulse width	tSCLH				2			
	Output clock	Period	tSCLx	SM0CK (PC0)	• Specified as interval up to time when output state starts changing.	2.5 to 3.6	10			
		Low level pulse width	tSCLLx				1/2			tSCL
		High level pulse width	tSCLHx				1/2			
SM0CK and SM0DA pins input spike suppression time			tsp	SM0CK (PC0) SM0DA (PC1)	• See Fig. 8.	2.5 to 3.6			1	Tfilt
Bus release time between start and stop	Input		tBUF	SM0CK (PC0) SM0DA (PC1)	• See Fig. 8.	2.5 to 3.6	2.5			Tfilt
	Output		tBUFx	SM0CK (PC0) SM0DA (PC1)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Start/restart condition hold time	Input		tHD;STA	SM0CK (PC0) SM0DA (PC1)	• When SMIIC register control bit, SHDS=0 • See Fig. 8.	2.5 to 3.6	2.0			Tfilt
					• When SMIIC register control bit, SHDS=1 • See Fig. 8.		2.5			
	Output		tHD;STAx	SM0CK (PC0) SM0DA (PC1)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.1			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.0			
Restart condition setup time	Input		tSU;STA	SM0CK (PC0) SM0DA (PC1)	• See Fig. 8.	2.5 to 3.6	1.0			Tfilt
	Output		tSU;STAx	SM0CK (PC0) SM0DA (PC1)	• Standard clock mode • Specified as interval up to time when output state starts changing.		5.5			µs
					• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			

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Parameter		Symbol	Applicable Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	Min	typ	max	Unit
Stop condition setup time	Input	tSU;STO	SM0CK (PC0) SM0DA (PC1)	• See Fig. 8.	2.5 to 3.6	1.0			Tfilt
	Output	tSU;STOx	SM0CK (PC0) SM0DA (PC1)	• Standard clock mode • Specified as interval up to time when output state starts changing.		4.9			µs
				• High-speed clock mode • Specified as interval up to time when output state starts changing.		1.6			
Data hold time	Input	tHD;DAT	SM0CK (PC0) SM0DA (PC1)	• See Fig. 8.	2.5 to 3.6	0			Tfilt
	Output	tHD;DATx	SM0CK (PC0) SM0DA (PC1)	• Specified as interval up to time when output state starts changing.		1		1.5	
Data setup time	Input	tSU;DAT	SM0CK (PC0) SM0DA (PC1)	• See Fig. 8.	2.5 to 3.6	1			Tfilt
	Output	tSU;DATx	SM0CK (PC0) SM0DA (PC1)	• Specified as interval up to time when output state starts changing.		1tSCL-1.5Tfilt			

Note 4-3-2: These specifications are theoretical values. Add margin depending on its use.

Note 4-3-3: The value of Tfilt is determined by the values of the register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	(1/3)tCYC×1
0	1	(1/3)tCYC×2
1	0	(1/3)tCYC×3
1	1	(1/3)tCYC×4

Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range:

250ns Tfilt > 140ns

Note 4-3-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 1

SCL frequency setting ≤ 100kHz

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows:

250ns ≥ Tfilt > 140ns

BRDQ (bit5) = 0

SCL frequency setting ≤ 400kHz

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD} [V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT4(P20 to P23), INT5(P24 to P27) INT6(P20), INT7(P24)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.5 to 3.6	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 3.6	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	2.5 to 3.6	200			µs

AD Converter Characteristics at $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

<12bits AD Converter Mode at Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN6(P86), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		2.5 to 3.6		12		bit
Absolute accuracy	ET		(Note 6-1)	2.5 to 3.6			±16	LSB
Conversion time	TCAD		See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	64		115	µs
				2.7 to 3.6	128		230	
				2.5 to 3.6	256		460	
Analog input voltage range	VAIN			2.5 to 3.6	V_{SS}		V_{DD}	V
Analog port input current	IAINH(1)	analog channel	VAIN=V_{DD}	2.5 to 3.6			1	µA
	IAINL(1)		VAIN=V_{SS}	2.5 to 3.6	-1			

<8bits AD Converter Mode at Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN6(P86), AN8(P70), AN9(P71), AN10(XT1), AN11(XT2)		2.5 to 3.6		8		bit
Absolute accuracy	ET		(Note 6-1)	2.5 to 3.6			±1.5	LSB
Conversion time	TCAD		See Conversion time calculation formulas. (Note 6-2)	3.0 to 3.6	39		71	µs
				2.7 to 3.6	79		140	
				2.5 to 3.6	157		280	
Analog input voltage range	VAIN			2.5 to 3.6	V_{SS}		V_{DD}	V
Analog port input current	IAINH(1)	analog channel	VAIN=V_{DD}	2.5 to 3.6			1	µA
	IAINL(1)		VAIN=V_{SS}	2.5 to 3.6	-1			

12bits AD Converter Mode: TCAD(Conversion time)= ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time)=((32/(AD division ratio))+2)×(1/3)×tCYC

Note 6-1: The quantization error (±1/2LSB) must be excluded from the absolute accuracy. The absolute accuracy must be measured in the microcontroller's state in which no I/O operations occur at the pins adjacent to the analog input channel.

Note 6-2: The conversion time refers to the period from the time an instruction for starting a conversion process till the time the conversion results register(s) are loaded with a complete digital conversion value corresponding to the analog input value.

The conversion time is 2 times the normal-time conversion time when:

- The first AD conversion is performed in the 12-bit AD conversion mode after a system reset.
- The first AD conversion is performed after the AD conversion mode is switched from 8-bit to 12-bit conversion mode.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pins/Remarks	Conditions	V_{DD}[V]	Specification min	Typ	Max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio.	2.7 to 3.6		3.6	9.5	mA
	IDDOP(2)		• FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio.	2.5 to 3.6		2.9	7.1	
	IDDOP(3)		• FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to internal RC oscillation • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	2.5 to 3.6		0.186	0.96	
	IDDOP(4)		• FmCF=0Hz (oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz side. • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	2.5 to 3.6		11.5	58	µA
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1 = V_{DD}2 = V_{DD}3$	• HALT mode • FmCF=12MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio.	2.7 to 3.6		1.5	2.9	mA
	IDDHALT(2)		• HALT mode • FmCF=8MHz ceramic oscillation mode • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/1 frequency division ratio.	2.5 to 3.6		1	1.8	
	IDDHALT(3)		• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'tal=32.768kHz by crystal oscillation mode • System clock set to internal RC oscillation • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	2.5 to 3.6		0.067	0.28	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

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Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	Max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(4)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=0Hz (oscillation stopped) • FmX'al=32.768kHz by crystal oscillation mode. • System clock set to 32.768kHz side. • Internal RC oscillation stopped • frequency variable RC oscillation stopped • 1/2 frequency division ratio.	2.5 to 3.6		7.4	49	µA
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	• HOLD mode • CF1=V_{DD} or open (External clock mode)	2.5 to 3.6		0.04	20	µA
Timer HOLD mode consumption current	IDDHOLD(2)		• Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FmX'tal=32.768kHz by crystal oscillation mode	2.5 to 3.6		5.9	35	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

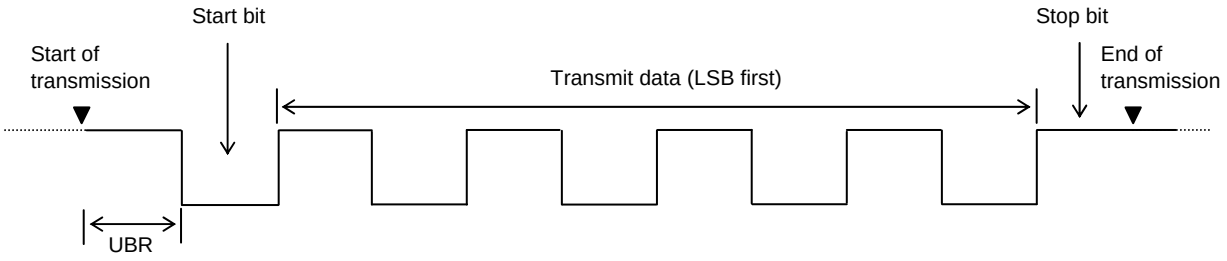
Parameter	Symbol	Pins/Remarks	Conditions	Specification				
				V_{DD}[V]	Min	Typ	Max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Without CPU curent	2.7 to 3.6		7	11	mA
Programming time	tFW(1)		• 2k byte Erasing	2.7 to 3.6		12	15	ms
	tFW(2)		• 2 byte Programming	2.7 to 3.6		35	45	µs

UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

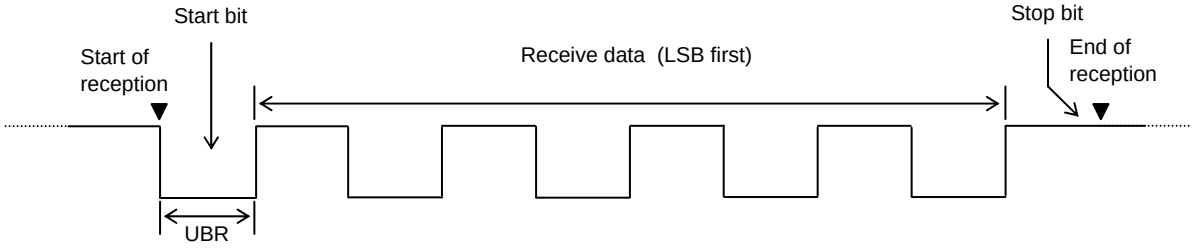
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
			V_{DD} [V]	min	typ	max	unit
Transfer rate	UBR	P32(UTX1), P33(URX1), P34(UTX2), P35(URX2)	2.5 to 3.6	16/3		8192/3	tCYC

Data length: 7, 8, and 9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (first transmit data=55H)



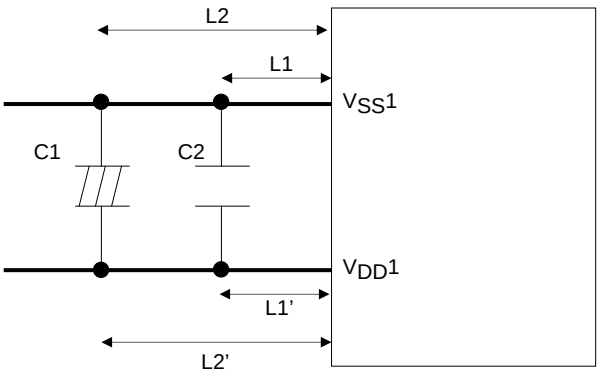
Example of Continuous 8-bit Data Reception Mode Processing (first receive data=55H)



$V_{DD}1$, $V_{SS}1$ Terminal Condition

It is necessary to place capacitors between $V_{DD}1$ and $V_{SS}1$ as describe below.

- Place capacitors as close to $V_{DD}1$ and VSS1 as possible.
- Place capacitors so that the length of each terminal to the each leg of the capacitor be equal (L1 = L1', L2 = L2').
- Place high capacitance capacitor C1 and low capacitance capacitor C2 in parallel.
- Capacitance of C2 must be more than 0.1µF.
- Use thicker pattern for $V_{DD}1$ and $V_{SS}1$.



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	330	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
8MHz		CSTCE8M00G52-R0	(10)	(10)	Open	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
		CSTLS8M00G53-B0	(15)	(15)	Open	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
4MHz		CSTCR4M00G53-R0	(15)	(15)	Open	1.5K	2.2 to 3.6	0.02	0.2	C1, C2 integrated type
		CSTLS4M00G53-B0	(15)	(15)	Open	1.5K	2.2 to 3.6	0.01	0.1	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after VDD goes above the operating voltage lower limit (see Fig. 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	9	9	OPEN	330K	2.2 to 3.6	1.0	3.0	CL=7pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

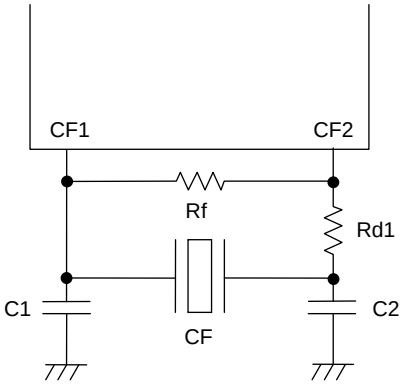


Figure 1 CF Oscillator Circuit

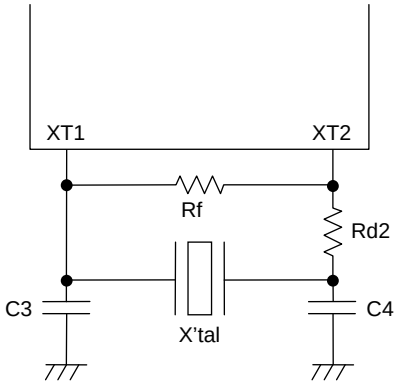


Figure 2 XT Oscillator Circuit

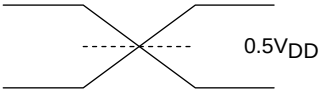
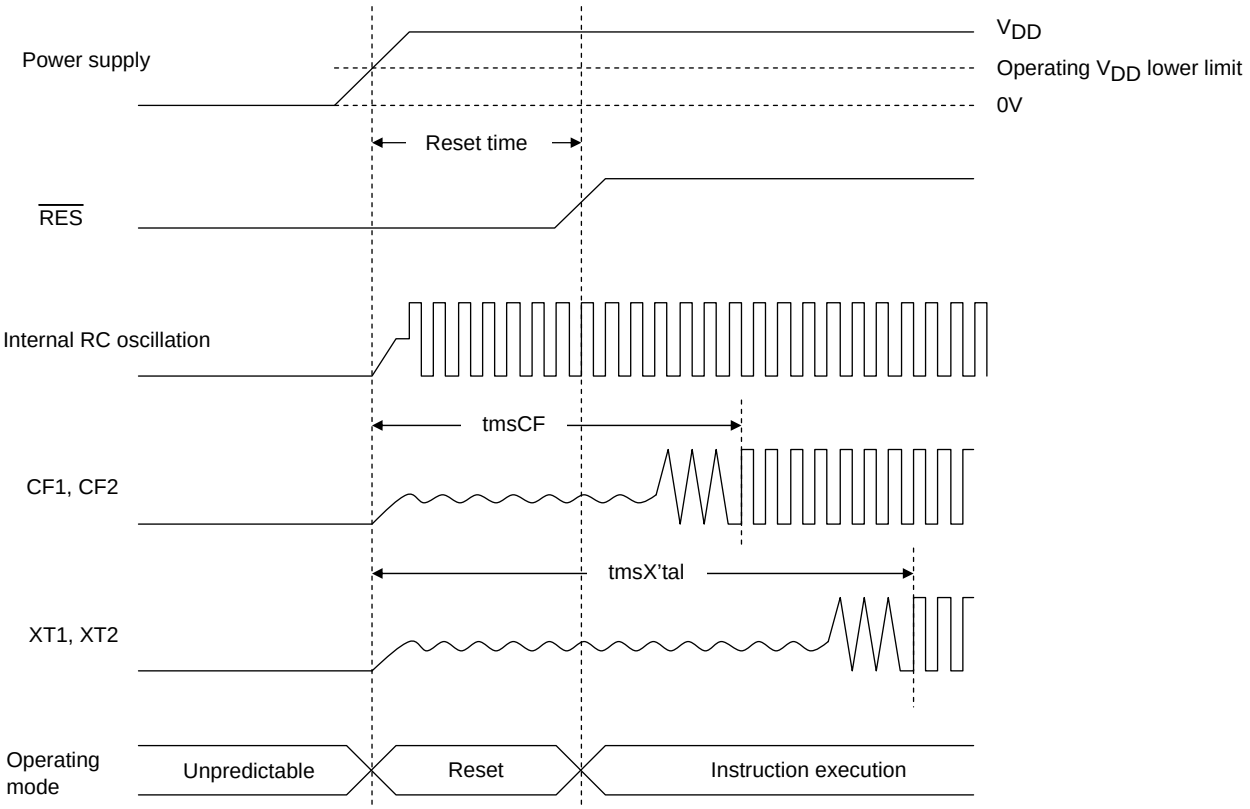
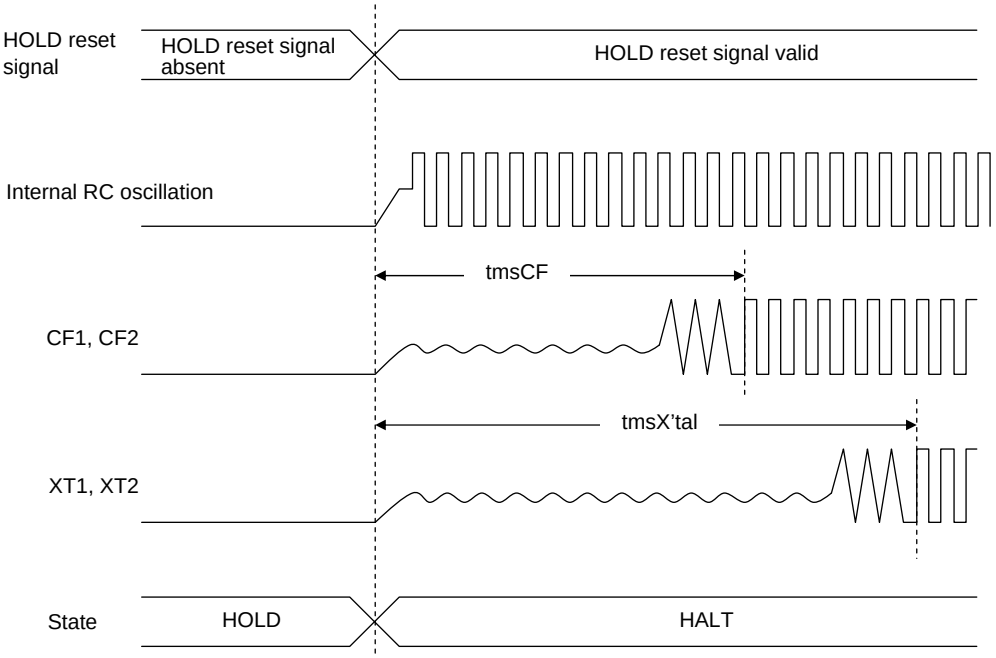


Figure 3 AC Timing Measurement Point

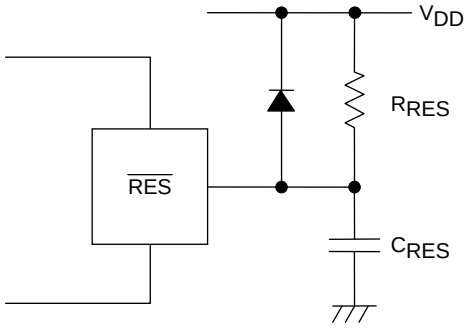


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note :

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200μs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

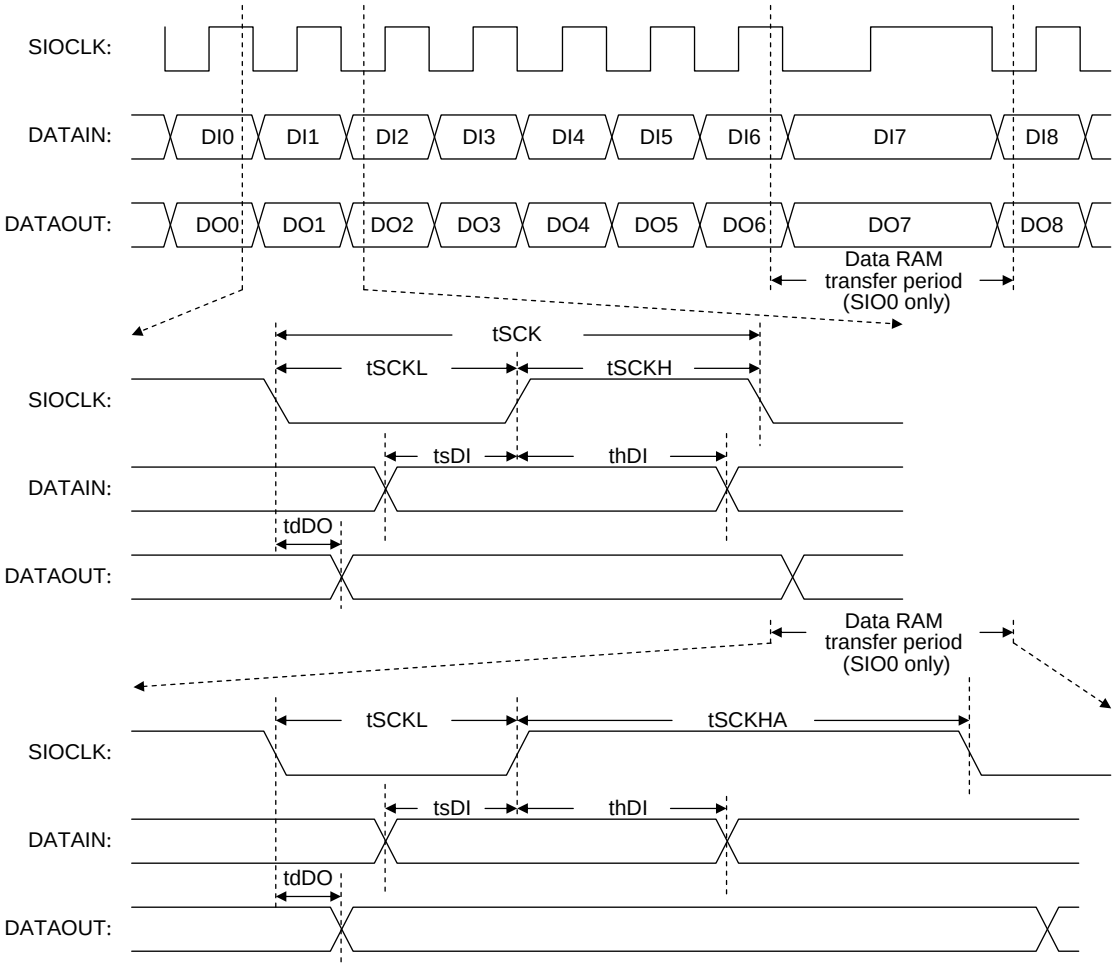


Figure 6 Serial Input/Output Waveforms

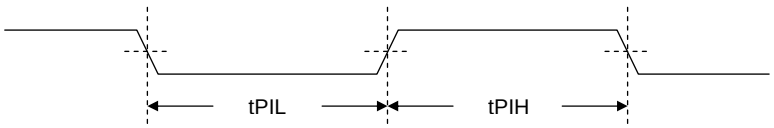
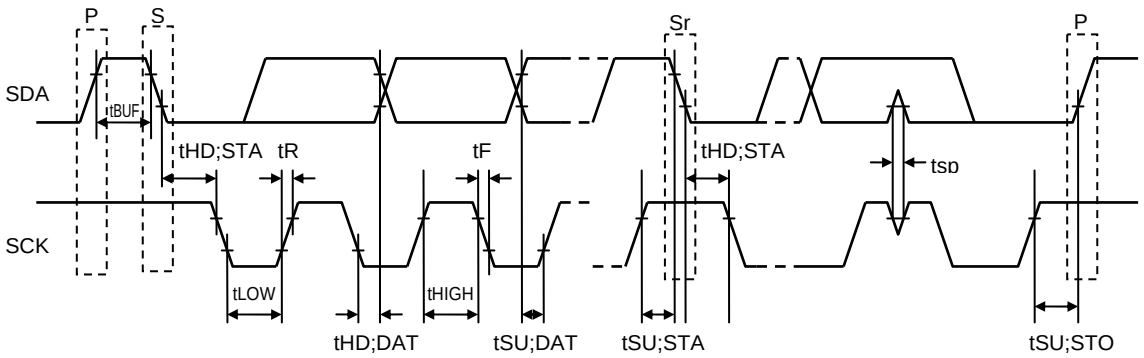


Figure 7 Pulse Input Timing Signal Waveform



S: Start condition
P: Stop condition

Sir: Restart condition

Figure 8 I^2C Timing