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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	I²C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401cbu6tr

Contents

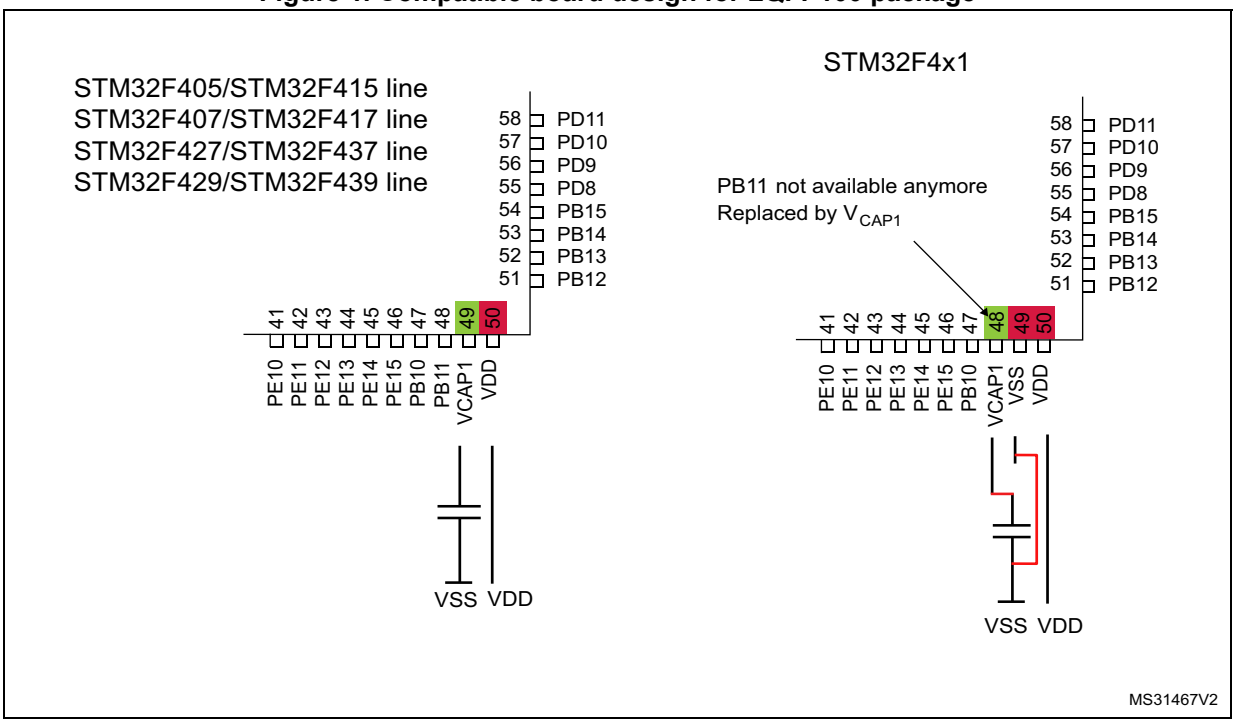
List of tables

2.1 Compatibility with STM32F4 series

The STM32F401xB/STM32F401xC are fully software and feature compatible with the STM32F4 series (STM32F42x, STM32F43x, STM32F41x, STM32F405 and STM32F407)

The STM32F401xB/STM32F401xC can be used as drop-in replacement of the other STM32F4 products but some slight changes have to be done on the PCB board.

Figure 1. Compatible board design for LQFP100 package



3 Functional overview

3.1 ARM® Cortex®-M4 with FPU core with embedded Flash and SRAM

The ARM® Cortex®-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM® Cortex®-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices. The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution. Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F401xB/STM32F401xC devices are compatible with all ARM tools and software.

Figure 3 shows the general block diagram of the STM32F401xB/STM32F401xC.

Note: Cortex®-M4 with FPU is binary compatible with Cortex®-M3.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the ARM® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 105 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 256-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 84 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices embed up to 256 Kbytes of Flash memory available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

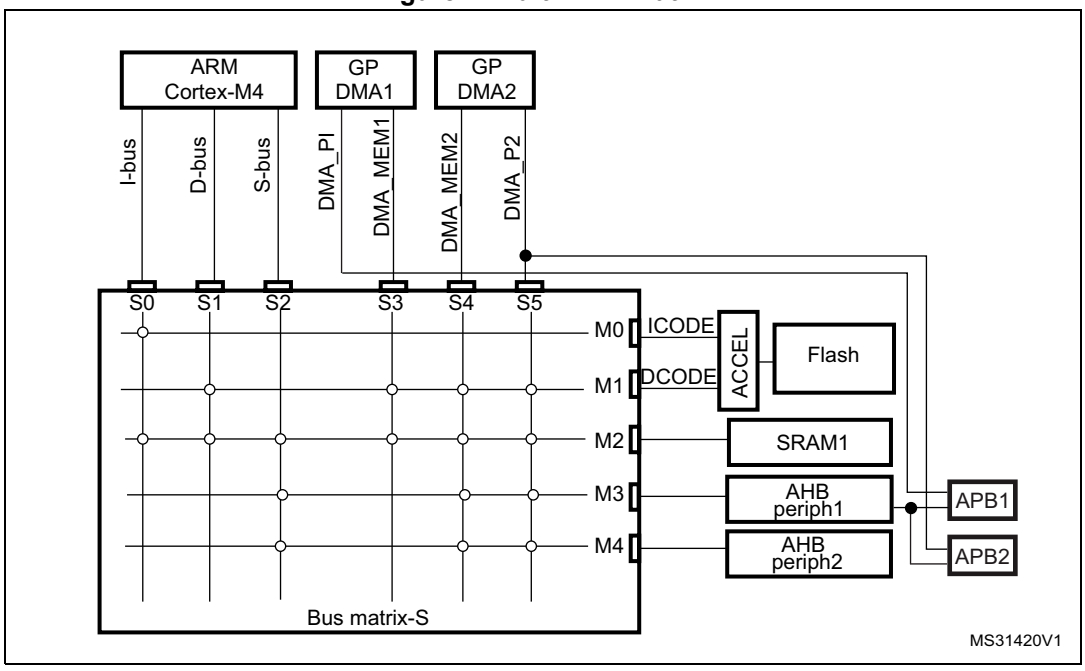
All devices embed:

- Up to 64 Kbytes of system SRAM which can be accessed (read/write) at CPU clock speed with 0 wait states

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 4. Multi-AHB matrix



3.14 Power supply supervisor

3.14.1 Internal reset ON

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V.

The internal power supply supervisor is enabled by holding PDR_ON high.

The devices have an integrated power-on reset (POR) / power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.

The devices remain in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

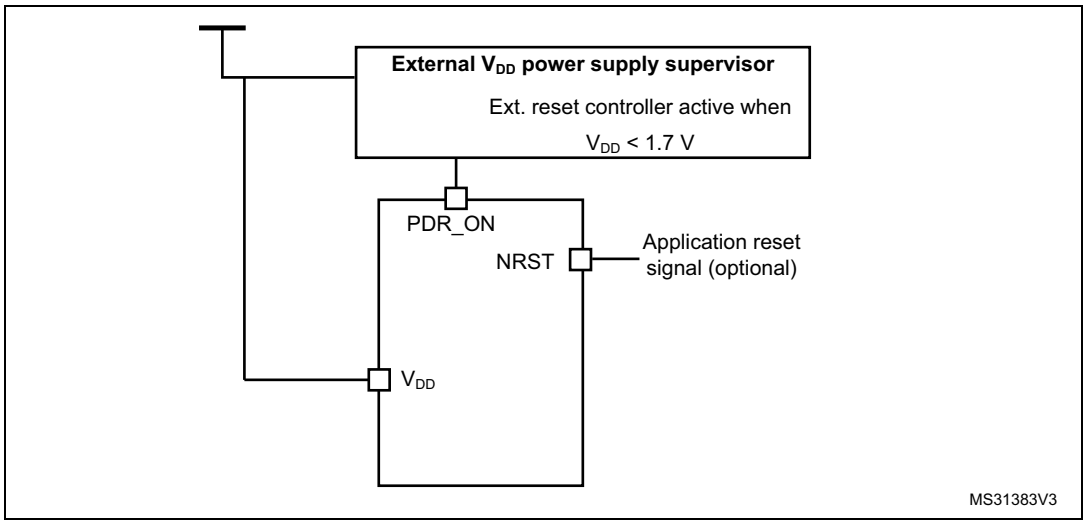
The devices also feature an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

3.14.2 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled by setting the PDR_ON pin to low.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 5: Power supply supervisor interconnection with internal reset OFF*.

Figure 5. Power supply supervisor interconnection with internal reset OFF(1)



1. The PRD_ON pin is only available on the WLCSP49 and UFBGA100 packages.

3.19 Timers and watchdogs

The devices embed one advanced-control timer, seven general-purpose timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control and general-purpose timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max. interface clock (MHz)	Max. timer clock (MHz)
Advanced -control	TIM1	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	84	84
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	84	84
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	84	84

3.19.1 Advanced-control timers (TIM1)

The advanced-control timer (TIM1) can be seen as three-phase PWM generators multiplexed on 4 independent channels. It has complementary PWM outputs with programmable inserted dead times. It can also be considered as a complete general-purpose timer. Its 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

Table 8. STM32F401xB/STM32F401xC pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	WLCSP49	LQFP64	LQFP100	UFBGA100						
13	E4	17	26	L3	PA3	I/O	FT	-	USART2_RX, TIM2_CH4, TIM5_CH4, TIM9_CH2, EVENTOUT	ADC1_IN3
-	-	18	27	-	VSS	S	-	-	-	-
-	-	19	28	-	VDD	S	-	-	-	-
-	-	-	-	E3	BYPASS_ REG	I	FT	-	-	-
14	G6	20	29	M3	PA4	I/O	FT	-	SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK, EVENTOUT	ADC1_IN4
15	F5	21	30	K4	PA5	I/O	FT	-	SPI1_SCK, TIM2_CH1/TIM2_ETR, EVENTOUT	ADC1_IN5
16	F4	22	31	L4	PA6	I/O	FT	-	SPI1_MISO, TIM1_BKIN, TIM3_CH1, EVENTOUT	ADC1_IN6
17	F3	23	32	M4	PA7	I/O	FT	-	SPI1_MOSI, TIM1_CH1N, TIM3_CH2, EVENTOUT	ADC1_IN7
-	-	24	33	K5	PC4	I/O	FT	-	EVENTOUT	ADC1_IN14
-	-	25	34	L5	PC5	I/O	FT	-	EVENTOUT	ADC1_IN15
18	G5	26	35	M5	PB0	I/O	FT	-	TIM1_CH2N, TIM3_CH3, EVENTOUT	ADC1_IN8
19	G4	27	36	M6	PB1	I/O	FT	-	TIM1_CH3N, TIM3_CH4, EVENTOUT	ADC1_IN9
20	G3	28	37	L6	PB2	I/O	FT	-	EVENTOUT	BOOT1
-	-	-	38	M7	PE7	I/O	FT	-	TIM1_ETR, EVENTOUT	-
-	-	-	39	L7	PE8	I/O	FT	-	TIM1_CH1N, EVENTOUT	-
-	-	-	40	M8	PE9	I/O	FT	-	TIM1_CH1, EVENTOUT	-
-	-	-	41	L8	PE10	I/O	FT	-	TIM1_CH2N, EVENTOUT	-
-	-	-	42	M9	PE11	I/O	FT	-	SPI4_NSS, TIM1_CH2, EVENTOUT	-
-	-	-	43	L9	PE12	I/O	FT	-	SPI4_SCK, TIM1_CH3N, EVENTOUT	-
-	-	-	44	M10	PE13	I/O	FT	-	SPI4_MISO, TIM1_CH3, EVENTOUT	-

5 Memory mapping

The memory map is shown in *Figure 15*.

Figure 15. Memory map

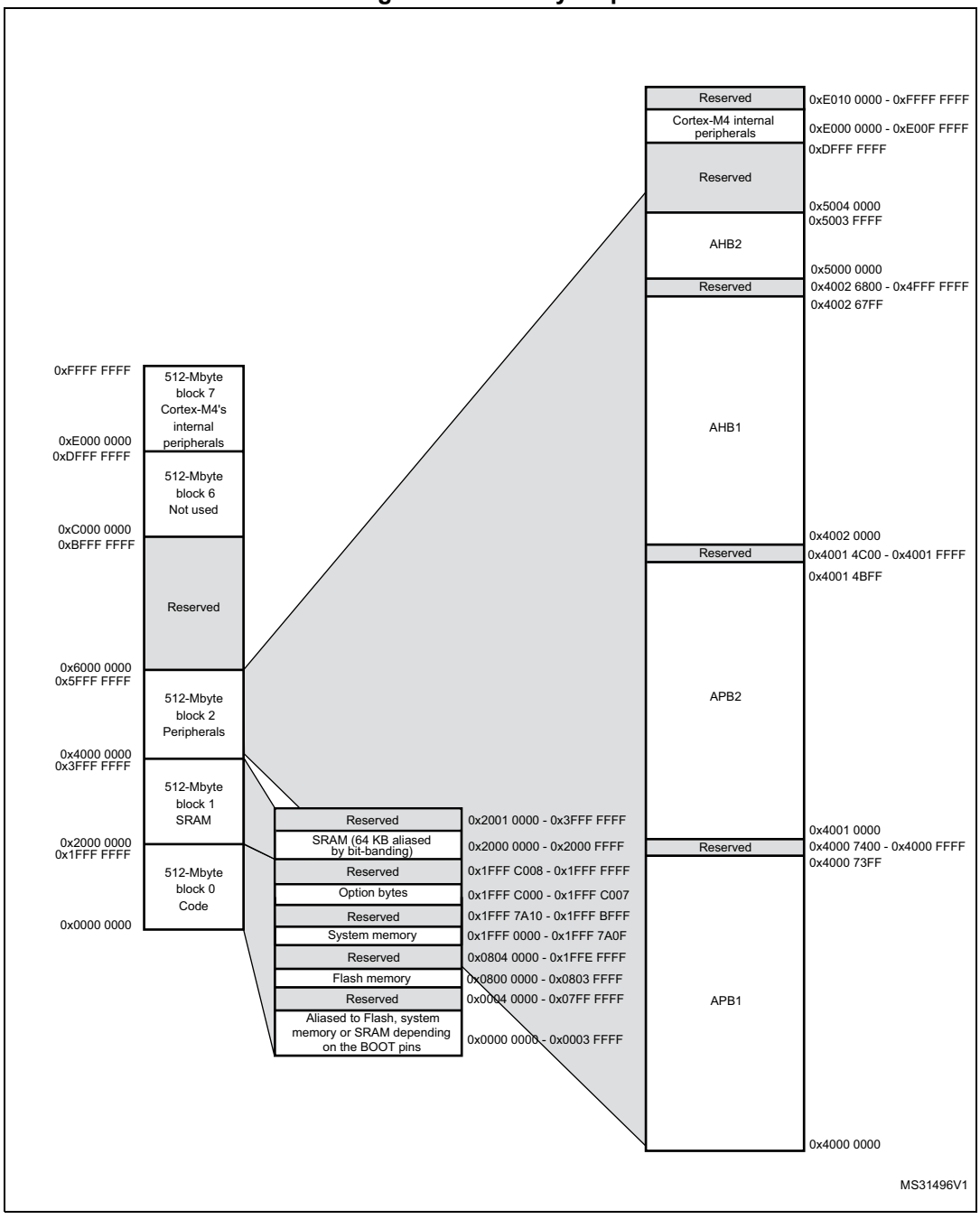


Table 10. STM32F401xB/STM32F401xC register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 4C00- 0x4001 FFFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 17. Input voltage measurement

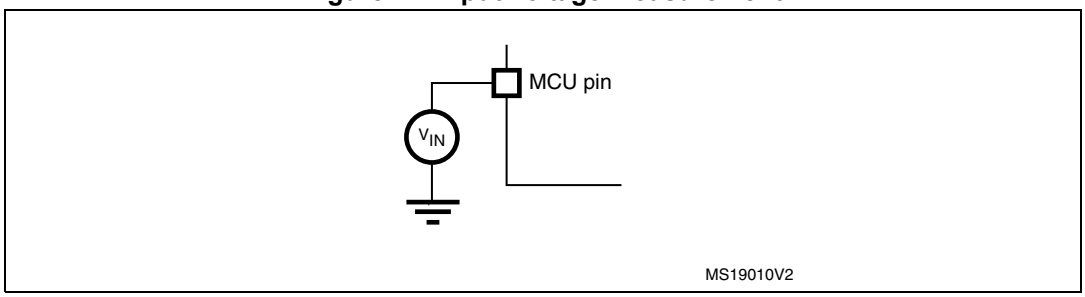


Table 27. Typical and maximum current consumptions in Stop mode - V_{DD}=1.8 V

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Main regulator usage	Flash in Stop mode, all oscillators OFF, no independent watchdog	109	135	440	650	µA
	Low power regulator usage		41	65	310	530(2)	
	Main regulator usage	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	72	95	345	530	
	Low power regulator usage		12	36	260	510(2)	
	Low power low voltage regulator usage		10	27	230	460	

1. Guaranteed by characterization.
2. Guaranteed by test in production.

Table 28. Typical and maximum current consumption in Stop mode - V_{DD}=3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Main regulator usage	Flash in Stop mode, all oscillators OFF, no independent watchdog	111	140	450	670	µA
	Low power regulator usage		42	65	330	560	
	Main regulator usage	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	73	100	360	560	
	Low power regulator usage		12	36	270	520	
	Low power low voltage regulator usage		10	28	230	470	

1. Guaranteed by characterization.

Table 29. Typical and maximum current consumption in Standby mode - V_{DD}=1.8 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE) and RTC ON	2.4	4.0	12.0	24.0	µA
		RTC and LSE OFF	1.8	3.0(3)	11.0	23.0(3)	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization, unless otherwise specified.
3. Guaranteed by test in production.

I/O system current consumption

The current consumption of the I/O system has two components: static and dynamic.

I/O static current consumption

All the I/Os used as inputs with pull-up generate current consumption when the pin is externally held low. The value of this current consumption can be simply computed by using the pull-up/pull-down resistors values given in *Table 54: I/O static characteristics*.

For the output pins, any external pull-down or external load must also be considered to estimate the current consumption.

Additional I/O current consumption is due to I/Os configured as inputs if an intermediate voltage level is externally applied. This current consumption is caused by the input Schmitt trigger circuits used to discriminate the input value. Unless this specific configuration is required by the application, this supply current consumption can be avoided by configuring these I/Os in analog mode. This is notably the case of ADC input pins which should be configured as analog inputs.

Caution: Any floating input pin can also settle to an intermediate voltage level or switch inadvertently, as a result of external electromagnetic noise. To avoid current consumption related to floating pins, they must either be configured in analog mode, or forced internally to a definite digital value. This can be done either by using pull-up/down resistors or by configuring the pins in output mode.

I/O dynamic current consumption

In addition to the internal peripheral current consumption (see *Table 33: Peripheral current consumption*), the I/Os used by an application also contribute to the current consumption. When an I/O pin switches, it uses the current from the MCU supply voltage to supply the I/O pin circuitry and to charge/discharge the capacitive load (internal or external) connected to the pin:

$$I_{SW} = V_{DD} \times f_{SW} \times C$$

where

I_{SW} is the current sunk by a switching I/O to charge/discharge the capacitive load

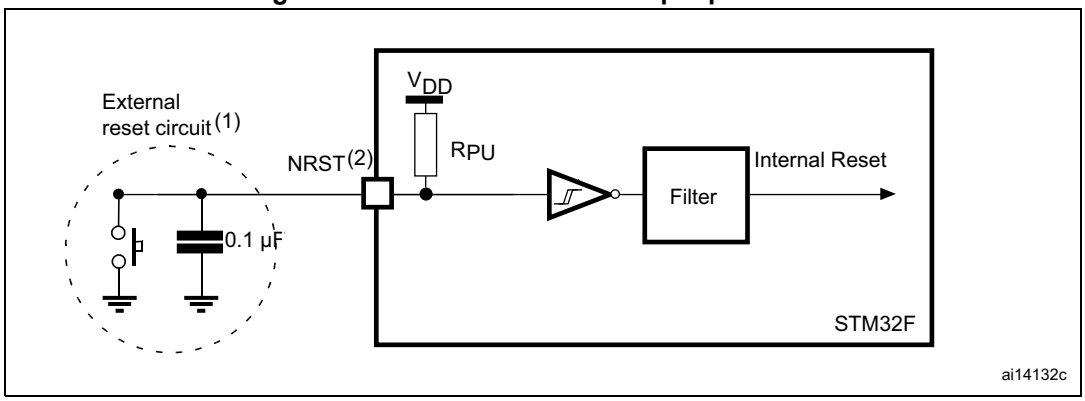
V_{DD} is the MCU supply voltage

f_{SW} is the I/O switching frequency

C is the total capacitance seen by the I/O pin: $C = C_{INT} + C_{EXT}$

The test pin is configured in push-pull output mode and is toggled by software at a fixed frequency.

Figure 32. Recommended NRST pin protection



1. The reset network protects the device against parasitic resets.
2. The external capacitor must be placed as close as possible to the device.
3. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 57*. Otherwise the reset is not taken into account by the device.

6.3.18 TIM timer characteristics

The parameters given in *Table 58* are guaranteed by design.

Refer to *Section 6.3.16: I/O port characteristics* for details on the input/output alternate function characteristics (output compare, input capture, external clock, PWM output).

Table 58. TIMx characteristics(1)(2)

Symbol	Parameter	Conditions(3)	Min	Max	Unit
$t_{res(TIM)}$	Timer resolution time	AHB/APBx prescaler=1 or 2 or 4, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
		AHB/APBx prescaler>4, $f_{TIMxCLK}$ = 84 MHz	1	-	$t_{TIMxCLK}$
			11.9	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	$f_{TIMxCLK}$ = 84 MHz	0	$f_{TIMxCLK}/2$	MHz
			0	42	MHz
Res_{TIM}	Timer resolution		-	16/32	bit
$t_{COUNTER}$	16-bit counter clock period when internal clock is selected	$f_{TIMxCLK}$ = 84 MHz	0.0119	780	µs
t_{MAX_COUNT}	Maximum possible count with 32-bit counter		-	65536 × 65536	$t_{TIMxCLK}$
		$f_{TIMxCLK}$ = 84 MHz	-	51.1	S

1. TIMx is used as a general term to refer to the TIM1 to TIM11 timers.
2. Guaranteed by design.
3. The maximum timer frequency on APB1 is 42 MHz and on APB2 is up to 84 MHz, by setting the TIMPRE bit in the RCC_DCKCFGR register, if APBx prescaler is 1 or 2 or 4, then TIMxCLK = HCKL, otherwise TIMxCLK >= 4x PCLKx.

Table 61. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	3	5	ns
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	2	-	-	ns

1. Guaranteed by characterization.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 34. SPI timing diagram - slave mode and CPHA = 0

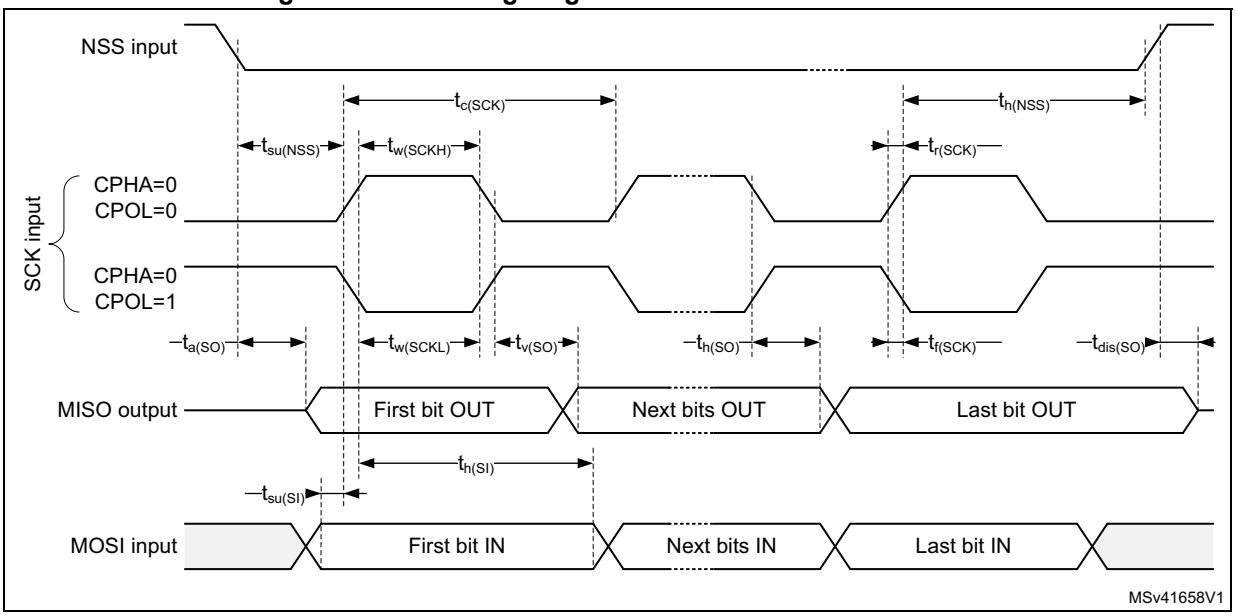
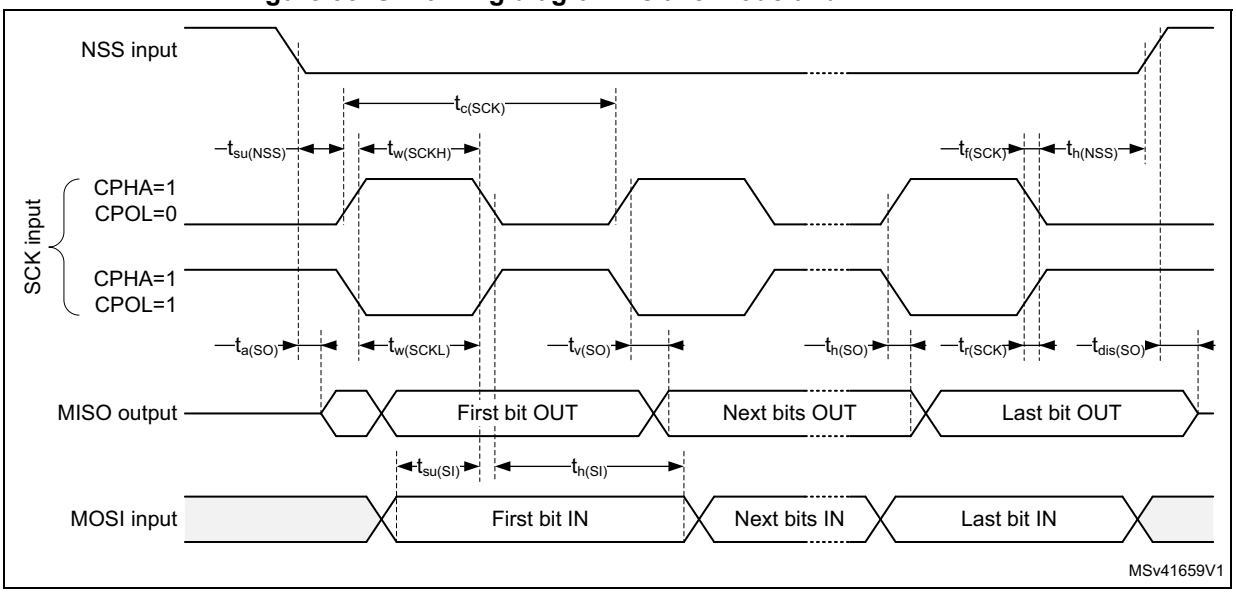


Figure 35. SPI timing diagram - slave mode and CPHA = 1(1)



USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 63. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	USB OTG FS transceiver startup time	1	µs

1. Guaranteed by design.

Table 64. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min.(1)	Typ.	Max.(1)	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0(2)	-	3.6	V
	V_{DI}(3)	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	V_{CM}(3)	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	V_{SE}(3)	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.5 kΩ to 3.6 V(4)	-	-	0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{DD}	17	21	24	kΩ
		PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA11, PA12 (USB_FS_DM/DP)	V_{IN} = V_{SS}	1.5	1.8	2.1	
		PA9 (OTG_FS_VBUS)	V_{IN} = V_{SS}	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_L is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 µA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Table 77. Dynamic characteristics: SD / MMC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp = 24MHz	1.5	-	-	ns
t_{IHD}	Input hold time SD	fpp = 24MHz	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =24MHz	-	4.5	6.5	ns
t_{OHD}	Output hold default time SD	fpp =24MHz	3.5	-	-	

1. Guaranteed by characterization results.
2. V_{DD} = 2.7 to 3.6 V.

6.3.25 RTC characteristics

Table 78. RTC characteristics

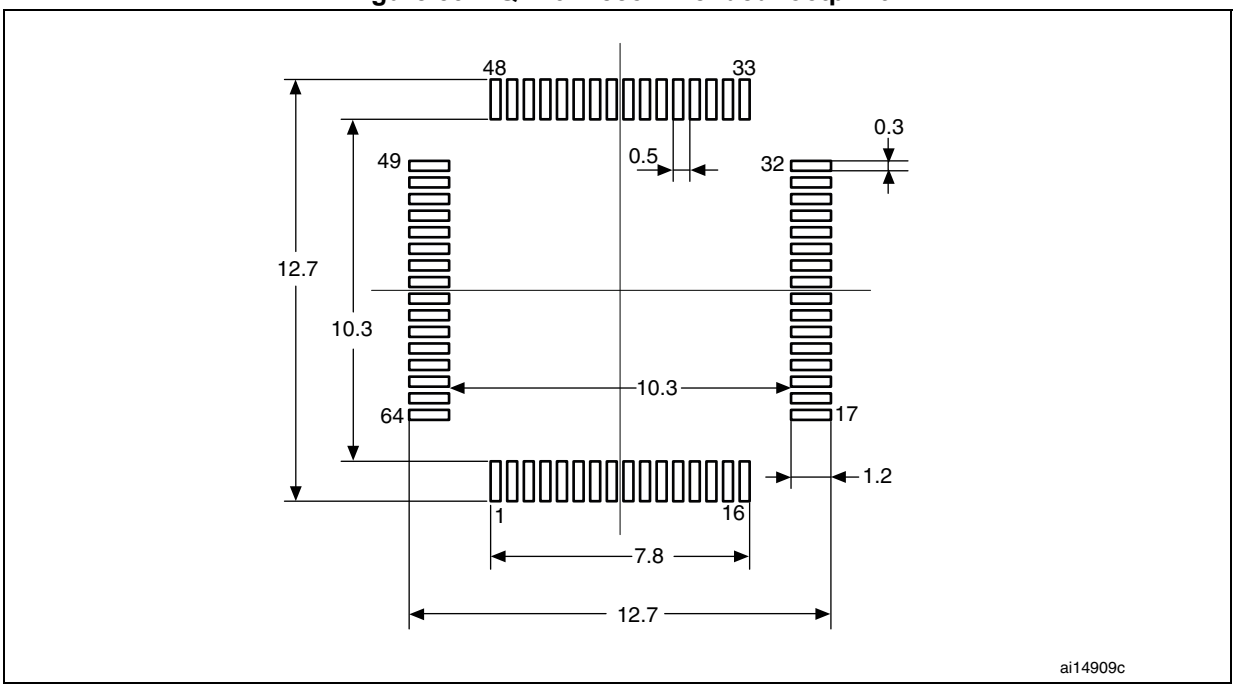
Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

Table 82. LQFP64 - 64-pin, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 53. LQFP64 recommended footprint



1. Dimensions are in millimeters.

Table 88. Document revision history (continued)

Date	Revision	Changes
16-May-2014	4	Change V_{DD}/V_{DDA} minimum value to 1.7 V. Changed number of EXTI lines in *Section 3.10: External interrupt/event controller (EXTI)*. Updated *Figure 18: Power supply scheme*. Updated *Table 11: Voltage characteristics*, *Table 12: Current characteristics* and *Table 14: General operating conditions*. Added note *4.* in *Table 26: Typical and maximum current consumption in Sleep mode*. Updated typical values at T_A = 25 °C in *Table 27: Typical and maximum current consumptions in Stop mode - V_{DD}=1.8 V*. Updated SDIO current consumption in *Table 33: Peripheral current consumption*. Updated *Table 54: I/O static characteristics*, *Table 56: I/O AC characteristics* and added *Figure 30: FT I/O input characteristics*. Updated *Table 55: Output voltage characteristics*. Updated *Table 53: I/O current injection susceptibility* and *Table 57: NRST pin characteristics*. Updated *Table 61: SPI dynamic characteristics*. Updated package dimensions in *Section 7.1* title. Added note below engineering sample marking schematics. Updated UFBGA100 Thermal resistance in *Table 86: Package thermal characteristics*.