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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	I²C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	36
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 10x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401ccu7

2 Description

The STM32F401xB/STM32F401xC devices are based on the high-performance ARM® Cortex®-M4 32-bit RISC core operating at a frequency of up to 84 MHz. The Cortex®-M4 core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F401xB/STM32F401xC incorporate high-speed embedded memories (up to 256 Kbytes of Flash memory, up to 64 Kbytes of SRAM), and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer one 12-bit ADC, a low-power RTC, six general-purpose 16-bit timers including one PWM timer for motor control, two general-purpose 32-bit timers. They also feature standard and advanced communication interfaces.

- Up to three I^2Cs
- Up to four SPIs
- Two full duplex I^2Ss. To achieve audio class accuracy, the I^2S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Three USARTs
- SDIO interface
- USB 2.0 OTG full speed interface

Refer to *Table 2: STM32F401xB/C features and peripheral counts* for the peripherals available for each part number.

The STM32F401xB/STM32F401xC operate in the –40 to +105 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F401xB/STM32F401xC microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub

Figure 3 shows the general block diagram of the devices.

Table 2. STM32F401xB/C features and peripheral counts

Peripherals		STM32F401xB			STM32F401xC		
Flash memory in Kbytes		128			256		
SRAM in Kbytes	System	64					
Timers	General-purpose	7					
	Advanced-control	1					
Communication interfaces	SPI/ I^2S	3/2 (full duplex)		4/2 (full duplex)	3/2 (full duplex)		4/2 (full duplex)
	I^2C	3					
	USART	3					
	SDIO	-	1		-	1	
USB OTG FS		1					
GPIOs		36	50	81	36	50	81
12-bit ADC Number of channels		1					
		10	16		10	16	
Maximum CPU frequency		84 MHz					
Operating voltage		1.7 to 3.6 V					
Operating temperatures		Ambient temperatures: –40 to +85 °C/–40 to +105 °C					
		Junction temperature: –40 to + 125 °C					
Package		WLCSP49 UFQFPN48	LQFP64	UFBGA100 LQFP100	WLCSP49 UFQFPN48	LQFP64	UFBGA100 LQFP100

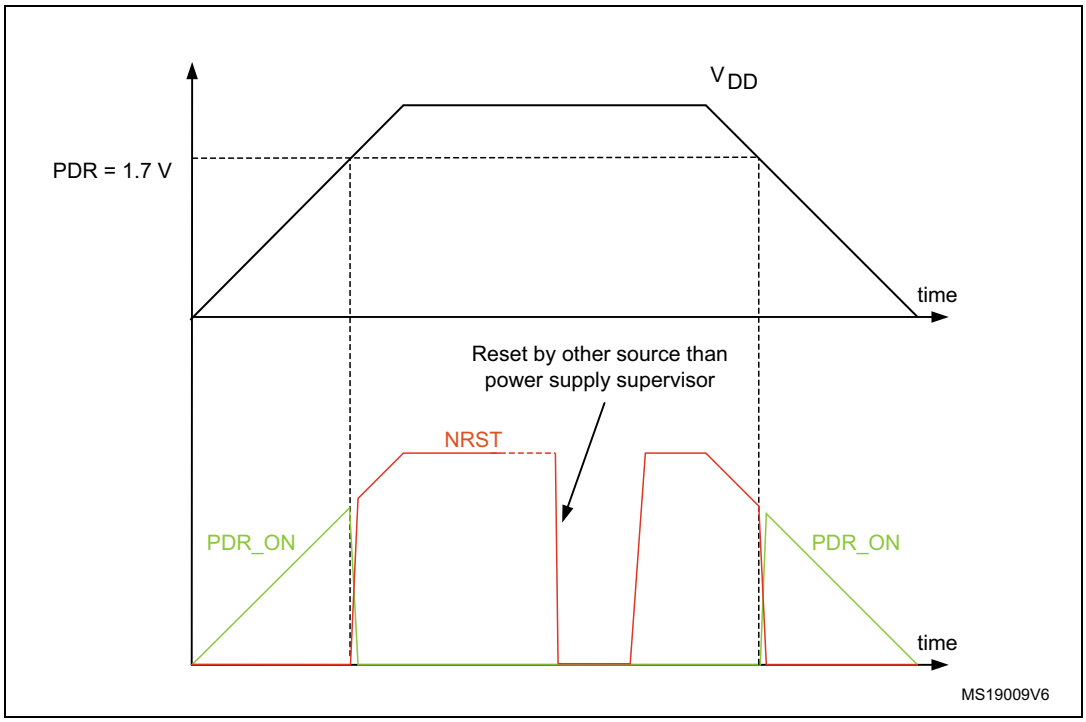
The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 6*).

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

Figure 6. PDR_ON control with internal reset OFF



3.15 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

Table 8. STM32F401xB/STM32F401xC pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	WLCSP49	LQFP64	LQFP100	UFBGA100						
-	-	-	45	M11	PE14	I/O	FT	-	SPI4_MOSI, TIM1_CH4, EVENTOUT	-
-	-	-	46	M12	PE15	I/O	FT	-	TIM1_BKIN, EVENTOUT	-
21	E3	29	47	L10	PB10	I/O	FT	-	SPI2_SCK/I2S2_CK, I2C2_SCL, TIM2_CH3, EVENTOUT	-
-	-	-	-	K9	PB11	I/O	FT	-	TIM2_CH4, I2C2_SDA, EVENTOUT	-
22	G2	30	48	L11	VCAP_1	S	-	-	-	-
23	D3	31	49	F12	VSS	S	-	-	-	-
24	F2	32	50	G12	VDD	S	-	-	-	-
25	E2	33	51	L12	PB12	I/O	FT	-	SPI2_NSS/I2S2_WS, I2C2_SMBA, TIM1_BKIN, EVENTOUT	-
26	G1	34	52	K12	PB13	I/O	FT	-	SPI2_SCK/I2S2_CK, TIM1_CH1N, EVENTOUT	-
27	F1	35	53	K11	PB14	I/O	FT	-	SPI2_MISO, I2S2ext_SD, TIM1_CH2N, EVENTOUT	-
28	E1	36	54	K10	PB15	I/O	FT	-	SPI2_MOSI/I2S2_SD, TIM1_CH3N, EVENTOUT	RTC_REFIN
-	-	-	55	-	PD8	I/O	FT	-	EVENTOUT	-
-	-	-	56	K8	PD9	I/O	FT	-	EVENTOUT	-
-	-	-	57	J12	PD10	I/O	FT	-	EVENTOUT	-
-	-	-	58	J11	PD11	I/O	FT	-	EVENTOUT	-
-	-	-	59	J10	PD12	I/O	FT	-	TIM4_CH1, EVENTOUT	-
-	-	-	60	H12	PD13	I/O	FT	-	TIM4_CH2, EVENTOUT	-
-	-	-	61	H11	PD14	I/O	FT	-	TIM4_CH3, EVENTOUT	-
-	-	-	62	H10	PD15	I/O	FT	-	TIM4_CH4, EVENTOUT	-
-	-	37	63	E12	PC6	I/O	FT	-	I2S2_MCK, USART6_TX, TIM3_CH1, SDIO_D6, EVENTOUT	-
-	-	38	64	E11	PC7	I/O	FT	-	I2S3_MCK, USART6_RX, TIM3_CH2, SDIO_D7, EVENTOUT	-

Table 9. Alternate function mapping

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port A	PA0	-	TIM2_CH1/ TIM2_ETR	TIM5_CH1	-	-	-	-	USART2_ CTS	-	-	-	-	-	-	-	EVENT OUT
	PA1	-	TIM2_CH2	TIM5_CH2	-	-	-	-	USART2_ RTS	-	-	-	-	-	-	-	EVENT OUT
	PA2	-	TIM2_CH3	TIM5_CH3	TIM9_CH1	-	-	-	USART2_ TX	-	-	-	-	-	-	-	EVENT OUT
	PA3	-	TIM2_CH4	TIM5_CH4	TIM9_CH2	-		-	USART2_ RX	-	-	-	-	-	-	-	EVENT OUT
	PA4	-	-	-	-	-	SPI1_NSS	SPI3_NSS/ I2S3_WS	USART2_ CK	-	-	-	-	-	-	-	EVENT OUT
	PA5	-	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA6	-	TIM1_BKIN	TIM3_CH1	-	-	SPI1_ MISO	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA7	-	TIM1_CH1N	TIM3_CH2	-	-	SPI1_ MOSI	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA8	MCO_1	TIM1_CH1	-	-	I2C3_SCL	-	-	USART1_ CK	-	-	OTG_FS_ SOF	-	-	-	-	EVENT OUT
	PA9	-	TIM1_CH2	-	-	I2C3_ SMBA	-	-	USART1_ TX	-	-	OTG_FS_ VBUS	-	-	--	-	EVENT OUT
	PA10	-	TIM1_CH3	-	-	-	-	-	USART1_ RX	-	-	OTG_FS_I D	-	-	-	-	EVENT OUT
	PA11	-	TIM1_CH4	-	-	-	-	-	USART1_ CTS	USART6_ TX	-	OTG_FS_ DM	-	-	-	-	EVENT OUT
	PA12	-	TIM1_ETR	-	-	-	-	-	USART1_ RTS	USART6_ RX	-	OTG_FS_ DP	-	-	-	-	EVENT OUT
	PA13	JTMS_ SWDIO	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA14	JTCK_ SWCLK	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PA15	JTDI	TIM2_CH1/ TIM2_ETR	-	-	-	SPI1_NSS	SPI3_NSS/ I2S3_WS	-	-	-	-	-	-	-	-	EVENT OUT

Table 9. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port E	PE0	-	-	TIM4_ETR	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE1	-	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE2	TRACECLK	-	-	-	-	SPI4_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE3	TRACED0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE4	TRACED1	-	-	-	-	SPI4_NSS	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE5	TRACED2	-	-	TIM9_CH1	-	SPI4_MISO	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE6	TRACED3	-	-	TIM9_CH2	-	SPI4_MOSI	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE7	-	TIM1_ETR	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE8	-	TIM1_CH1N	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE9	-	TIM1_CH1	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE10	-	TIM1_CH2N	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE11	-	TIM1_CH2	-	-	-	SPI4_NSS	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE12	-	TIM1_CH3N	-	-	-	SPI4_SCK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE13	-	TIM1_CH3	-	-	-	SPI4_MISO	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE14	-	TIM1_CH4	-	-	-	SPI4_MOSI	-	-	-	-	-	-	-	-	-	EVENT OUT
	PE15	-	TIM1_BKIN	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

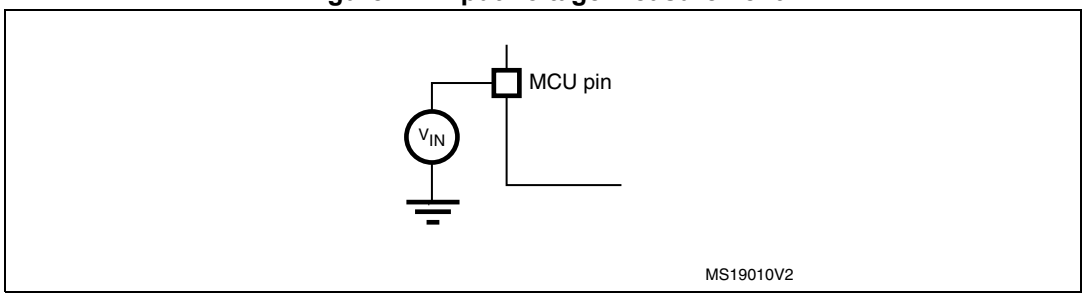
Table 10. STM32F401xB/STM32F401xC register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB2	0x4001 4C00- 0x4001 FFFF	Reserved
	0x4001 4800 - 0x4001 4BFF	TIM11
	0x4001 4400 - 0x4001 47FF	TIM10
	0x4001 4000 - 0x4001 43FF	TIM9
	0x4001 3C00 - 0x4001 3FFF	EXTI
	0x4001 3800 - 0x4001 3BFF	SYSCFG
	0x4001 3400 - 0x4001 37FF	SPI4/I2S4
	0x4001 3000 - 0x4001 33FF	SPI1
	0x4001 2C00 - 0x4001 2FFF	SDIO
	0x4001 2400 - 0x4001 2BFF	Reserved
	0x4001 2000 - 0x4001 23FF	ADC1
	0x4001 1800 - 0x4001 1FFF	Reserved
	0x4001 1400 - 0x4001 17FF	USART6
	0x4001 1000 - 0x4001 13FF	USART1
	0x4001 0800 - 0x4001 0FFF	Reserved
	0x4001 0400 - 0x4001 07FF	TIM8
	0x4001 0000 - 0x4001 03FF	TIM1
	0x4000 7400 - 0x4000 FFFF	Reserved

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 17*.

Figure 17. Input voltage measurement



Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in input mode with a static value at VDD or VSS (no load).
- All peripherals are disabled except if it is explicitly mentioned.
- The Flash memory access time is adjusted to both f_{HCLK} frequency and VDD ranges (refer to *Table 15: Features depending on the operating power supply range*).
- The voltage scaling is adjusted to f_{HCLK} frequency as follows:
  - Scale 3 for $f_{HCLK} \leq 60$ MHz
  - Scale 2 for 60 MHz < $f_{HCLK} \leq 84$ MHz
- The system clock is HCLK, $f_{PCLK1} = f_{HCLK}/2$, and $f_{PCLK2} = f_{HCLK}$.
- External clock is 4 MHz and PLL is on when f_{HCLK} is higher than 25 MHz.
- The maximum values are obtained for V_{DD} = 3.6 V and a maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Table 20. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} =1.8V

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A= 25 °C	T_A=85 °C	T_A=105 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(2)(3)	84	20.0	21	22	23(4)	mA
			60	14.5	15	16	17	
			40	10.4	11	12	13	
			20	5.5	6	7	8	
		External clock, all peripherals disabled(3)	84	10.9	11	13	14(4)	
			60	8.0	9	10	11	
			40	5.8	6	7	8	
			20	3.2	4	5	6	

1. Guaranteed by characterization, unless otherwise specified.
2. When analog peripheral blocks such as ADC, HSE, LSE, HSI, or LSI are ON, an additional power consumption has to be considered.
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
4. Guaranteed by test in production.

Table 33. Peripheral current consumption (continued)

Peripheral		I_{DD} (typ)	Unit
APB2 (up to 84MHz)	TIM1	5.71	µA/MHz
	TIM9	2.86	
	TIM10	1.79	
	TIM11	2.02	
	ADC1(2)	2.98	
	SPI1	1.19	
	USART1	3.10	
	USART6	2.86	
	SDIO	5.95	
	SPI4	1.31	
	SYSCFG	0.71	

1. I2SMOD bit set in SPI_I2SCFGR register, and then the I2SE bit set to enable I2S peripheral.
2. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.

6.3.7 Wakeup time from low-power modes

The wakeup times given in *Table 34* are measured starting from the wakeup event trigger up to the first instruction executed by the CPU:

- For Stop or Sleep modes: the wakeup event is WFE.
- WKUP (PA0) pin is used to wakeup from Standby, Stop and Sleep modes.

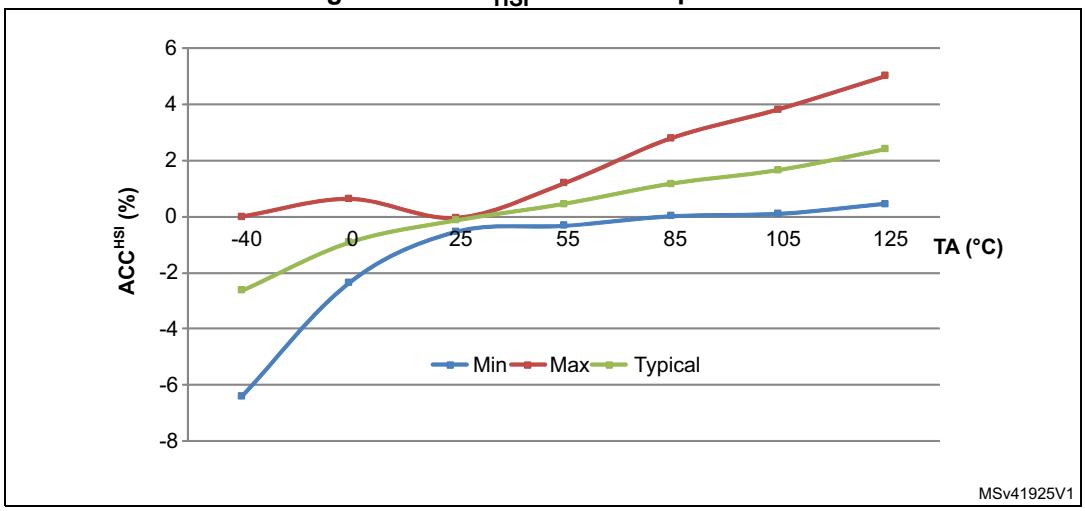
All timings are derived from tests performed under ambient temperature and V_{DD}=3.3 V.

Table 34. Low-power mode wakeup timings(1)

Symbol	Parameter	Min(1)	Typ(1)	Max(1)	Unit
$t_{WUSLEEP}$(2)	Wakeup from Sleep mode	-	4	6	CPU clock cycle
t_{WUSTOP}(2)	Wakeup from Stop mode, usage of main regulator	-	13.5	14.5	µs
	Wakeup from Stop mode, usage of main regulator, Flash memory in Deep power down mode	-	105	111	
	Wakeup from Stop mode, regulator in low power mode	-	21	33	
	Wakeup from Stop mode, regulator in low power mode, Flash memory in Deep power down mode	-	113	130	
$t_{WUSTDBY}$(2)(3)	Wakeup from Standby mode	-	314	407	µs

1. Guaranteed by characterization.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. $t_{WUSTDBY}$ maximum value is given at –40 °C.

Figure 26. ACC_{HSI} versus temperature



1. Guaranteed by characterization.

Low-speed internal (LSI) RC oscillator

Table 40. LSI oscillator characteristics (1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{LSI} (2)	Frequency	17	32	47	kHz
$t_{su(LSI)}$ (3)	LSI oscillator startup time	-	15	40	µs
$I_{DD(LSI)}$ (3)	LSI oscillator power consumption	-	0.4	0.6	µA

1. V_{DD} = 3 V, T_A = –40 to 105 °C unless otherwise specified.
2. Guaranteed by characterization.
3. Guaranteed by design.

Table 55. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}(1)	Output low level voltage for an I/O pin	CMOS port(2) I_{IO} = +8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4	-	
V_{OL} (1)	Output low level voltage for an I/O pin	TTL port(2) I_{IO} =+8 mA 2.7 V ≤V_{DD} ≤3.6 V	-	0.4	V
V_{OH} (3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +20 mA 2.7 V ≤V_{DD} ≤3.6 V	-	1.3(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–1.3(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +6 mA 1.8 V ≤V_{DD} ≤3.6 V	-	0.4(4)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(4)	-	
V_{OL}(1)	Output low level voltage for an I/O pin	I_{IO} = +4 mA 1.7 V ≤V_{DD} ≤3.6 V	-	0.4(5)	V
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DD}–0.4(5)	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in *Table 12*. and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in *Table 12* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}.
4. Guaranteed by characterization.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 31* and *Table 56*, respectively.

Unless otherwise specified, the parameters given in *Table 56* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 56. I/O AC characteristics(1)(2)

OSPEEDRy [1:0] bit value(1)	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{max(IO)out}$	Maximum frequency(3)	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	4	MHz
			C_L = 50 pF, V_{DD}≥ 1.7 V	-	-	2	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	8	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	4	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} = 1.7 V to 3.6 V	-	-	100	ns

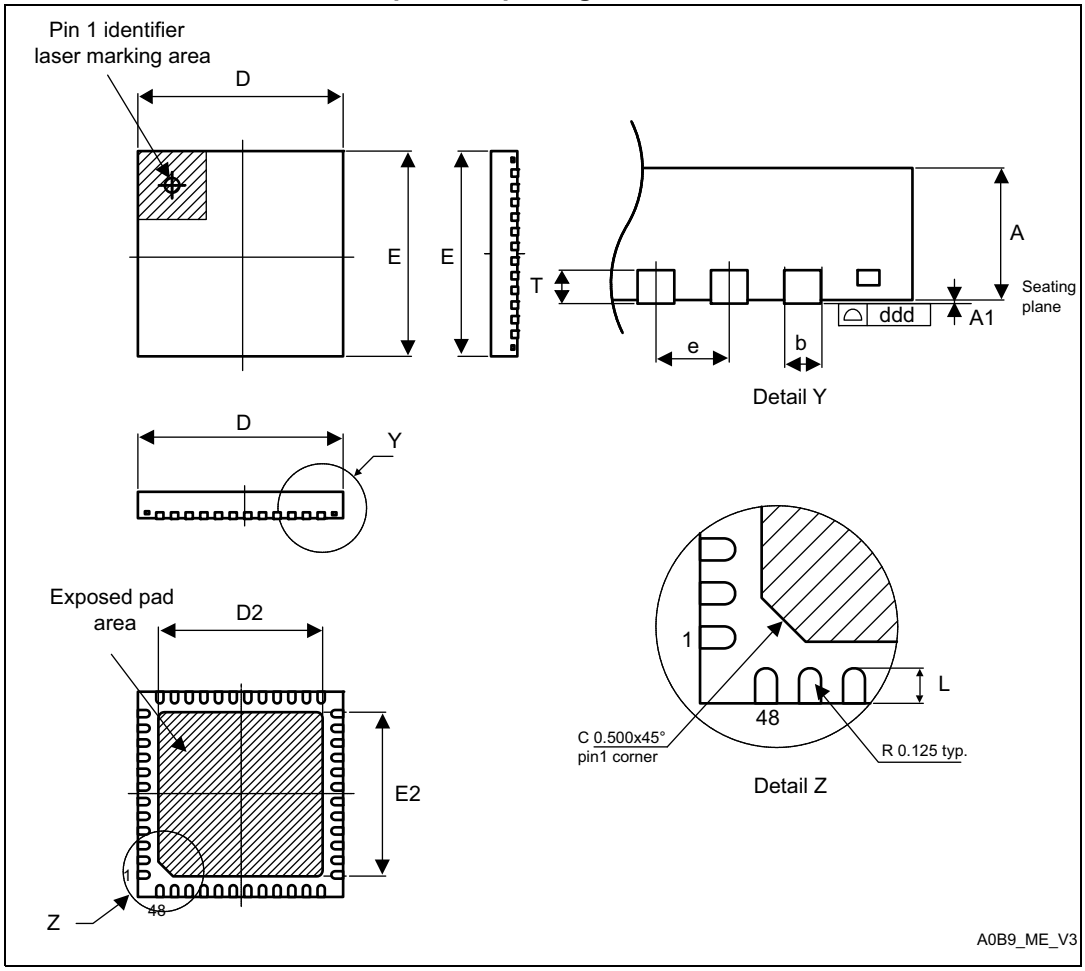
Table 66. ADC characteristics (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{lat}(2)	Injection trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.100	µs
			-	-	3(5)	$1/f_{ADC}$
t_{latr}(2)	Regular trigger conversion latency	f_{ADC} = 30 MHz	-	-	0.067	µs
			-	-	2(5)	$1/f_{ADC}$
t_S(2)	Sampling time	f_{ADC} = 30 MHz	0.100	-	16	µs
			3	-	480	$1/f_{ADC}$
t_{STAB}(2)	Power-up time		-	2	3	µs
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 30 MHz 12-bit resolution	0.50	-	16.40	µs
		f_{ADC} = 30 MHz 10-bit resolution	0.43	-	16.34	µs
		f_{ADC} = 30 MHz 8-bit resolution	0.37	-	16.27	µs
		f_{ADC} = 30 MHz 6-bit resolution	0.30	-	16.20	µs
		9 to 492 (t_S for sampling +n-bit resolution for successive approximation)				$1/f_{ADC}$
f_S(2)	Sampling rate (f_{ADC} = 30 MHz, and t_S = 3 ADC cycles)	12-bit resolution Single ADC	-	-	2	Msps
		12-bit resolution Interleave Dual ADC mode	-	-	3.75	Msps
		12-bit resolution Interleave Triple ADC mode	-	-	6	Msps
I_{VREF+}(2)	ADC V_{REF} DC current consumption in conversion mode		-	300	500	µA
I_{VDDA}(2)	ADC V_{DDA} DC current consumption in conversion mode		-	1.6	1.8	mA

1. V_{DDA} minimum value of 1.7 V is possible with the use of an external power supply supervisor (refer to *Section 3.14.2: Internal reset OFF*).
2. Guaranteed by characterization.
3. V_{REF+} is internally connected to V_{DDA} and V_{REF-} is internally connected to V_{SSA}.
4. R_{ADC} maximum value is given for V_{DD}=1.7 V, and minimum value for V_{DD}=3.3 V.
5. For external triggers, a delay of $1/f_{PCLK2}$ must be added to the latency specified in *Table 66*.

7.2 UFQFPN48 package information

Figure 49. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package outline



1. Drawing is not to scale.
2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.
3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 81. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

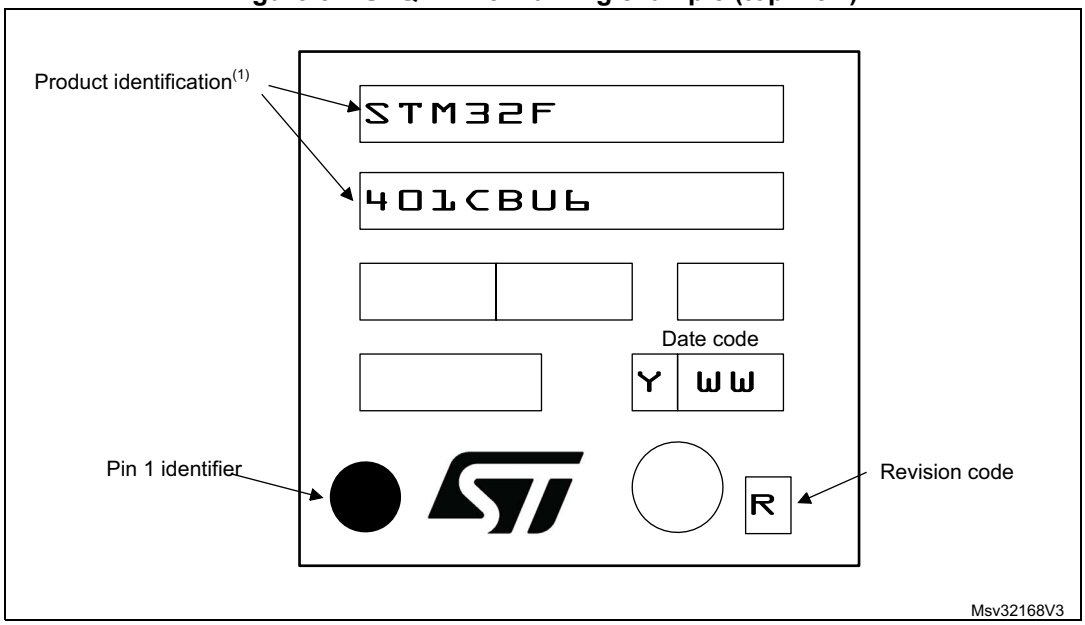
Symbol	millimeters			inches(1)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244

UFQFPN48 device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Other optional marking or inset/upset marks, which depend on supply chain operations, are not indicated below.

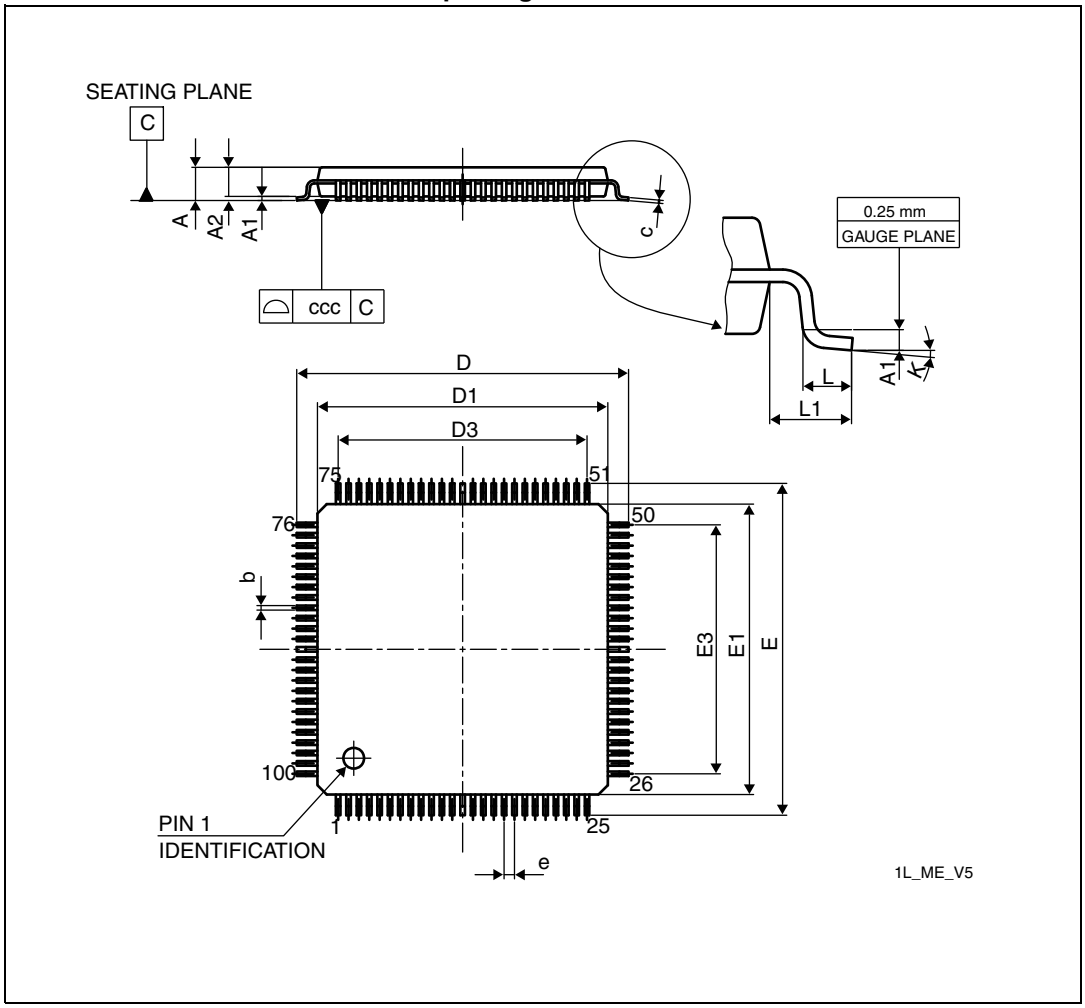
Figure 51. UFQFPN48 marking example (top view)



1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

7.4 LQFP100 package information

Figure 55. LQFP100 - 100-pin, 14 x 14 mm, 100-pin low-profile quad flat package outline



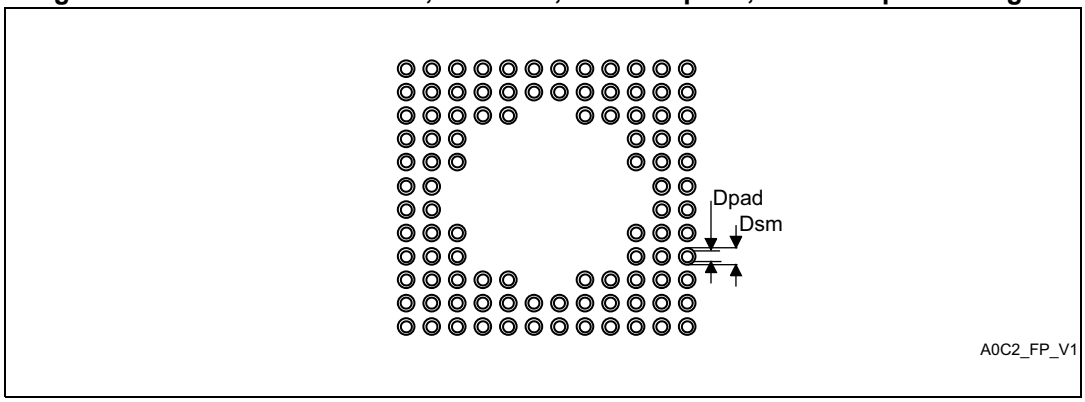
1. Drawing is not to scale.

Table 84. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 59. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid



array
package recommended footprint

Table 85. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

9 Revision history

Table 88. Document revision history

Date	Revision	Changes
23-Jul-2013	1	Initial release.
06-Sep-2013	2	Updated product status to production data Added I2C 1 MBit/s in *Features* Updated *Figure 1: Compatible board design for LQFP100 package* Added notes and revised the main function after reset columnn *Table 8: STM32F401xB/STM32F401xC pin definitions*. Replaced 'I2S2_CKIN' signal name with 'I2S_CKIN' and added EVENTOUT alternate function in *Table 8: STM32F401xB/STM32F401xC pin definitions* and *Table 9: Alternate function mapping* Updated *Section 3.28: Analog-to-digital converter (ADC)* Updated the reference of $V_{ESD(CDM)}$ in *Table 51: ESD absolute maximum ratings* Updated *Section 3.20: Inter-integrated circuit interface (I2C)*, including *Table 5: Comparison of I2C analog and digital filters* Removed first sentence ("Unless otherwise specified...") in *I2C interface characteristics* Changed the order of the tables in *Section 6.3.6: Supply current characteristics* Modified the "SDA and SCL rise time" fast mode I2C minimum value in *Table 59: I^2C characteristics* Updated *Figure 33: I^2C bus AC waveforms and measurement circuit* and *Table 60: SCL frequency (f_{PCLK1}= 42 MHz, V_{DD} = V_{DD_I2C} = 3.3 V)* Replaced "Marking of engineering samples" sections with "Marking of samples" sections, and added *UFBGA100 device marking* section for package UFGBA100 in *Section 7: Package information*
08-Nov-2013	3	Updated UFBGA100 in *Table 86: Package thermal characteristics*. Changed WLCSP49 package measurements to 3 x 3 mm in *Section 7.1*.

Table 88. Document revision history (continued)

Date	Revision	Changes
06-Aug-2015	5	Changed current consumption to 128 µA/MHz on cover page. Updated *Table 3: Regulator ON/OFF and internal power supply supervisor availability* for UFQFPN48. Updated *Figure 10: STM32F401xB/STM32F401xC WLCSP49 pinout* to show top view instead of bump view. Renamed VCAP1/2 into VCAP_1/_2 in *Figure 10: STM32F401xB/STM32F401xC WLCSP49 pinout*, *Figure 11: STM32F401xB/STM32F401xC UFQFPN48 pinout*, *Figure 13: STM32F401xB/STM32F401xC LQFP100 pinout* and *Figure 14: STM32F401xB/STM32F401xC UFBGA100 pinout*. In whole *Section 6: Electrical characteristics*, modified notes related to characteristics guaranteed by design and by tests during characterization. Updated PLS[2:0]=101 (falling edge) in *Table 19: Embedded reset and power control block characteristics*. Updated *Table 39: HSI oscillator characteristics*. Updated V_{HYS} in *Table 56: I/O AC characteristics*. Added t_{SP} in *Table 59: I^2C characteristics*. Removed note 1 in *Table 67: ADC accuracy at f_{ADC} = 18 MHz*, *Table 68: ADC accuracy at f_{ADC} = 30 MHz* and *Table 69: ADC accuracy at f_{ADC} = 36 MHz*. Added WLCSP49 *Figure 47: WLCSP49 0.4 mm pitch wafer level chip scale recommended footprint* and *Table 80: WLCSP49 recommended PCB design rules (0.4 mm pitch)*. Added *Section : WLCSP49 device marking*. Updated *Section : UFQFPN48 device marking*. Updated *Table 82: LQFP64 - 64-pin, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data* and *Section : LQFP64 device marking*. Updated *Section : LQFP64 device marking* and *Section : LQFP100 device marking* Updated *Table 84: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data*, *Figure 59: UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint*. Added *Table 85: UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)*. updated *Section : UFBGA100 device marking*. Added Temperature range 7 in *Table 87: Ordering information scheme*.