STMicroelectronics - STM32F401RBT6TR Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	I²C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401rbt6tr

List of figures

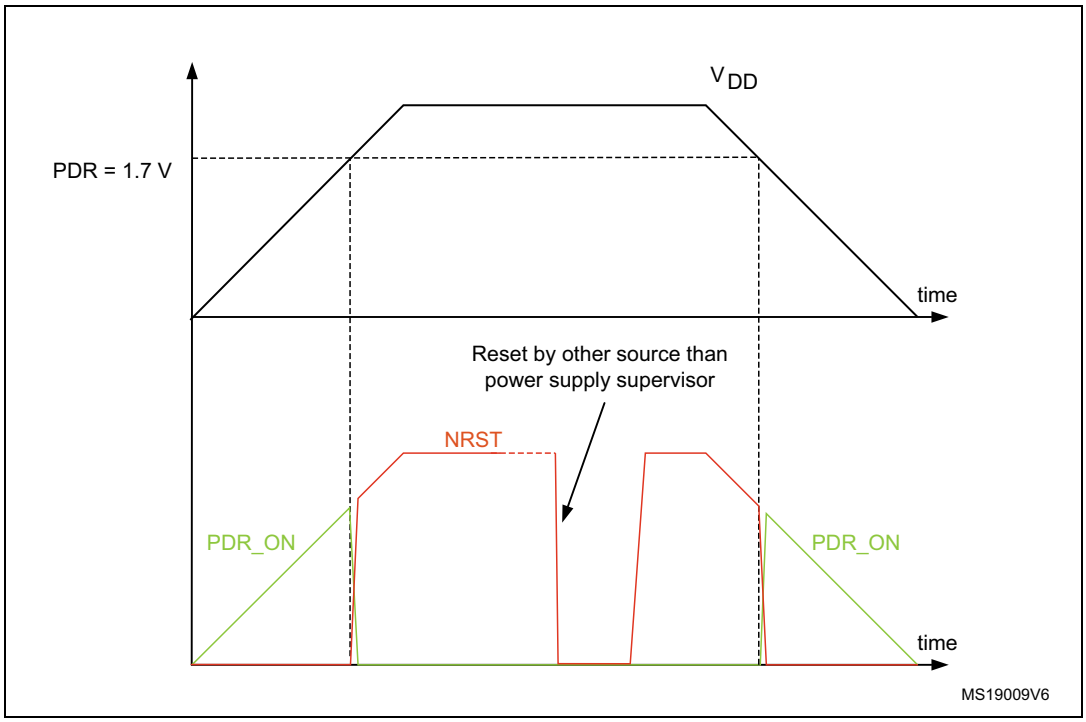
The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.7 V (see *Figure 6*).

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no longer supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled.
- The brownout reset (BOR) circuitry must be disabled.
- The embedded programmable voltage detector (PVD) is disabled.
- V_{BAT} functionality is no more available and VBAT pin should be connected to V_{DD}.

Figure 6. PDR_ON control with internal reset OFF



3.15 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

3.19.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.20 Inter-integrated circuit interface (I^2C)

Up to three I^2C bus interfaces can operate in multimaster and slave modes. They can support the standard (up to 100 kHz) and fast (up to 400 kHz) modes. The I2C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.They also support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 5*).

Table 5. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks

3.21 Universal synchronous/asynchronous receiver transmitters (USART)

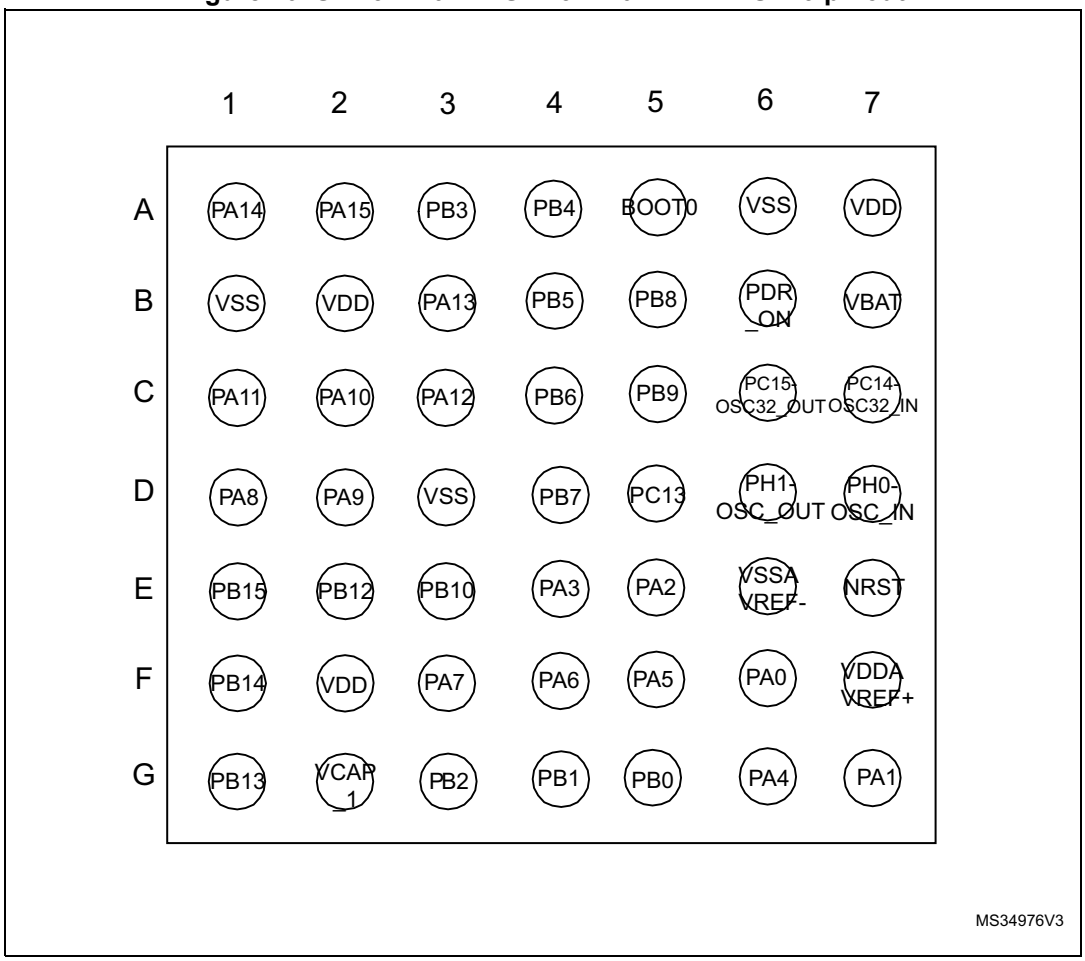
The devices embed three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART6).

These three interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The USART2 interface communicates at up to 5.25 bit/s.

USART1 and USART2 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

4 Pinouts and pin description

Figure 10. STM32F401xB/STM32F401xC WLCSP49 pinout



1. The above figure shows the package top view.

Table 8. STM32F401xB/STM32F401xC pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	WLCSP49	LQFP64	LQFP100	UFBGA100						
47	A6	63	99	-	VSS	S	-	-	-	-
-	B6	-	-	H3	PDR_ON	I	FT	-	-	-
48	A7	64	100	-	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F401xx reference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA100 and the BYPASS_REG pin is set to VDD (Regulator off/internal reset ON mode), then PA0 is used as an internal Reset (active low)

Table 9. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port C	PC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC2	-	-	-	-	-	SPI2_ MISO	I2S2ext_SD	-	-	-	-	-	-	-	-	EVENT OUT
	PC3	-	-	-	-	-	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC4	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC6	-	--	TIM3_CH1	-	-	I2S2_MCK	-	-	USART6_ TX	-	-	-	SDIO_ D6	-	-	EVENT OUT
	PC7	-		TIM3_CH2	-	-	-	I2S3_MCK	-	USART6_ RX	-	-	-	SDIO_ D7	-	-	EVENT OUT
	PC8	-	-	TIM3_CH3	-	-	-	-	-	USART6_ CK	-	-	-	SDIO_ D0	-	-	EVENT OUT
	PC9	MCO_2	-	TIM3_CH4	-	I2C3_SDA	I2S_CKIN	-	-	-	-	-	-	SDIO_ D1	-	-	EVENT OUT
	PC10	-	-	-	-	-	-	SPI3_SCK/ I2S3_CK	-	-	-	-	-	SDIO_ D2	-	-	EVENT OUT
	PC11	-	-	-	-	-	I2S3ext_ SD	SPI3_MISO	-	-	-	-	-	SDIO_ D3	-	-	EVENT OUT
	PC12	-	-	-	-	-	-	SPI3_MOSI/ I2S3_SD	-	-	-	-	-	SDIO_ CK	-	-	EVENT OUT
	PC13	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PC15	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 9. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port D	PD0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD2	-	-	TIM3_ETR	-	-	-	-	-	-	-	-	-	SDIO_ CMD	-	-	EVENT OUT
	PD3	-	-	-	-	-	SPI2_SCK/ I2S2_CK	-	USART2_ CTS	--	-	-	-	-	-	-	EVENT OUT
	PD4	-	-	-	-	-	-	-	USART2_ RTS		-	-	-	-	-	-	EVENT OUT
	PD5	-	-	-	-	-	-	-	USART2_ TX	-	-	-	-	-	-	-	EVENT OUT
	PD6	-	-	-	-	-	SPI3_MOSI /I2S3_SD	-	USART2_ RX	-	-	-	-	-	-	-	EVENT OUT
	PD7	-	-	-	-	-	-	-	USART2_ CK	-	-	-	-	-	-	-	EVENT OUT
	PD8	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD9	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD11	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD12	-	-	TIM4_CH1	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD13	-	-	TIM4_CH2	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD14	-	-	TIM4_CH3	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PD15	-	-	TIM4_CH4	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT

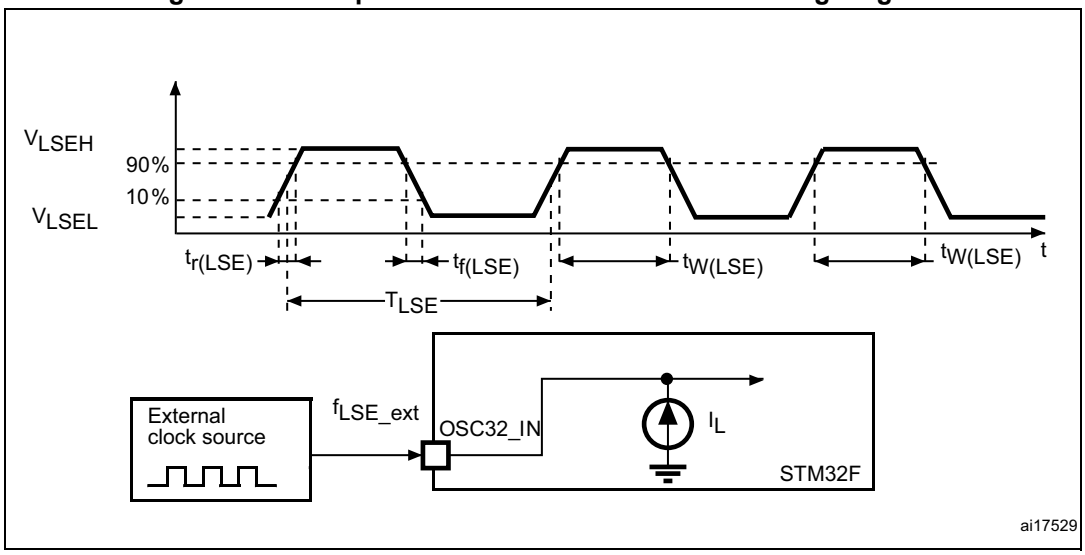
6.3 Operating conditions

6.3.1 General operating conditions

Table 14. General operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HCLK}	Internal AHB clock frequency	Power Scale3: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x01	0	-	60	MHz
		Power Scale2: Regulator ON, VOS[1:0] bits in PWR_CR register = 0x10	0	-	84	
f_{PCLK1}	Internal APB1 clock frequency		0	-	42	
f_{PCLK2}	Internal APB2 clock frequency		0	-	84	
V_{DD}	Standard operating voltage		1.7(1)	-	3.6	V
V_{DDA} (2)(3)	Analog operating voltage (ADC limited to 1.2 M samples)	Must be the same potential as V_{DD}(4)	1.7(1)	-	2.4	
	Analog operating voltage (ADC limited to 2.4 M samples)		2.4	-	3.6	
V_{BAT}	Backup operating voltage		1.65	-	3.6	
V_{12}	Regulator ON: 1.2 V internal voltage on V_{CAP_1}/V_{CAP_2} pins	VOS[1:0] bits in PWR_CR register = 0x01 Max frequency 60 MHz	1.08(5)	1.14	1.20(5)	
		VOS[1:0] bits in PWR_CR register = 0x10 Max frequency 84 MHz	1.20(5)	1.26	1.32(5)	
V_{12}	Regulator OFF: 1.2 V external voltage must be supplied on V_{CAP_1}/V_{CAP_2} pins	Max. frequency 60 MHz.	1.1	1.14	1.2	
		Max. frequency 84 MHz.	1.2	1.26	1.32	
V_{IN}	Input voltage on RST and FT pins(6)	$2\ V \le V_{DD} \le 3.6\ V$	–0.3	-	5.5	
		$V_{DD} \le 2\ V$	–0.3	-	5.2	
	Input voltage on BOOT0 pin		0	-	9	
P_D	Maximum allowed package power dissipation for suffix 6 and 7(7)	UFQFPN48	-	-	625	mW
		WLCSP49	-	-	385	
		LQFP64	-	-	313	
		LQFP100	-	-	465	
		UFBGA100	-	-	323	

Figure 23. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 37. HSE 4-26 MHz oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	kΩ
I_{DD}	HSE current consumption	V_{DD}=3.3 V, ESR= 30 Ω, C_L=5 pF @25 MHz	-	450	-	µA
		V_{DD}=3.3 V, ESR= 30 Ω, C_L=10 pF @25 MHz	-	530	-	
$G_{m\_crit\_max}$	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE)}$(2)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 24*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the

Figure 28 and *Figure 29* show the main PLL output clock waveforms in center spread and down spread modes, where:

F0 is f_{PLL_OUT} nominal.

T_{mode} is the modulation period.

md is the modulation depth.

Figure 28. PLL output clock waveforms in center spread mode

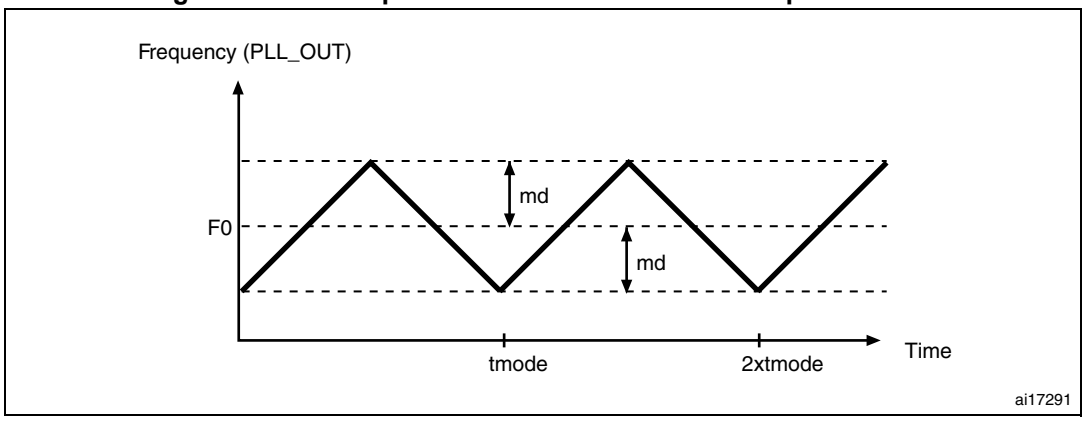
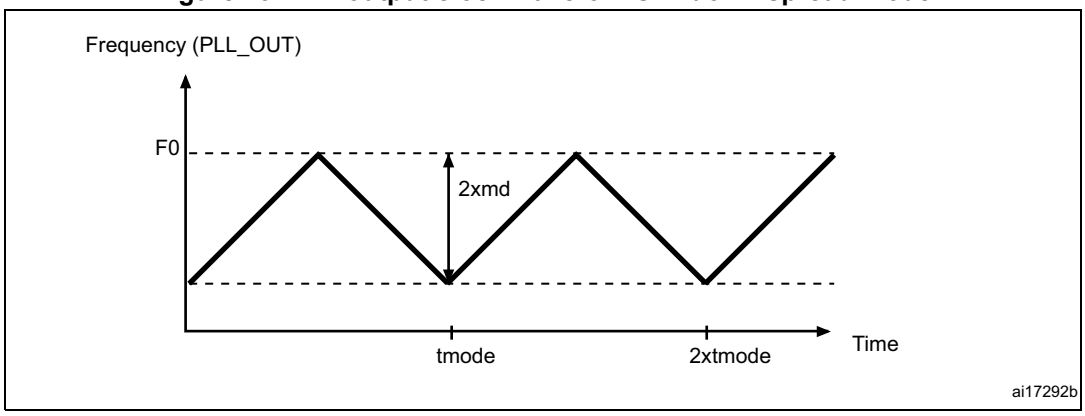


Figure 29. PLL output clock waveforms in down spread mode



6.3.12 Memory characteristics

Flash memory

The characteristics are given at T_A = –40 to 105 °C unless otherwise specified.

The devices are shipped to customers with the Flash memory erased.

Table 44. Flash memory characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current	Write / Erase 8-bit mode, V_{DD} = 1.7 V	-	5	-	mA
		Write / Erase 16-bit mode, V_{DD} = 2.1 V	-	8	-	
		Write / Erase 32-bit mode, V_{DD} = 3.3 V	-	12	-	

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics for WLCSP49

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/84 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, conforming to IEC61967-2	0.1 to 30 MHz	-6	dBµV
			30 to 130 MHz	-6	
			130 MHz to 1 GHz	-10	
			SAE EMI Level	1.5	-

Table 50. EMI characteristics for LQFP100

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/84 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, conforming to IEC61967-2	0.1 to 30 MHz	18	dBµV
			30 to 130 MHz	23	
			130 MHz to 1 GHz	12	
			SAE EMI Level	3.5	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

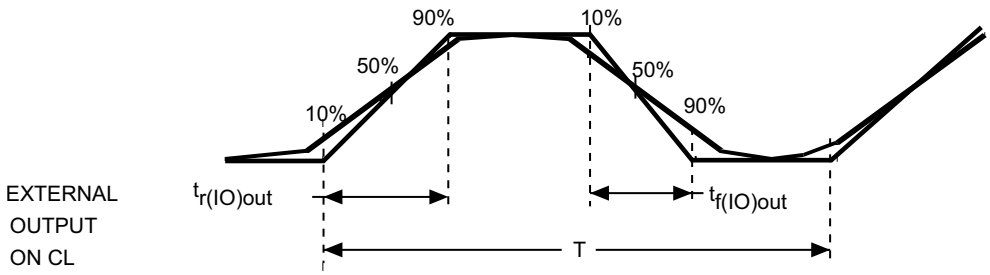
Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Table 56. I/O AC characteristics[1][2] (continued)

OSPEEDRy [1:0] bit value[1]	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
01	$f_{max(IO)out}$	Maximum frequency[3]	C_L = 50 pF, V_{DD} ≥ 2.70 V	-	-	25	MHz
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	12.5	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	50	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	20	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 50 pF, V_{DD} ≥2.7 V	-	-	10	ns
			C_L = 50 pF, V_{DD} ≥ 1.7 V	-	-	20	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	6	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	10	
10	$f_{max(IO)out}$	Maximum frequency[3]	C_L = 40 pF, V_{DD} ≥ 2.70 V	-	-	50[4]	MHz
			C_L = 40 pF, V_{DD} ≥ 1.7 V	-	-	25	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	100[4]	
			C_L = 10 pF, V_{DD} ≥ 1.7 V	-	-	50[4]	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 40 pF, V_{DD}≥ 2.70 V	-	-	6	ns
			C_L = 40 pF, V_{DD}≥ 1.7 V	-	-	10	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	4	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	6	
11	$F_{max(IO)out}$	Maximum frequency[3]	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	100[4]	MHz
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	50[4]	
			C_L = 10 pF, V_{DD} ≥ 2.70 V	-	-	180[4]	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	100[4]	
	$t_{f(IO)out}$/ $t_{r(IO)out}$	Output high to low level fall time and output low to high level rise time	C_L = 30 pF, V_{DD} ≥ 2.70 V	-	-	4	ns
			C_L = 30 pF, V_{DD} ≥ 1.7 V	-	-	6	
			C_L = 10 pF, V_{DD}≥ 2.70 V	-	-	2.5	
			C_L = 10 pF, V_{DD}≥ 1.7 V	-	-	4	
-	t_{EXTIpw}	Pulse width of external signals detected by the EXTI controller		10	-	-	ns

1. Guaranteed by characterization.
2. The I/O speed is configured using the OSPEEDRy[1:0] bits. Refer to the STM32F4xx reference manual for a description of the GPIOx_SPEEDR GPIO port output speed register.
3. The maximum frequency is defined in *Figure 31*.
4. For maximum frequencies above 50 MHz and V_{DD} > 2.4 V, the compensation cell should be used.

Figure 31. I/O AC characteristics definition



Maximum frequency is achieved if (t_r + t_f) ≤ (2/3)T and if the duty cycle is (45-55%) when loaded by CL specified in the table " *I/O AC characteristics*".

ai14131d

6.3.17 NRST pin characteristics

The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see *Table 54*).

Unless otherwise specified, the parameters given in *Table 57* are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in *Table 14*. Refer to *Table 54: I/O static characteristics* for the values of VIH and VIL for NRST pin.

Table 57. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Weak pull-up equivalent resistor(1)	$V_{IN} = V_{SS}$	30	40	50	kΩ
$V_{F(NRST)}$(2)	NRST Input filtered pulse		-	-	100	ns
$V_{NF(NRST)}$(2)	NRST Input not filtered pulse	V_{DD} > 2.7 V	300	-	-	ns
T_{NRST_OUT}	Generated reset pulse duration	Internal Reset source	20	-	-	µs

1. The pull-up is designed with a true resistance in series with a switchable PMOS. This PMOS contribution to the series resistance must be minimum (~10% order).
2. Guaranteed by design.

Table 61. SPI dynamic characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)	-	3	5	ns
$t_{h(MO)}$	Data output hold time	Master mode (after enable edge)	2	-	-	ns

1. Guaranteed by characterization.
2. Maximum frequency in Slave transmitter mode is determined by the sum of $t_{v(SO)}$ and $t_{su(MI)}$ which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having $t_{su(MI)}$ = 0 while Duty(SCK) = 50%

Figure 34. SPI timing diagram - slave mode and CPHA = 0

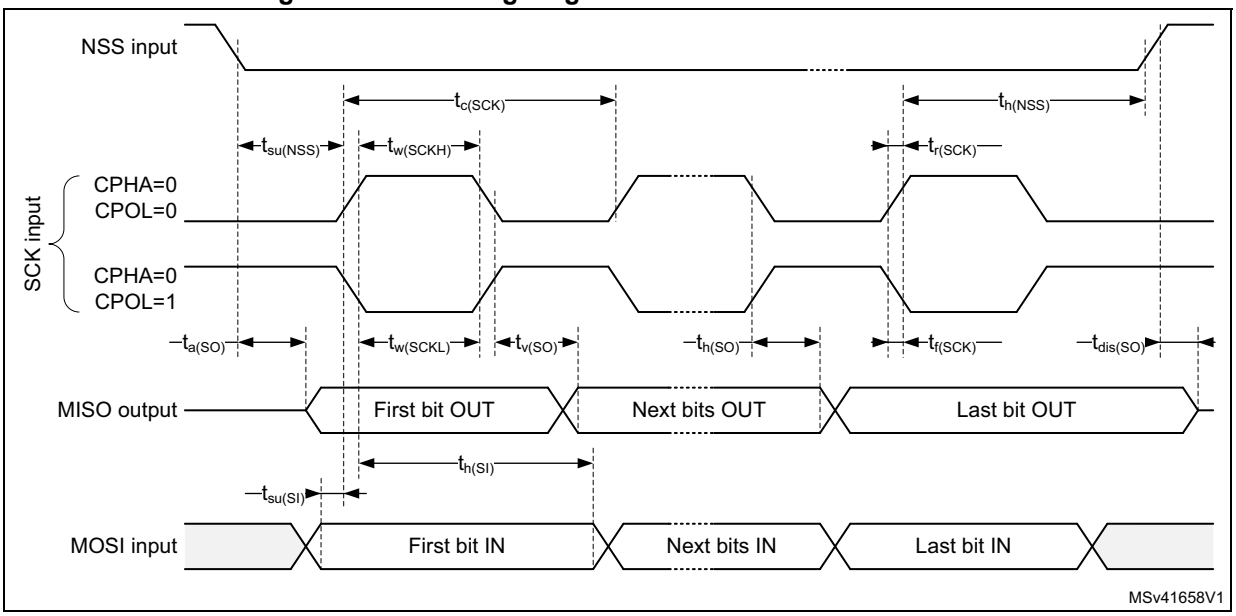
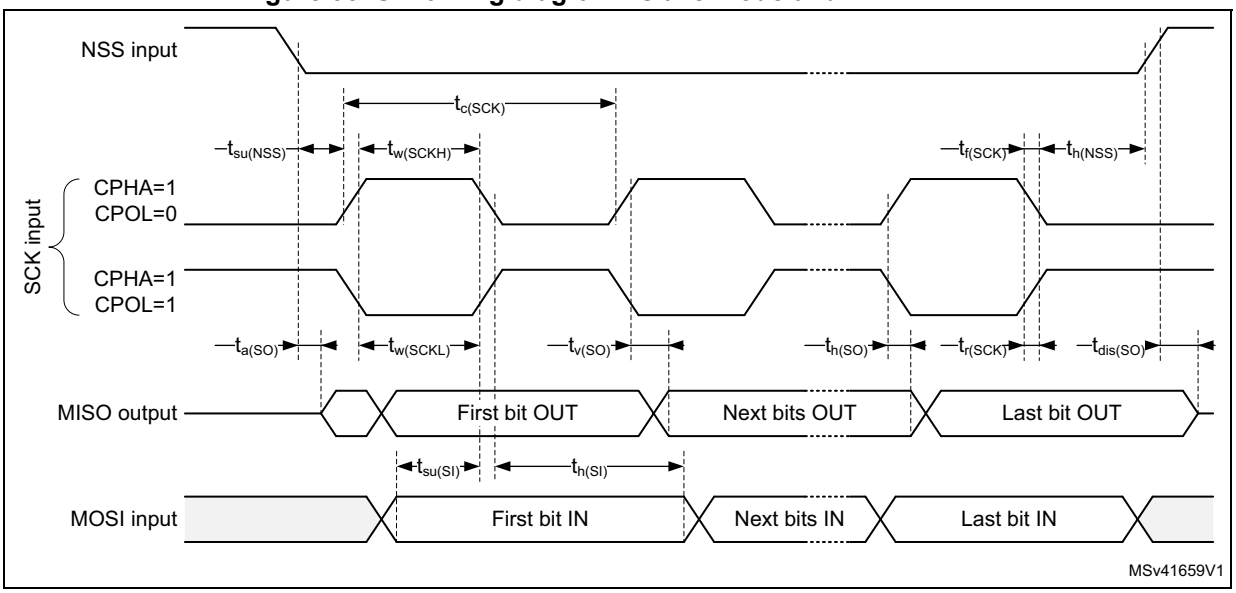


Figure 35. SPI timing diagram - slave mode and CPHA = 1(1)



I²S interface characteristics

Unless otherwise specified, the parameters given in *Table 62* for the I²S interface are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 14*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 10
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5V_{DD}$

Refer to *Section 6.3.16: I/O port characteristics* for more details on the input/output alternate function characteristics (CK, SD, WS).

Table 62. I²S dynamic characteristics(1)

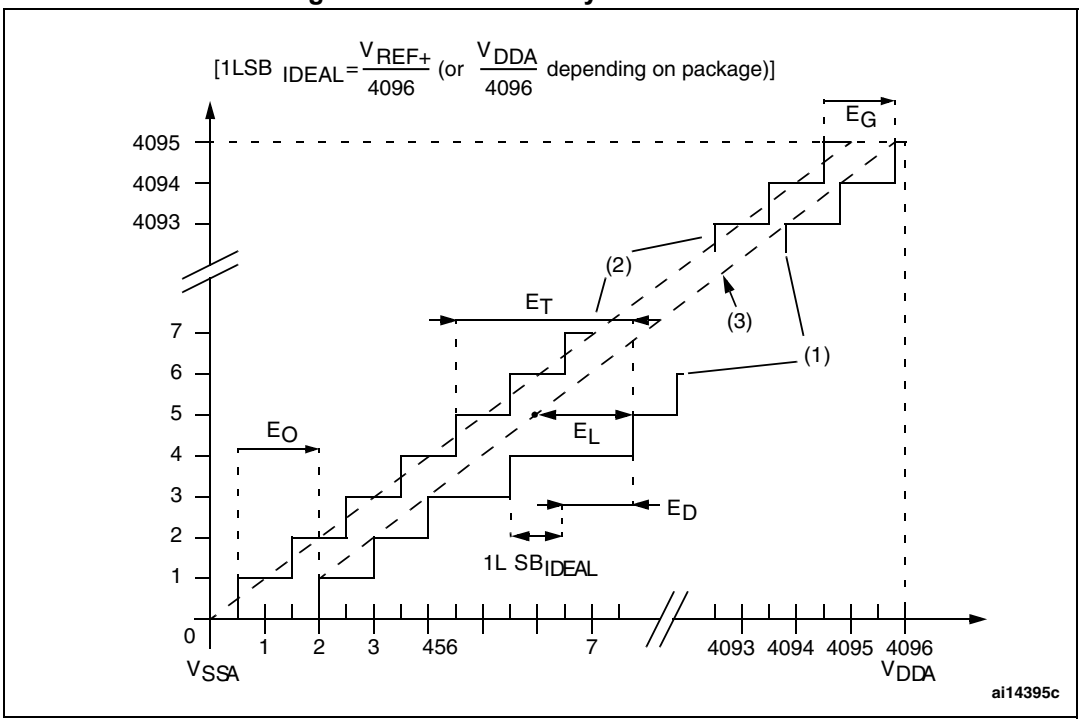
Symbol	Parameter	Conditions	Min	Max	Unit
f_{MCK}	I2S Main clock output	-	256x8K	256xFs(2)	MHz
f_{CK}	I2S clock frequency	Master data: 32 bits	-	64xFs	MHz
		Slave data: 32 bits	-	64xFs	
D_{CK}	I2S clock frequency duty cycle	Slave receiver	30	70	%
$t_{v(WS)}$	WS valid time	Master mode	0	6	ns
$t_{h(WS)}$	WS hold time	Master mode	0	-	
$t_{su(WS)}$	WS setup time	Slave mode	1	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	7.5	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0	-	
$t_{h(SD\_SR)}$		Slave receiver	0	-	
$t_{v(SD\_ST)}$ $t_{h(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	27	
$t_{v(SD\_MT)}$		Master transmitter (after enable edge)	-	20	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	2.5	-	

1. Guaranteed by characterization.
2. The maximum value of 256xFs is 42 MHz (APB1 maximum frequency).

Note: Refer to the I2S section of the reference manual for more details on the sampling frequency (F_S).

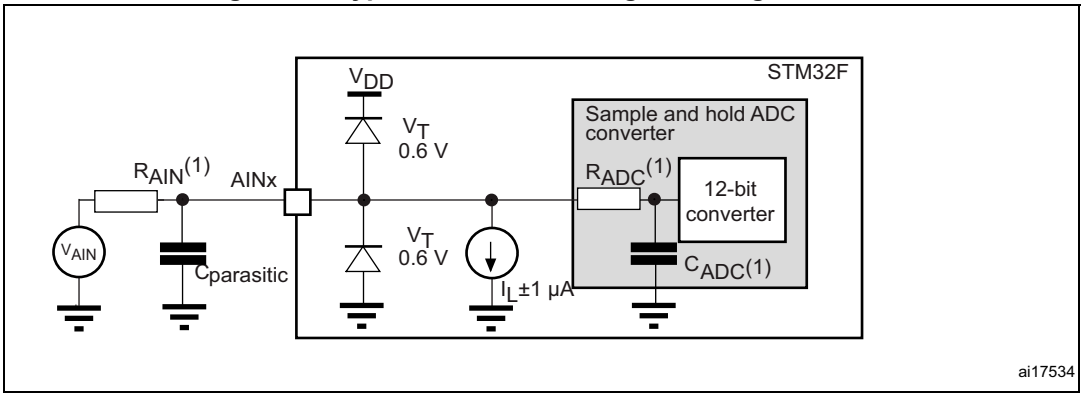
*f_{MCK}, f_{CK}, and D_{CK} values reflect only the digital peripheral behavior. The values of these parameters might be slightly impacted by the source clock precision. D_{CK} depends mainly on the value of ODD bit. The digital contribution leads to a minimum value of (I2SDIV/(2*I2SDIV+ODD) and a maximum value of (I2SDIV+ODD)/(2*I2SDIV+ODD). F_S maximum value is supported for each mode/condition.*

Figure 40. ADC accuracy characteristics



1. See also *Table 68*.
2. Example of an actual transfer curve.
3. Ideal transfer curve.
4. End point correlation line.
5. E_T = Total Unadjusted Error: maximum deviation between the actual and the ideal transfer curves.
   EO = Offset Error: deviation between the first actual transition and the first ideal one.
   EG = Gain Error: deviation between the last ideal transition and the last actual one.
   ED = Differential Linearity Error: maximum deviation between actual steps and the ideal one.
   EL = Integral Linearity Error: maximum deviation between any actual transition and the end point correlation line.

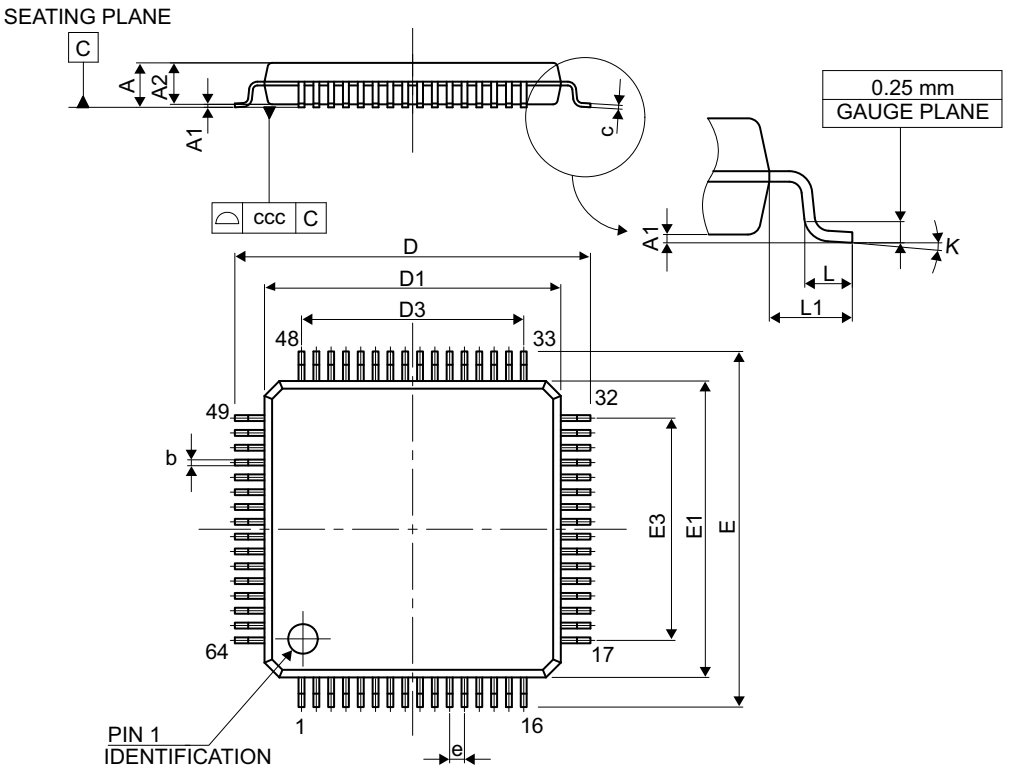
Figure 41. Typical connection diagram using the ADC



1. Refer to *Table 66* for the values of R_{AIN}, R_{ADC} and C_{ADC}.
2. $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 5 pF). A high $C_{parasitic}$ value downgrades conversion accuracy. To remedy this, f_{ADC} should be reduced.

7.3 LQFP64 package information

Figure 52. LQFP64 - 64-pin, 10 x 10 mm, 64-pin low-profile quad flat package outline



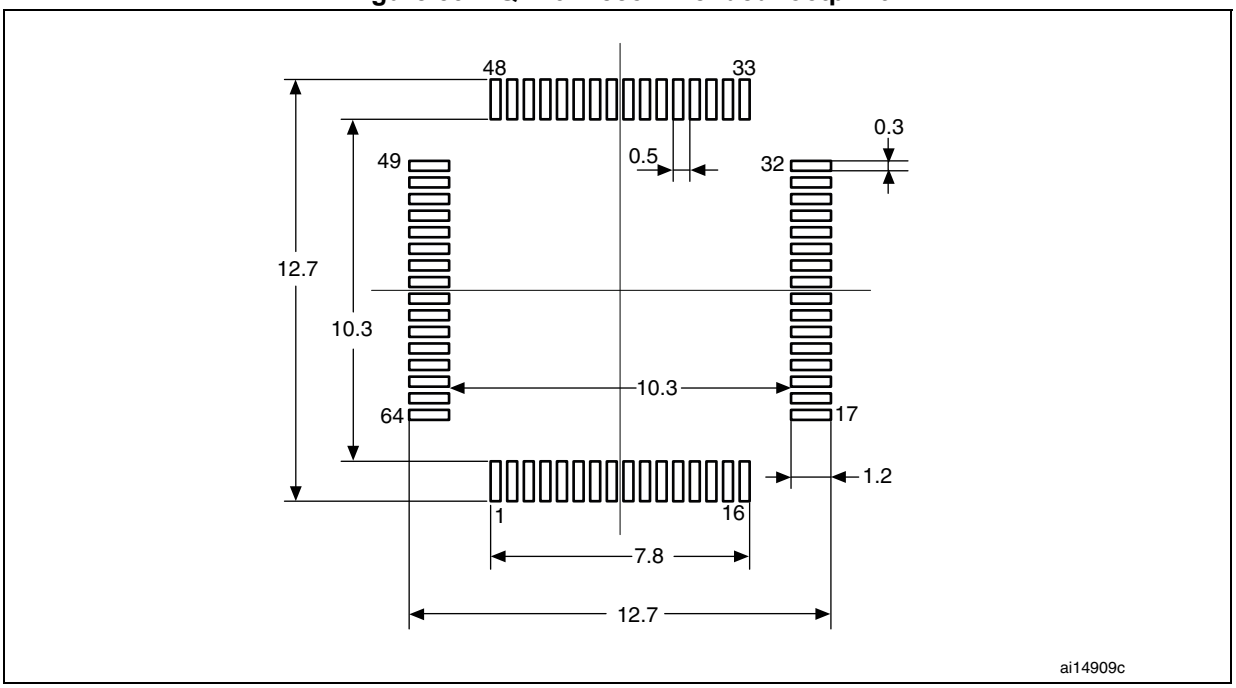
1. Drawing is not to scale.

Table 82. LQFP64 - 64-pin, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-
E3	-	7.5000	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

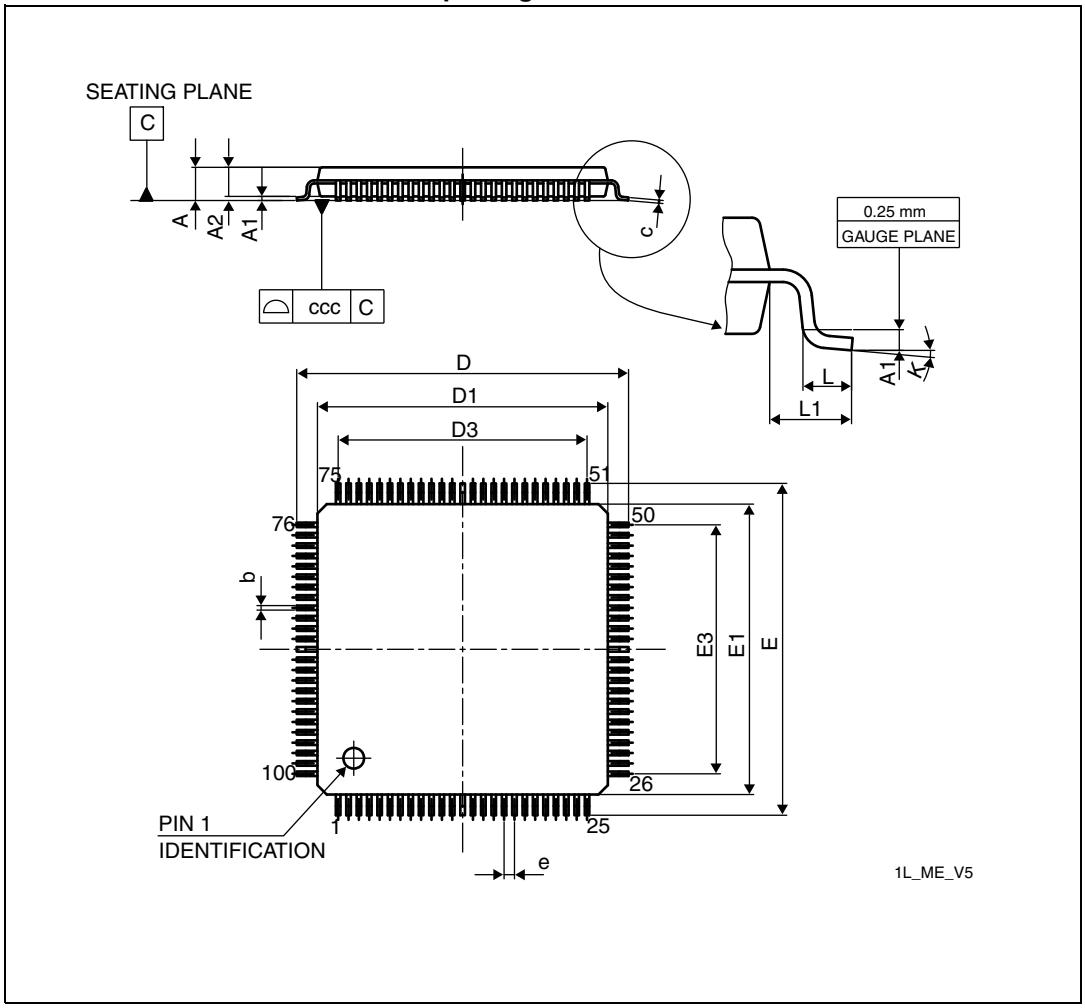
Figure 53. LQFP64 recommended footprint



1. Dimensions are in millimeters.

7.4 LQFP100 package information

Figure 55. LQFP100 - 100-pin, 14 x 14 mm, 100-pin low-profile quad flat package outline



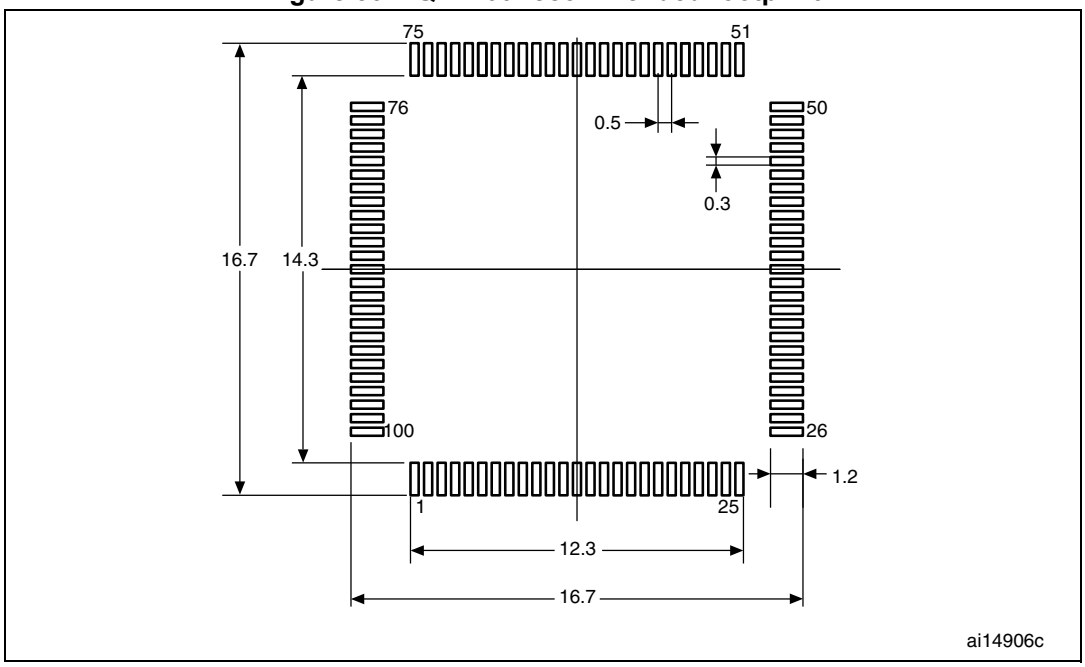
1. Drawing is not to scale.

Table 83. LQPF100- 100-pin, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	-	-	1.60	-	-	0.063
A1	0.050	-	0.150	0.002	-	0.0059
A2	1.350	1.40	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.622	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.622	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
K	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	0.080			0.0031		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 56. LQFP100 recommended footprint



1. Dimensions are in millimeters.