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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	I²C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401rct6tr

List of tables

Table 1. Device summary . . . 1
Table 2. STM32F401xB/C features and peripheral counts . . . 11
Table 3. Regulator ON/OFF and internal power supply supervisor availability . . . 24
Table 4. Timer feature comparison . . . 26
Table 5. Comparison of I2C analog and digital filters . . . 28
Table 6. USART feature comparison . . . 29
Table 7. Legend/abbreviations used in the pinout table . . . 37
Table 8. STM32F401xB/STM32F401xC pin definitions . . . 37
Table 9. Alternate function mapping . . . 44
Table 10. STM32F401xB/STM32F401xC register boundary addresses . . . 51
Table 11. Voltage characteristics . . . 57
Table 12. Current characteristics . . . 58
Table 13. Thermal characteristics . . . 58
Table 14. General operating conditions . . . 59
Table 15. Features depending on the operating power supply range . . . 60
Table 16. VCAP_1/VCAP_2 operating conditions . . . 61
Table 17. Operating conditions at power-up / power-down (regulator ON) . . . 61
Table 18. Operating conditions at power-up / power-down (regulator OFF) . . . 62
Table 19. Embedded reset and power control block characteristics . . . 62
Table 20. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM - V_{DD} =1.8V . . . 64
Table 21. Typical and maximum current consumption, code with data processing (ART accelerator disabled) running from SRAM . . . 65
Table 22. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory- V_{DD} = 1.8 V . . . 65
Table 23. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled except prefetch) running from Flash memory - V_{DD} = 3.3 V . . . 66
Table 24. Typical and maximum current consumption in run mode, code with data processing (ART accelerator disabled) running from Flash memory . . . 66
Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory . . . 67
Table 26. Typical and maximum current consumption in Sleep mode . . . 67
Table 27. Typical and maximum current consumptions in Stop mode - V_{DD}=1.8 V . . . 68
Table 28. Typical and maximum current consumption in Stop mode - V_{DD}=3.3 V . . . 68
Table 29. Typical and maximum current consumption in Standby mode - V_{DD}=1.8 V . . . 68
Table 30. Typical and maximum current consumption in Standby mode - V_{DD}=3.3 V . . . 69
Table 31. Typical and maximum current consumptions in V_{BAT} mode . . . 69
Table 32. Switching output I/O current consumption . . . 71
Table 33. Peripheral current consumption . . . 72
Table 34. Low-power mode wakeup timings(1) . . . 73
Table 35. High-speed external user clock characteristics . . . 74
Table 36. Low-speed external user clock characteristics . . . 75
Table 37. HSE 4-26 MHz oscillator characteristics . . . 76
Table 38. LSE oscillator characteristics (f_{LSE} = 32.768 kHz) . . . 77
Table 39. HSI oscillator characteristics . . . 78
Table 40. LSI oscillator characteristics . . . 79
Table 41. Main PLL characteristics . . . 80

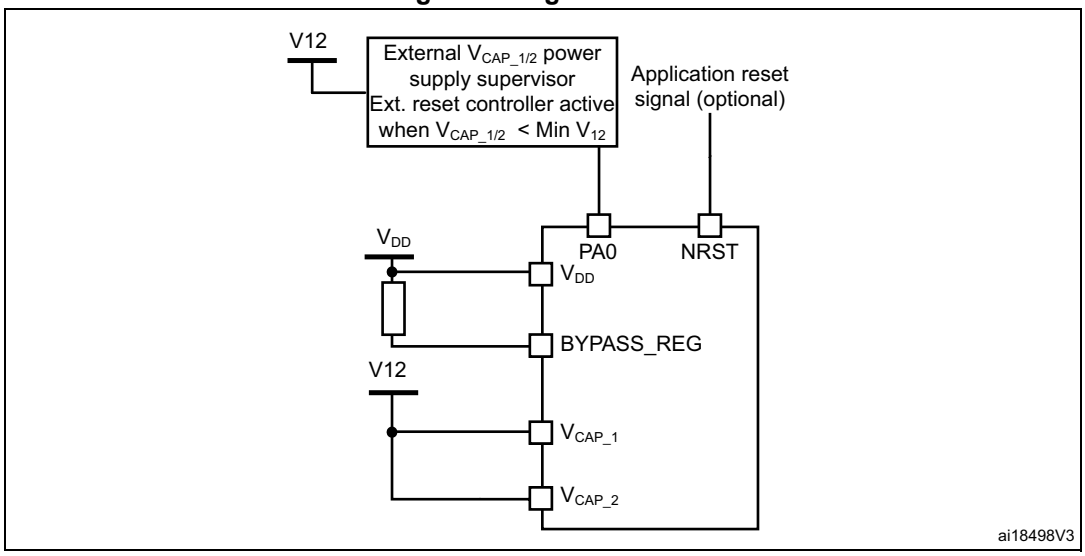
1 Introduction

This datasheet provides the description of the STM32F401xB/STM32F401xC line of microcontrollers.

The STM32F401xB/STM32F401xC datasheet should be read in conjunction with RM0368 reference manual which is available from the STMicroelectronics website *www.st.com*. It includes all information concerning Flash memory programming.

For information on the Cortex®-M4 core, please refer to the Cortex®-M4 programming manual (PM0214) available from *www.st.com*.

Figure 7. Regulator OFF

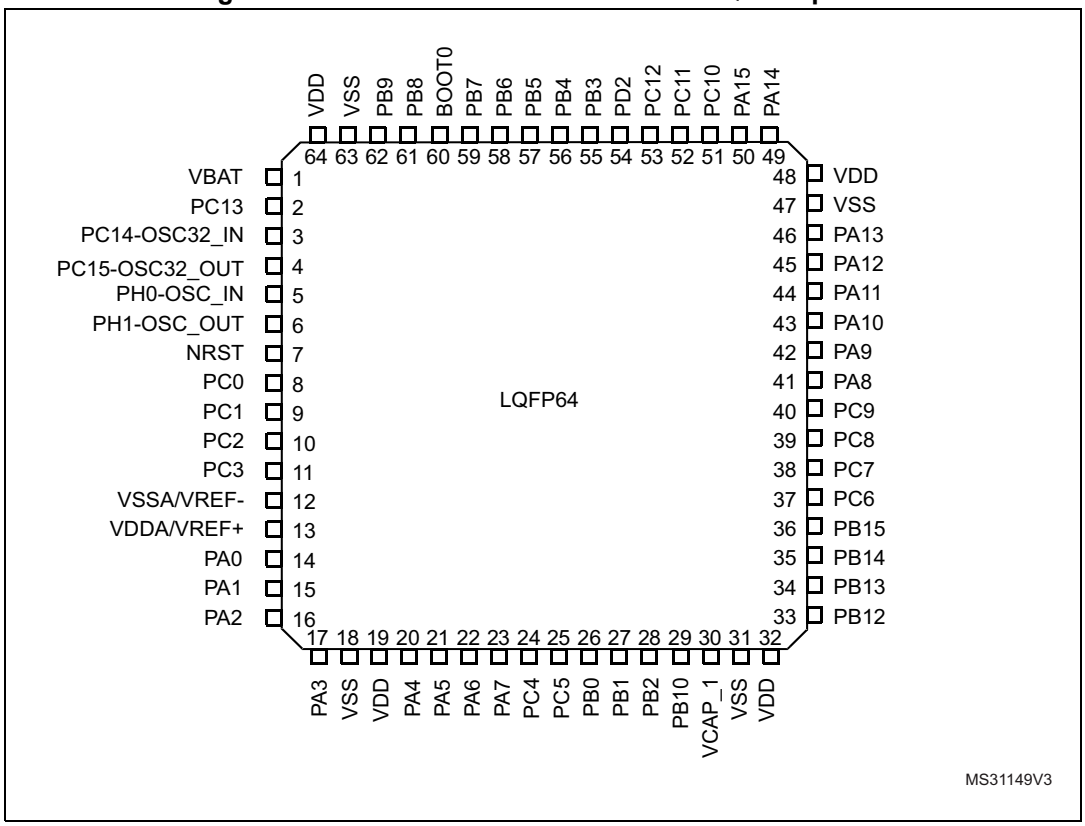


The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.7 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches 1.7 V (see *Figure 8*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.7 V, then PA0 could be asserted low externally (see *Figure 9*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.7 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application

Figure 12. STM32F401xB/STM32F401xC LQFP64 pinout



1. The above figure shows the package top view.

Table 8. STM32F401xB/STM32F401xC pin definitions (continued)

Pin Number					Pin name (function after reset)[1]	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	WLCSP49	LQFP64	LQFP100	UFBGA100						
47	A6	63	99	-	VSS	S	-	-	-	-
-	B6	-	-	H3	PDR_ON	I	FT	-	-	-
48	A7	64	100	-	VDD	S	-	-	-	-

1. Function availability depends on the chosen device.
2. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
   - The speed should not exceed 2 MHz with a maximum load of 30 pF.
   - These I/Os must not be used as a current source (e.g. to drive an LED).
3. Main function after the first backup domain power-up. Later on, it depends on the contents of the RTC registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the RTC register description sections in the STM32F401xx reference manual.
4. FT = 5 V tolerant except when in analog mode or oscillator mode (for PC14, PC15, PH0 and PH1).
5. If the device is delivered in an UFBGA100 and the BYPASS_REG pin is set to VDD (Regulator off/internal reset ON mode), then PA0 is used as an internal Reset (active low)

Table 9. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_FS		SDIO			
Port B	PB0	-	TIM1_CH2N	TIM3_CH3	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB1	-	TIM1_CH3N	TIM3_CH4	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB3	JTDO-SWO	TIM2_CH2	-	-	-	SPI1_SCK	SPI3_SCK/ I2S3_CK	-	-	I2C2_SDA	-	-	-	-	-	EVENT OUT
	PB4	JTRST	-	TIM3_CH1	-	-	SPI1_ MISO	SPI3_MISO	I2S3ext_SD	-	I2C3_SDA	-	-	-	-	-	EVENT OUT
	PB5	-	-	TIM3_CH2	-	I2C1_ SMBA	SPI1 _MOSI	SPI3_MOSI/ I2S3_SD	-	-	-	-	-	-	-	-	EVENT OUT
	PB6	-	-	TIM4_CH1	-	I2C1_SCL	-	-	USART1_ TX	-	-	-	-	-	-	-	EVENT OUT
	PB7	-	-	TIM4_CH2	-	I2C1_SDA	-	-	USART1_ RX	-	-	-	-	-	-	-	EVENT OUT
	PB8	-	-	TIM4_CH3	TIM10_CH1	I2C1_SCL	-	-	-	-	-	-	-	SDIO_ D4	-	-	EVENT OUT
	PB9	-	-	TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/I 2S2_WS	-	-	-	-	-	-	SDIO_ D5	-	-	EVENT OUT
	PB10	-	TIM2_CH3	-	-	I2C2_SCL	SPI2_SCK/I 2S2_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB11	-	TIM2_CH4	-	-	I2C2_SDA	-	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB12	-	TIM1_BKIN	-	-	I2C2_ SMBA	SPI2_NSS/I 2S2_WS	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB13	-	TIM1_CH1N	-	-	-	SPI2_SCK/I 2S2_CK	-	-	-	-	-	-	-	-	-	EVENT OUT
	PB14	-	TIM1_CH2N	-	-	-	SPI2_MISO	I2S2ext_SD	-	-	-	-	-	-	-	-	EVENT OUT
	PB15	RTC_ REFN	TIM1_CH3N	-	-	-	SPI2_MOSI /I2S2_SD	-	-	-	-	-	-	-	-	-	EVENT OUT

Table 10. STM32F401xB/STM32F401xC register boundary addresses (continued)

Bus	Boundary address	Peripheral
APB1	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6000 - 0x4000 6FFF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 4800 - 0x4000 53FF	Reserved
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 1000 - 0x4000 27FF	Reserved
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source)(1)	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink)(1)	-160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source)(1)	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink)(1)	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins (2)	120	
	Total output current sourced by sum of all I/Os and control pins(2)	-120	
$I_{INJ(PIN)}$ (3)	Injected current on FT pins (4)	–5/+0	
	Injected current on NRST and B pins (4)		
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(5)	±25	

1. All main power (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in *Section 6.3.20: 12-bit ADC characteristics*.
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	–65 to +150	°C
T_J	Maximum junction temperature	125	
T_{LEAD}	Maximum lead temperature during soldering (WLCSP49, LQFP64/100, UFQFPN48, UFBGA100)	see note (1)	

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

Table 25. Typical and maximum current consumption in run mode, code with data processing (ART accelerator enabled with prefetch) running from Flash memory

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Run mode**	External clock, all peripherals enabled(2)(3)	84	31.8	33	35	36	mA
			60	21.8	22	23	24	
			40	16.0	17	18	19	
			30	12.9	14	15	16	
			20	10.4	11	12	13	
		External clock, all peripherals disabled(3)	84	21.2	22	23	24	
			60	15.0	16	17	18	
			40	10.9	12	13	14	
			30	8.8	10	11	12	
			20	7.1	8	9	10	

1. Guaranteed by characterization, unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2), add an additional power consumption of 1.6mA per ADC for the analog part.

Table 26. Typical and maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK} (MHz)	Typ	Max(1)			Unit
					T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in **Sleep** mode	External clock, all peripherals enabled(2)(3)	84	16.2	17	18	19	mA
			60	10.7	11	12	13	
			40	8.3	9	10	11	
			30	6.8	7	8	9	
			20	5.9	6	7	8	
		External clock, all peripherals disabled(3)(4)	84	5.2	6	7	8	
			60	3.6	4	5	6	
			40	2.9	3	4	5	
			30	2.6	3	4	5	
			20	2.6	3	4	5	

1. Guaranteed by characterization, unless otherwise specified.
2. Add an additional power consumption of 1.6 mA per ADC for the analog part. In applications, this consumption occurs only while the ADC is ON (ADON bit is set in the ADC_CR2 register).
3. When the ADC is ON (ADON bit set in the ADC_CR2 register), add an additional power consumption of 1.6 mA for the analog part.
4. Same current consumption for f_{HCLK} at 30 MHz and 20 MHz due to VCO running slower at 30 MHz.

Table 27. Typical and maximum current consumptions in Stop mode - V_{DD}=1.8 V

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Main regulator usage	Flash in Stop mode, all oscillators OFF, no independent watchdog	109	135	440	650	µA
	Low power regulator usage		41	65	310	530(2)	
	Main regulator usage	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	72	95	345	530	
	Low power regulator usage		12	36	260	510(2)	
	Low power low voltage regulator usage		10	27	230	460	

1. Guaranteed by characterization.
2. Guaranteed by test in production.

Table 28. Typical and maximum current consumption in Stop mode - V_{DD}=3.3 V

Symbol	Parameter	Conditions	Typ	Max(1)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STOP}	Main regulator usage	Flash in Stop mode, all oscillators OFF, no independent watchdog	111	140	450	670	µA
	Low power regulator usage		42	65	330	560	
	Main regulator usage	Flash in Deep power down mode, all oscillators OFF, no independent watchdog	73	100	360	560	
	Low power regulator usage		12	36	270	520	
	Low power low voltage regulator usage		10	28	230	470	

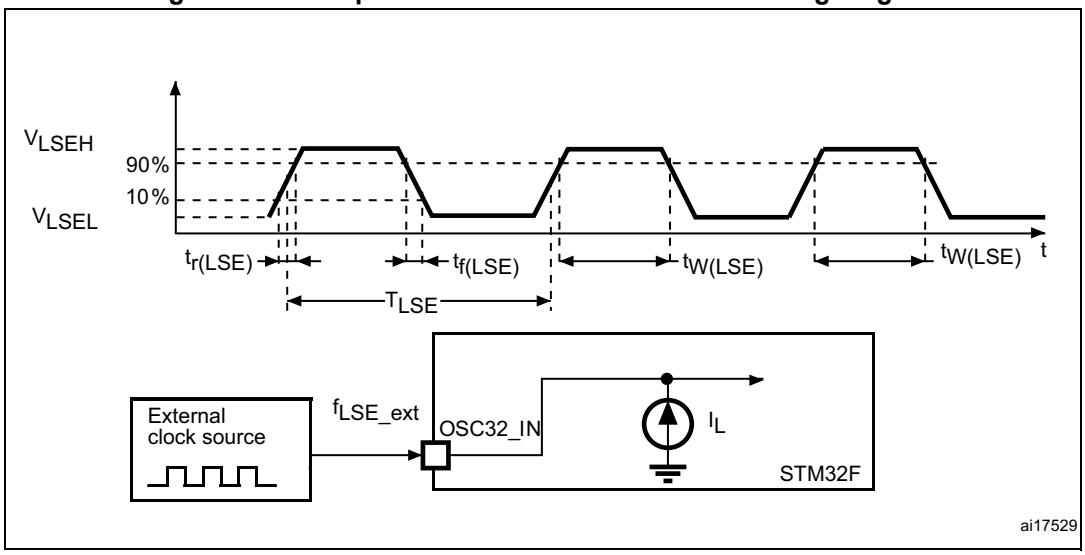
1. Guaranteed by characterization.

Table 29. Typical and maximum current consumption in Standby mode - V_{DD}=1.8 V

Symbol	Parameter	Conditions	Typ(1)	Max(2)			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_STBY}	Supply current in Standby mode	Low-speed oscillator (LSE) and RTC ON	2.4	4.0	12.0	24.0	µA
		RTC and LSE OFF	1.8	3.0(3)	11.0	23.0(3)	

1. When the PDR is OFF (internal reset is OFF), the typical current consumption is reduced by 1.2 µA.
2. Guaranteed by characterization, unless otherwise specified.
3. Guaranteed by test in production.

Figure 23. Low-speed external clock source AC timing diagram



High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 26 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in *Table 37*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

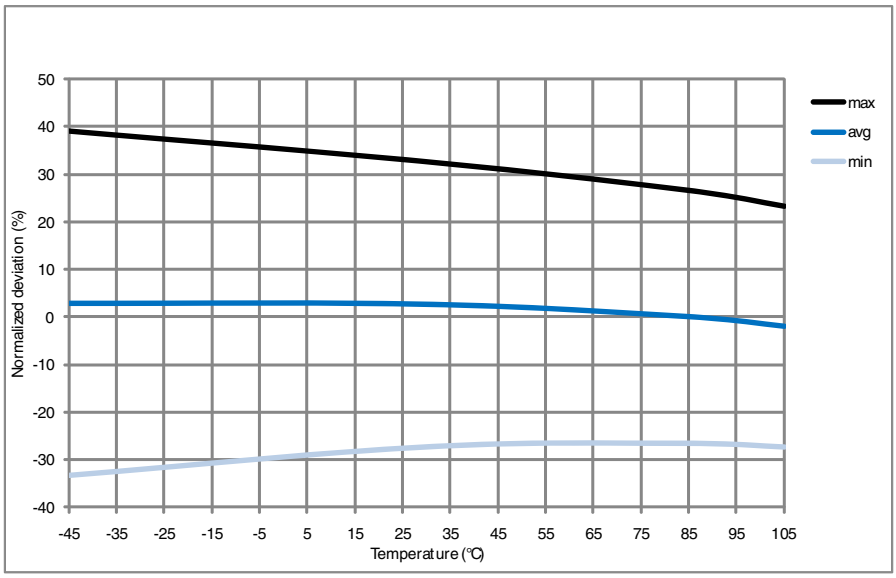
Table 37. HSE 4-26 MHz oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency		4	-	26	MHz
R_F	Feedback resistor		-	200	-	kΩ
I_{DD}	HSE current consumption	V_{DD}=3.3 V, ESR= 30 Ω, C_L=5 pF @25 MHz	-	450	-	µA
		V_{DD}=3.3 V, ESR= 30 Ω, C_L=10 pF @25 MHz	-	530	-	
$G_{m\_crit\_max}$	Maximum critical crystal g_m	Startup	-	-	1	mA/V
$t_{SU(HSE)}$(2)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 24*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the

Figure 27. ACC_{LSI} versus temperature



6.3.10 PLL characteristics

The parameters given in *Table 41* and *Table 42* are derived from tests performed under temperature and V_{DD} supply voltage conditions summarized in *Table 14*.

Table 41. Main PLL characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(1)			0.95(2)	1	2.10	MHz
f_{PLL_OUT}	PLL multiplier output clock			24	-	84	MHz
f_{PLL48_OUT}	48 MHz PLL multiplier output clock			-	48	75	MHz
f_{VCO_OUT}	PLL VCO output			192	-	432	MHz
t_{LOCK}	PLL lock time	VCO freq = 192 MHz		75	-	200	µs
		VCO freq = 432 MHz		100	-	300	
Jitter(3)	Cycle-to-cycle jitter	System clock 84 MHz	RMS	-	25	-	ps
			peak to peak	-	±150	-	
	Period Jitter		RMS	-	15	-	
			peak to peak	-	±200	-	

Table 48. EMS characteristics for LQFP100 package

Symbol	Parameter	Conditions	Level/ Class
V_{FESD}	Voltage limits to be applied on any I/O pin to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, WLCSP49, T_A = +25 °C, f_{HCLK} = 84 MHz, conforms to IEC 61000-4-2	2B
V_{EFTB}	Fast transient voltage burst limits to be applied through 100 pF on V_{DD} and V_{SS} pins to induce a functional disturbance	V_{DD} = 3.3 V, LQFP100, WLCSP49, T_A = +25 °C, f_{HCLK} = 84 MHz, conforms to IEC 61000-4-4	4A

When the application is exposed to a noisy environment, it is recommended to avoid pin exposition to disturbances. The pins showing a middle range robustness are: PA0, PA1, PA2, on LQFP100 packages and PDR_ON on WLCSP49.

As a consequence, it is recommended to add a serial resistor (1 kΩ maximum) located as close as possible to the MCU to the pins exposed to noise (connected to tracks longer than 50 mm on PCB).

Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

Software recommendations

The software flowchart must include the management of runaway conditions such as:

- Corrupted program counter
- Unexpected reset
- Critical Data corruption (control registers...)

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application, executing EEMBC code, is running. This emission test is compliant with SAE IEC61967-2 standard which specifies the test board and the pin loading.

Table 49. EMI characteristics for WLCSP49

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/84 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, conforming to IEC61967-2	0.1 to 30 MHz	-6	dBµV
			30 to 130 MHz	-6	
			130 MHz to 1 GHz	-10	
			SAE EMI Level	1.5	-

Table 50. EMI characteristics for LQFP100

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{CPU}]	Unit
				25/84 MHz	
S_{EMI}	Peak level	V_{DD} = 3.3 V, T_A = 25 °C, conforming to IEC61967-2	0.1 to 30 MHz	18	dBµV
			30 to 130 MHz	23	
			130 MHz to 1 GHz	12	
			SAE EMI Level	3.5	-

6.3.14 Absolute maximum ratings (electrical sensitivity)

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the JESD22-A114/C101 standard.

Figure 39. USB OTG FS timings: definition of data signal rise and fall time

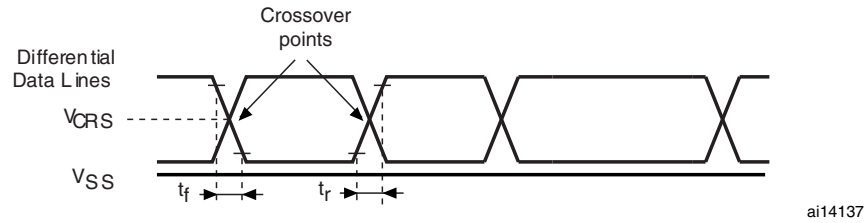


Table 65. USB OTG FS electrical characteristics(1)

Driver characteristics					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
t_r	Rise time(2)	C_L = 50 pF	4	20	ns
t_f	Fall time(2)	C_L = 50 pF	4	20	ns
t_{rfm}	Rise/ fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage		1.3	2.0	V

1. Guaranteed by design.
2. Measured from 10% to 90% of the data signal. For more detailed informations, please refer to USB Specification - Chapter 7 (version 2.0).

6.3.20 12-bit ADC characteristics

Unless otherwise specified, the parameters given in *Table 66* are derived from tests performed under the ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 14*.

Table 66. ADC characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Power supply	$V_{DDA} - V_{REF+} < 1.2$ V	1.7(1)	-	3.6	V
V_{REF+}	Positive reference voltage		1.7(1)	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-	-	0	-	
f_{ADC}	ADC clock frequency	V_{DDA} = 1.7(1) to 2.4 V	0.6	15	18	MHz
		V_{DDA} = 2.4 to 3.6 V	0.6	30	36	MHz
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 30 MHz, 12-bit resolution	-	-	1764	kHz
			-	-	17	$1/f_{ADC}$
V_{AIN}	Conversion voltage range(3)		0 (V_{SSA} or V_{REF-} tied to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	See *Equation 1* for details	-	-	50	kΩ
R_{ADC}(2)(4)	Sampling switch resistance		-	-	6	kΩ
C_{ADC}(2)	Internal sample and hold capacitor		-	4	7	pF

Equation 1: R_{AIN} max formula

$$R_{AIN} = \frac{(k - 0.5)}{f_{ADC} \times C_{ADC} \times \ln(2^{N+2})} - R_{ADC}$$

The formula above (*Equation 1*) is used to determine the maximum external impedance allowed for an error below 1/4 of LSB. N = 12 (from 12-bit resolution) and k is the number of sampling periods defined in the ADC_SMPR1 register.

Table 67. ADC accuracy at f_{ADC} = 18 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =18 MHz V_{DDA} = 1.7 to 3.6 V V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±3	±4	LSB
EO	Offset error		±2	±3	
EG	Gain error		±1	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±2	±3	

1. Guaranteed by characterization.

Table 68. ADC accuracy at f_{ADC} = 30 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} = 30 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V, $V_{DDA} - V_{REF}$ < 1.2 V	±2	±5	LSB
EO	Offset error		±1.5	±2.5	
EG	Gain error		±1.5	±3	
ED	Differential linearity error		±1	±2	
EL	Integral linearity error		±1.5	±3	

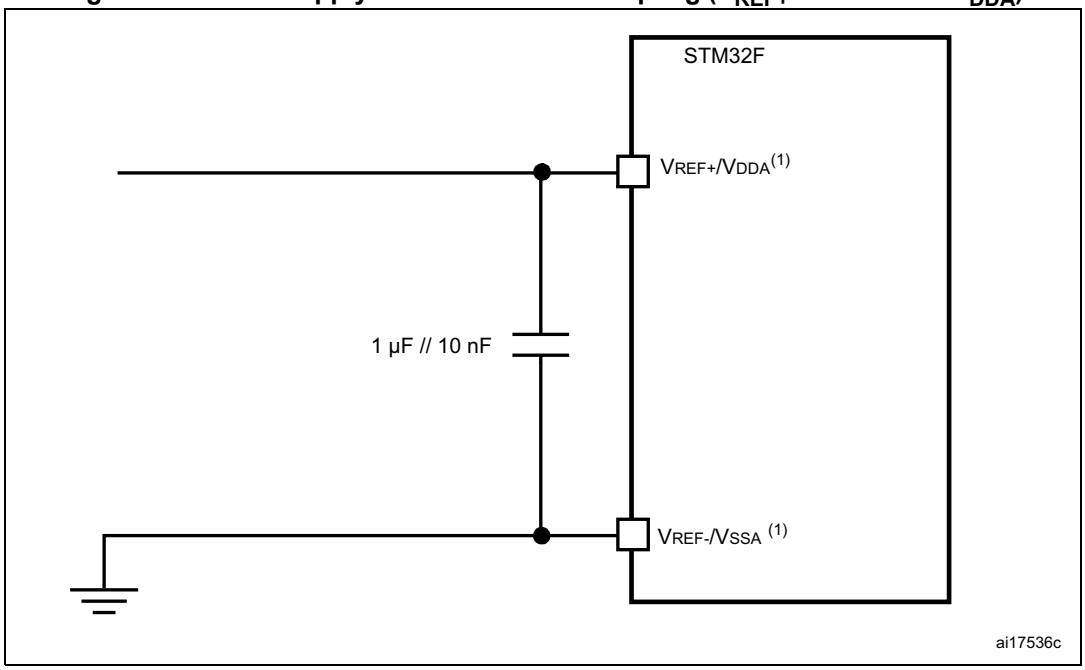
1. Guaranteed by characterization.

Table 69. ADC accuracy at f_{ADC} = 36 MHz

Symbol	Parameter	Test conditions	Typ	Max(1)	Unit
ET	Total unadjusted error	f_{ADC} =36 MHz, V_{DDA} = 2.4 to 3.6 V, V_{REF} = 1.7 to 3.6 V $V_{DDA} - V_{REF}$ < 1.2 V	±4	±7	LSB
EO	Offset error		±2	±3	
EG	Gain error		±3	±6	
ED	Differential linearity error		±2	±3	
EL	Integral linearity error		±3	±6	

1. Guaranteed by characterization.

Figure 43. Power supply and reference decoupling (V_{REF+} connected to V_{DDA})



1. V_{REF+} and V_{REF-} inputs are both available on UFBGA100. V_{REF+} is also available on LQFP100. When V_{REF+} and V_{REF-} are not available, they are internally connected to V_{DDA} and V_{SSA}.

6.3.21 Temperature sensor characteristics

Table 72. Temperature sensor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L(1)	V_{SENSE} linearity with temperature	-	±1	±2	°C
Avg_Slope(1)	Average slope	-	2.5	-	mV/°C
V_{25}(1)	Voltage at 25 °C	-	0.76	-	V
t_{START}(2)	Startup time	-	6	10	µs
T_{S_temp}(2)	ADC sampling time when reading the temperature (1 °C accuracy)	10	-	-	µs

1. Guaranteed by characterization.
2. Guaranteed by design.

Table 73. Temperature sensor calibration values

Symbol	Parameter	Memory address
TS_CAL1	TS ADC raw data acquired at temperature of 30 °C, V_{DDA}= 3.3 V	0x1FFF 7A2C - 0x1FFF 7A2D
TS_CAL2	TS ADC raw data acquired at temperature of 110 °C, V_{DDA}= 3.3 V	0x1FFF 7A2E - 0x1FFF 7A2F

Table 77. Dynamic characteristics: SD / MMC characteristics(1)(2) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	fpp = 24MHz	1.5	-	-	ns
t_{IHD}	Input hold time SD	fpp = 24MHz	0.5	-	-	
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	fpp =24MHz	-	4.5	6.5	ns
t_{OHD}	Output hold default time SD	fpp =24MHz	3.5	-	-	

1. Guaranteed by characterization results.
2. V_{DD} = 2.7 to 3.6 V.

6.3.25 RTC characteristics

Table 78. RTC characteristics

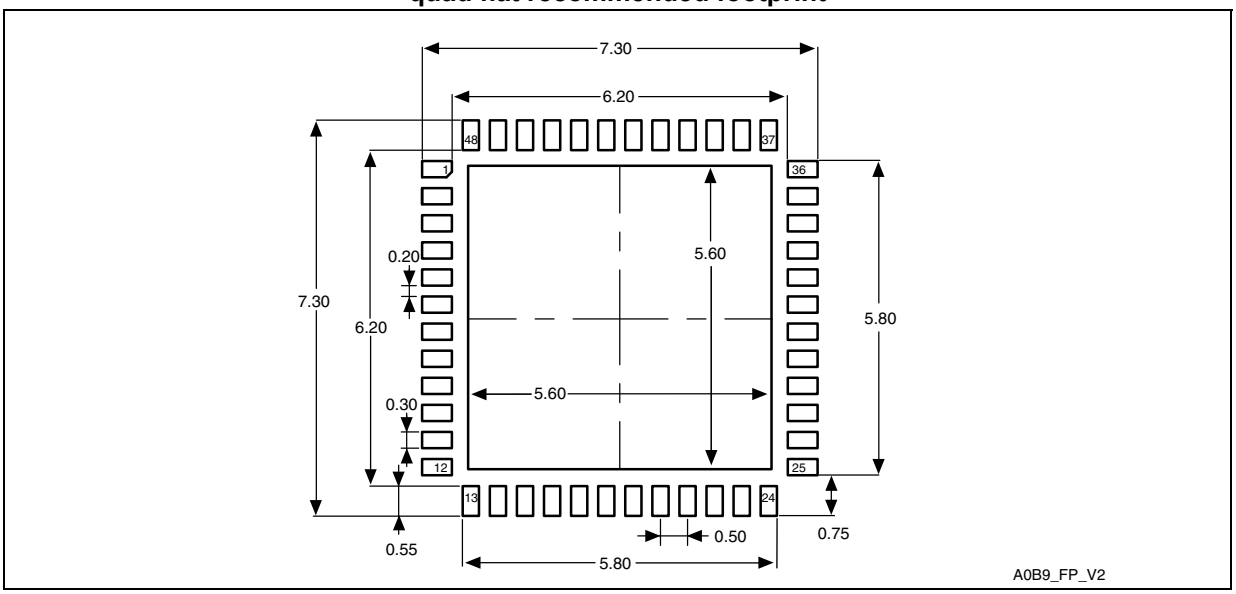
Symbol	Parameter	Conditions	Min	Max
-	f_{PCLK1}/RTCCLK frequency ratio	Any read/write operation from/to an RTC register	4	-

Table 81. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 50. UFQFPN48 - 48-lead, 7 x 7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat recommended footprint



1. Dimensions are in millimeters.