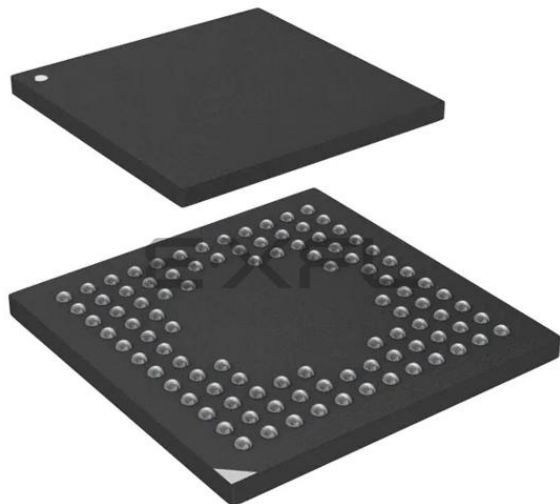




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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	84MHz
Connectivity	I ² C, IrDA, LINbus, SDIO, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.7V ~ 3.6V
Data Converters	A/D 16x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-UFBGA
Supplier Device Package	100-UFBGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32f401vbh6

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1 Introduction

This datasheet provides the description of the STM32F401xB/STM32F401xC line of microcontrollers.

The STM32F401xB/STM32F401xC datasheet should be read in conjunction with RM0368 reference manual which is available from the STMicroelectronics website www.st.com. It includes all information concerning Flash memory programming.

For information on the Cortex[®]-M4 core, please refer to the Cortex[®]-M4 programming manual (PM0214) available from www.st.com.



Table 2. STM32F401xB/C features and peripheral counts

Peripherals		STM32F401xB			STM32F401xC		
Flash memory in Kbytes		128			256		
SRAM in Kbytes	System	64					
Timers	General-purpose	7					
	Advanced-control	1					
Communication interfaces	SPI/ I ² S	3/2 (full duplex)		4/2 (full duplex)	3/2 (full duplex)		4/2 (full duplex)
	I ² C	3					
	USART	3					
	SDIO	-	1		-	1	
USB OTG FS		1					
GPIOs		36	50	81	36	50	81
12-bit ADC		1					
Number of channels		10	16		10	16	
Maximum CPU frequency		84 MHz					
Operating voltage		1.7 to 3.6 V					
Operating temperatures		Ambient temperatures: −40 to +85 °C/−40 to +105 °C					
		Junction temperature: −40 to + 125 °C					
Package		WLCSP49 UFQFPN48	LQFP64	UFBGA100 LQFP100	WLCSP49 UFQFPN48	LQFP64	UFBGA100 LQFP100

3.15.1 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)
In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.
- LPR is used in the Stop modes
The LP regulator mode is configured by software when entering Stop mode.
- Power-down is used in Standby mode.
The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost.

Depending on the package, one or two external ceramic capacitors should be connected on the V_{CAP_1} and V_{CAP_2} pins. The V_{CAP_2} pin is only available for the LQFP100 and UFBGA100 packages.

All packages have the regulator ON feature.

3.15.2 Regulator OFF

The Regulator OFF is available only on the UFBGA100, which features the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency. Refer to [Table 14: General operating conditions](#).

The two 2.2 μ F V_{CAP} ceramic capacitors should be replaced by two 100 nF decoupling capacitors. Refer to [Figure 18: Power supply scheme](#).

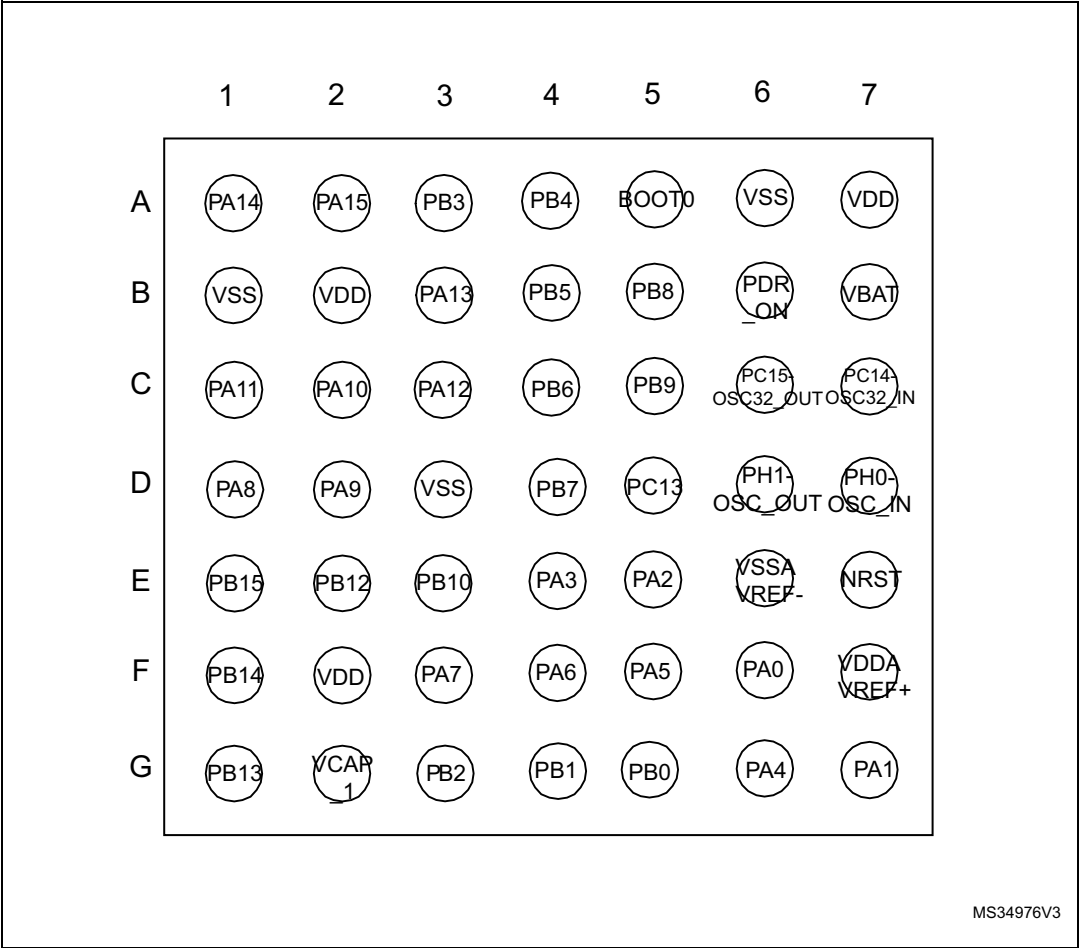
When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V12 logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

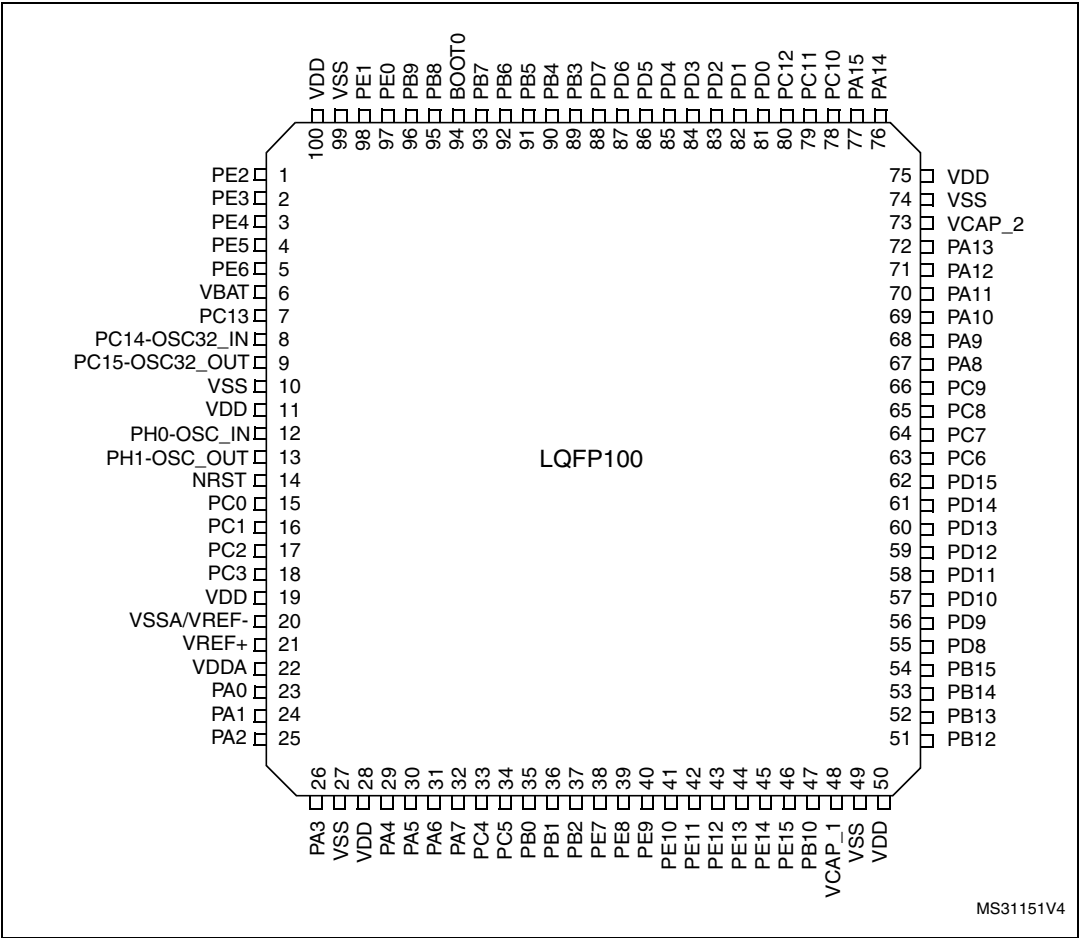
4 Pinouts and pin description

Figure 10. STM32F401xB/STM32F401xC WLCSP49 pinout



1. The above figure shows the package top view.

Figure 13. STM32F401xB/STM32F401xC LQFP100 pinout



1. The above figure shows the package top view.

Table 7. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name	Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name	
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes	Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset	
Alternate functions	Functions selected through GPIOx_AFR registers	
Additional functions	Functions directly selected/enabled through peripheral registers	

Table 8. STM32F401xB/STM32F401xC pin definitions

Pin Number					Pin name (function after reset) ⁽¹⁾	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	WLCSP49	LQFP64	LQFP100	UFBGA100						
-	-	-	1	B2	PE2	I/O	FT	-	SPI4_SCK, TRACECLK, EVENTOUT	-
-	-	-	2	A1	PE3	I/O	FT	-	TRACED0, EVENTOUT	-
-	-	-	3	B1	PE4	I/O	FT	-	SPI4_NSS, TRACED1, EVENTOUT	-
-	-	-	4	C2	PE5	I/O	FT	-	SPI4_MISO, TIM9_CH1, TRACED2, EVENTOUT	-
-	-	-	5	D2	PE6	I/O	FT	-	SPI4_MOSI, TIM9_CH2, TRACED3, EVENTOUT	-
-	-	-	-	D3	VSS	S	-	-	-	-
-	-	-	-	C4	VDD	S	-	-	-	-
1	B7	1	6	E2	VBAT	S	-	-	-	-
2	D5	2	7	C1	PC13	I/O	FT	(2) (3)	EVENTOUT,	RTC_TAMP1, RTC_OUT, RTC_TS

**Table 10. STM32F401xB/STM32F401xC
register boundary addresses**

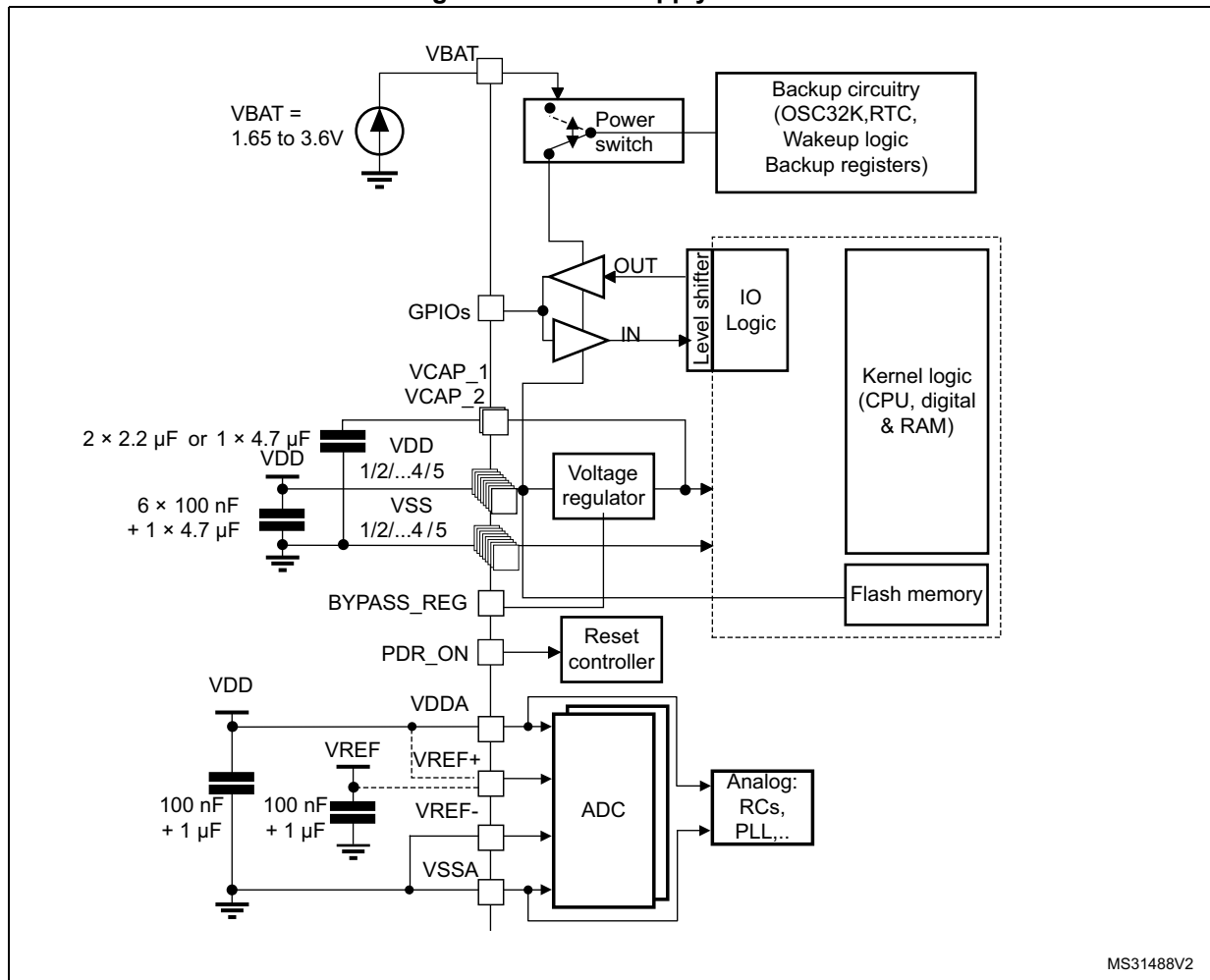
Bus	Boundary address	Peripheral
	0xE010 0000 - 0xFFFF FFFF	Reserved
Cortex [®] -M4	0xE000 0000 - 0xE00F FFFF	Cortex-M4 internal peripherals
	0x5004 0000 - 0xDFFF FFFF	Reserved
AHB2	0x5000 0000 - 0x5003 FFFF	USB OTG FS
AHB1	0x4002 6800 - 0x4FFF FFFF	Reserved
	0x4002 6400 - 0x4002 67FF	DMA2
	0x4002 6000 - 0x4002 63FF	DMA1
	0x4002 5000 - 0x4002 4FFF	Reserved
	0x4002 3C00 - 0x4002 3FFF	Flash interface register
	0x4002 3800 - 0x4002 3BFF	RCC
	0x4002 3400 - 0x4002 37FF	Reserved
	0x4002 3000 - 0x4002 33FF	CRC
	0x4002 2000 - 0x4002 2FFF	Reserved
	0x4002 1C00 - 0x4002 1FFF	GPIOH
	0x4002 1400 - 0x4002 1BFF	Reserved
	0x4002 1000 - 0x4002 13FF	GPIOE
	0x4002 0C00 - 0x4002 0FFF	GIPOD
	0x4002 0800 - 0x4002 0BFF	GPIOC
	0x4002 0400 - 0x4002 07FF	GPIOB
	0x4002 0000 - 0x4002 03FF	GPIOA

**Table 10. STM32F401xB/STM32F401xC
register boundary addresses (continued)**

Bus	Boundary address	Peripheral
APB1	0x4000 7000 - 0x4000 73FF	PWR
	0x4000 6000 - 0x4000 6FFF	Reserved
	0x4000 5C00 - 0x4000 5FFF	I2C3
	0x4000 5800 - 0x4000 5BFF	I2C2
	0x4000 5400 - 0x4000 57FF	I2C1
	0x4000 4800 - 0x4000 53FF	Reserved
	0x4000 4400 - 0x4000 47FF	USART2
	0x4000 4000 - 0x4000 43FF	I2S3ext
	0x4000 3C00 - 0x4000 3FFF	SPI3 / I2S3
	0x4000 3800 - 0x4000 3BFF	SPI2 / I2S2
	0x4000 3400 - 0x4000 37FF	I2S2ext
	0x4000 3000 - 0x4000 33FF	IWDG
	0x4000 2C00 - 0x4000 2FFF	WWDG
	0x4000 2800 - 0x4000 2BFF	RTC & BKP Registers
	0x4000 1000 - 0x4000 27FF	Reserved
	0x4000 0C00 - 0x4000 0FFF	TIM5
	0x4000 0800 - 0x4000 0BFF	TIM4
	0x4000 0400 - 0x4000 07FF	TIM3
	0x4000 0000 - 0x4000 03FF	TIM2

6.1.6 Power supply scheme

Figure 18. Power supply scheme



1. To connect PDR_ON pin, refer to [Section 3.14: Power supply supervisor](#).
2. The 4.7 µF ceramic capacitor must be connected to one of the V_{DD} pin.
3. V_{CAP_2} pad is only available on LQFP100 and UFBGA100 packages.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

Table 12. Current characteristics

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source) ⁽¹⁾	160	mA
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink) ⁽¹⁾	-160	
I_{VDD}	Maximum current into each V_{DD_x} power line (source) ⁽¹⁾	100	
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink) ⁽¹⁾	-100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/O and control pin	-25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins ⁽²⁾	120	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	-120	
$I_{INJ(PIN)}$ ⁽³⁾	Injected current on FT pins ⁽⁴⁾	-5/+0	
	Injected current on NRST and B pins ⁽⁴⁾		
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins) ⁽⁵⁾	±25	

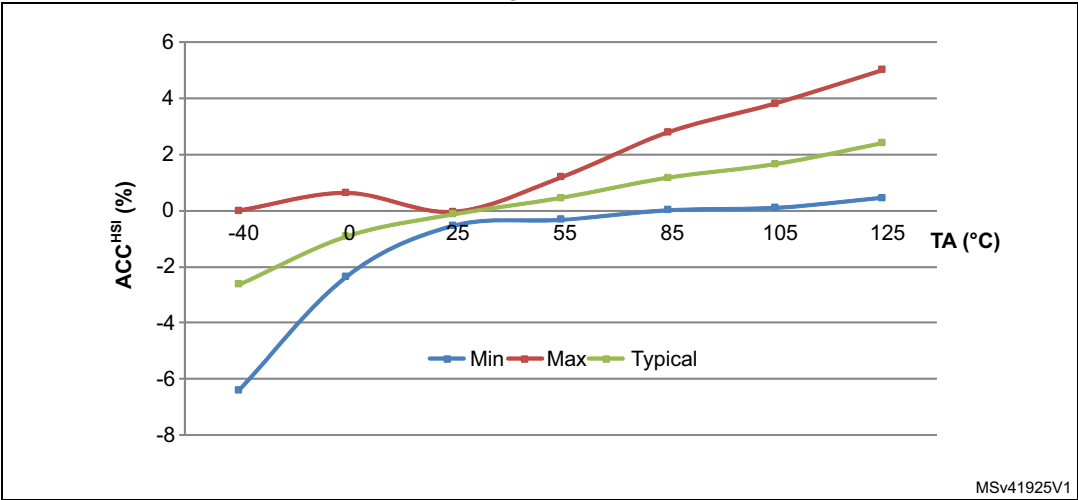
1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in [Section 6.3.20: 12-bit ADC characteristics](#).
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 13. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	-65 to +150	°C
T_J	Maximum junction temperature	125	
T_{LEAD}	Maximum lead temperature during soldering (WLCSP49, LQFP64/100, UFQFPN48, UFBGA100)	see note ⁽¹⁾	

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK[®] 7191395 specification, and the European directive on Restrictions on Hazardous Substances (ROHS directive 2011/65/EU, July 2011).

Figure 26. ACC_{HSI} versus temperature



1. Guaranteed by characterization.

Low-speed internal (LSI) RC oscillator

Table 40. LSI oscillator characteristics ⁽¹⁾

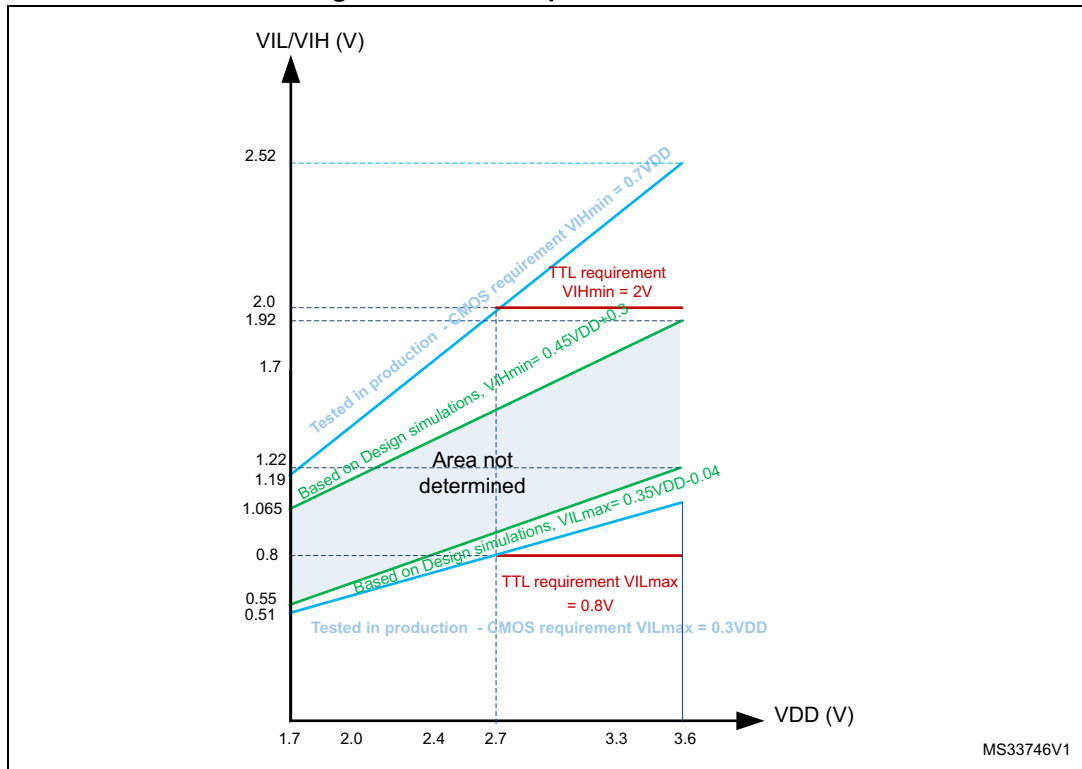
Symbol	Parameter	Min	Typ	Max	Unit
$f_{LSI}^{(2)}$	Frequency	17	32	47	kHz
$t_{su(LSI)}^{(3)}$	LSI oscillator startup time	-	15	40	μs
$I_{DD(LSI)}^{(3)}$	LSI oscillator power consumption	-	0.4	0.6	μA

1. $V_{DD} = 3 V$, $T_A = -40$ to $105\text{ }^{\circ}C$ unless otherwise specified.

2. Guaranteed by characterization.

3. Guaranteed by design.

Figure 30. FT I/O input characteristics



Output driving current

The GPIOs (general purpose input/outputs) can sink or source up to ± 8 mA, and sink or source up to ± 20 mA (with a relaxed V_{OL}/V_{OH}) except PC13, PC14 and PC15 which can sink or source up to ± 3 mA. When using the PC13 to PC15 GPIOs in output mode, the speed should not exceed 2 MHz with a maximum load of 30 pF.

In the user application, the number of I/O pins which can drive current must be limited to respect the absolute maximum rating specified in [Section 6.2](#). In particular:

- The sum of the currents sourced by all the I/Os on V_{DD} , plus the maximum Run consumption of the MCU sourced on V_{DD} , cannot exceed the absolute maximum rating ΣI_{VDD} (see [Table 12](#)).
- The sum of the currents sunk by all the I/Os on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS} cannot exceed the absolute maximum rating ΣI_{VSS} (see [Table 12](#)).

Output voltage levels

Unless otherwise specified, the parameters given in [Table 55](#) are derived from tests performed under ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#). All I/Os are CMOS and TTL compliant.

Table 55. Output voltage characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	CMOS port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	TTL port ⁽²⁾ $I_{IO} = +8 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	0.4	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		2.4	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +20 \text{ mA}$ $2.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$1.3^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-1.3^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +6 \text{ mA}$ $1.8 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(4)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(4)}$	-	
$V_{OL}^{(1)}$	Output low level voltage for an I/O pin	$I_{IO} = +4 \text{ mA}$ $1.7 \text{ V} \leq V_{DD} \leq 3.6 \text{ V}$	-	$0.4^{(5)}$	V
$V_{OH}^{(3)}$	Output high level voltage for an I/O pin		$V_{DD}-0.4^{(5)}$	-	

1. The I_{IO} current sunk by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS} .
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. The I_{IO} current sourced by the device must always respect the absolute maximum rating specified in [Table 12](#) and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD} .
4. Guaranteed by characterization.
5. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in [Figure 31](#) and [Table 56](#), respectively.

Unless otherwise specified, the parameters given in [Table 56](#) are derived from tests performed under the ambient temperature and V_{DD} supply voltage conditions summarized in [Table 14](#).

Table 56. I/O AC characteristics⁽¹⁾⁽²⁾

OSPEEDRy [1:0] bit value ⁽¹⁾	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
00	$f_{\max(I/O)out}$	Maximum frequency ⁽³⁾	$C_L = 50 \text{ pF}$, $V_{DD} \geq 2.70 \text{ V}$	-	-	4	MHz
			$C_L = 50 \text{ pF}$, $V_{DD} \geq 1.7 \text{ V}$	-	-	2	
			$C_L = 10 \text{ pF}$, $V_{DD} \geq 2.70 \text{ V}$	-	-	8	
			$C_L = 10 \text{ pF}$, $V_{DD} \geq 1.7 \text{ V}$	-	-	4	
	$t_{f(I/O)out}/$ $t_{r(I/O)out}$	Output high to low level fall time and output low to high level rise time	$C_L = 50 \text{ pF}$, $V_{DD} = 1.7 \text{ V}$ to 3.6 V	-	-	100	ns

6.3.19 Communications interfaces

I²C interface characteristics

The I²C interface meets the requirements of the standard I²C communication protocol with the following restrictions: the I/O pins SDA and SCL are mapped to are not “true” open-drain. When configured as open-drain, the PMOS connected between the I/O pin and VDD is disabled, but is still present.

The I²C characteristics are described in [Table 59](#). Refer also to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output alternate function characteristics (SDA and SCL).

The I²C bus interface supports standard mode (up to 100 kHz) and fast mode (up to 400 kHz). The I²C bus frequency can be increased up to 1 MHz. For more details about the complete solution, please contact your local ST sales representative.

Table 59. I²C characteristics

Symbol	Parameter	Standard mode I ² C ⁽¹⁾		Fast mode I ² C ⁽¹⁾⁽²⁾		Unit
		Min	Max	Min	Max	
t _w (SCLL)	SCL clock low time	4.7	-	1.3	-	μs
t _w (SCLH)	SCL clock high time	4.0	-	0.6	-	
t _{su} (SDA)	SDA setup time	250	-	100	-	ns
t _h (SDA)	SDA data hold time	0	-	0	900 ⁽³⁾	
t _r (SDA) t _r (SCL)	SDA and SCL rise time	-	1000	-	300	
t _f (SDA) t _f (SCL)	SDA and SCL fall time	-	300	-	300	
t _h (STA)	Start condition hold time	4.0	-	0.6	-	μs
t _{su} (STA)	Repeated Start condition setup time	4.7	-	0.6	-	
t _{su} (STO)	Stop condition setup time	4.0	-	0.6	-	μs
t _w (STO:STA)	Stop to Start condition time (bus free)	4.7	-	1.3	-	μs
t _{SP}	Pulse width of the spikes that are suppressed by the analog filter for standard fast mode	0	50 ⁽⁴⁾	0	50 ⁽⁴⁾	ns
C _b	Capacitive load for each bus line	-	400	-	400	pF

1. Guaranteed by design.
2. f_{PCLK1} must be at least 2 MHz to achieve standard mode I²C frequencies. It must be at least 4 MHz to achieve fast mode I²C frequencies, and a multiple of 10 MHz to reach the 400 kHz maximum I²C fast mode clock.
3. The maximum data hold time has only to be met if the interface does not stretch the low period of SCL signal.
4. The minimum width of the spikes filtered by the analog filter is above t_{SP} (max).

USB OTG full speed (FS) characteristics

This interface is present in USB OTG FS controller.

Table 63. USB OTG FS startup time

Symbol	Parameter	Max	Unit
$t_{\text{STARTUP}}^{(1)}$	USB OTG FS transceiver startup time	1	μs

1. Guaranteed by design.

Table 64. USB OTG FS DC electrical characteristics

Symbol		Parameter	Conditions	Min. ⁽¹⁾	Typ.	Max. ⁽¹⁾	Unit
Input levels	V_{DD}	USB OTG FS operating voltage		3.0 ⁽²⁾	-	3.6	V
	$V_{\text{DI}}^{(3)}$	Differential input sensitivity	I(USB_FS_DP/DM)	0.2	-	-	V
	$V_{\text{CM}}^{(3)}$	Differential common mode range	Includes V_{DI} range	0.8	-	2.5	
	$V_{\text{SE}}^{(3)}$	Single ended receiver threshold		1.3	-	2.0	
Output levels	V_{OL}	Static output level low	R_{L} of 1.5 k Ω to 3.6 V ⁽⁴⁾	-	-	0.3	V
	V_{OH}	Static output level high	R_{L} of 15 k Ω to $V_{\text{SS}}^{(4)}$	2.8	-	3.6	
R_{PD}		PA11, PA12 (USB_FS_DM/DP)	$V_{\text{IN}} = V_{\text{DD}}$	17	21	24	k Ω
		PA9 (OTG_FS_VBUS)		0.65	1.1	2.0	
R_{PU}		PA11, PA12 (USB_FS_DM/DP)	$V_{\text{IN}} = V_{\text{SS}}$	1.5	1.8	2.1	
		PA9 (OTG_FS_VBUS)	$V_{\text{IN}} = V_{\text{SS}}$	0.25	0.37	0.55	

1. All the voltages are measured from the local ground potential.
2. The USB OTG FS functionality is ensured down to 2.7 V but not the full USB full speed electrical characteristics which are degraded in the 2.7-to-3.0 V V_{DD} voltage range.
3. Guaranteed by design.
4. R_{L} is the load connected on the USB OTG FS drivers.

Note: When VBUS sensing feature is enabled, PA9 should be left at their default state (floating input), not as alternate function. A typical 200 μA current consumption of the embedded sensing block (current to voltage conversion to determine the different sessions) can be observed on PA9 when the feature is enabled.

Refer to [Section 6.3.16: I/O port characteristics](#) for more details on the input/output characteristics.

Figure 44. SDIO high-speed mode

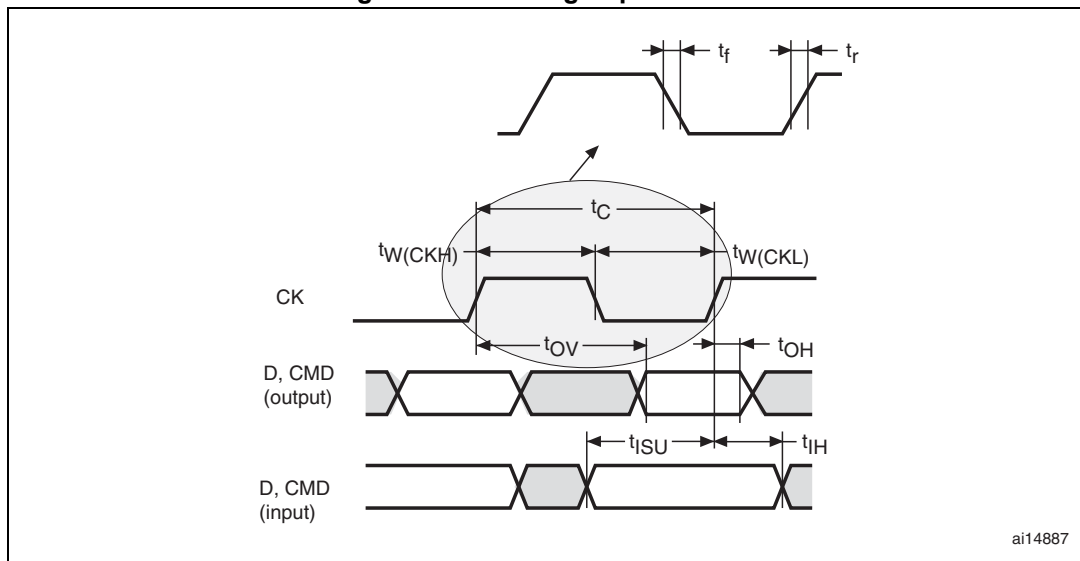


Figure 45. SD default mode

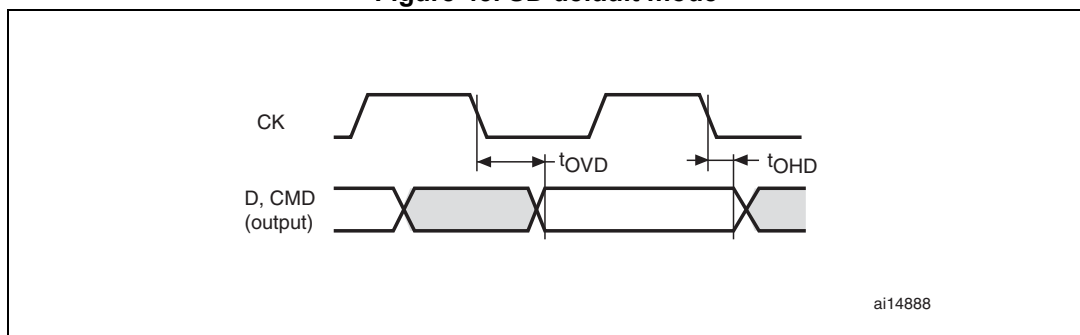


Table 77. Dynamic characteristics: SD / MMC characteristics⁽¹⁾⁽²⁾

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f _{PP}	Clock frequency in data transfer mode		0	-	48	MHz
-	SDIO_CK/fPCLK2 frequency ratio		-	-	8/3	-
t _{W(CKL)}	Clock low time	fpp = 48MHz	8.5	9	-	ns
t _{W(CKH)}	Clock high time	fpp = 48MHz	8.3	10	-	
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t _{ISU}	Input setup time HS	fpp = 48MHz	3.5	-	-	ns
t _{IH}	Input hold time HS	fpp = 48MHz	0	-	-	
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t _{OV}	Output valid time HS	fpp = 48MHz	-	4.5	7	ns
t _{OH}	Output hold time HS	fpp = 48MHz	3	-	-	

9 Revision history

Table 88. Document revision history

Date	Revision	Changes
23-Jul-2013	1	Initial release.
06-Sep-2013	2	Updated product status to production data Added I2C 1 MBit/s in Features Updated Figure 1: Compatible board design for LQFP100 package Added notes and revised the main function after reset columnn Table 8: STM32F401xB/STM32F401xC pin definitions. Replaced 'I2S2_CKIN' signal name with 'I2S_CKIN' and added EVENTOUT alternate function in Table 8: STM32F401xB/STM32F401xC pin definitions and Table 9: Alternate function mapping Updated Section 3.28: Analog-to-digital converter (ADC) Updated the reference of $V_{ESD(CDM)}$ in Table 51: ESD absolute maximum ratings Updated Section 3.20: Inter-integrated circuit interface (I2C), including Table 5: Comparison of I2C analog and digital filters Removed first sentence ("Unless otherwise specified...") in I2C interface characteristics Changed the order of the tables in Section 6.3.6: Supply current characteristics Modified the "SDA and SCL rise time" fast mode I2C minimum value in Table 59: I²C characteristics Updated Figure 33: I²C bus AC waveforms and measurement circuit and Table 60: SCL frequency ($f_{PCLK1} = 42$ MHz, $V_{DD} = V_{DD_I2C} = 3.3$ V) Replaced "Marking of engineering samples" sections with "Marking of samples" sections, and added UFBGA100 device marking section for package UFBGA100 in Section 7: Package information
08-Nov-2013	3	Updated UFBGA100 in Table 86: Package thermal characteristics. Changed WLCSP49 package measurements to 3 x 3 mm in Section 7.1.